# 7.8 inch
# E-paper Display Series

GooDisplay®

## GDEW078M01

Dalian Good Display Co., Ltd.

# Product Specifications

| | |
|---|---|
| **Customer** | **Standard** |
| **Description** | **7.8” E-PAPER DISPLAY** |
| **Model Name** | **GDEW078M01** |
| **Date** | **2020/07/03** |
| **Revision** | **1.0** |

| | Design Engineering | | |
|---|---|---|---|
| | **Approval** | **Check** | **Design** |
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# Revision History

| Rev. | Issued Date | Revised Contents |
|---|---|---|
| 1.0 | Jul.30.2020 | Preliminary |
| | | |
| | | |

# 1. General Description

## 1.1 Over View

The display is a TFT active matrix electrophoretic display, with interface and a reference system design. The 7.8” active area contains 1404×1872 pixels, and has 2-16 gray levels (1-4 bits) white/black full display capabilities.

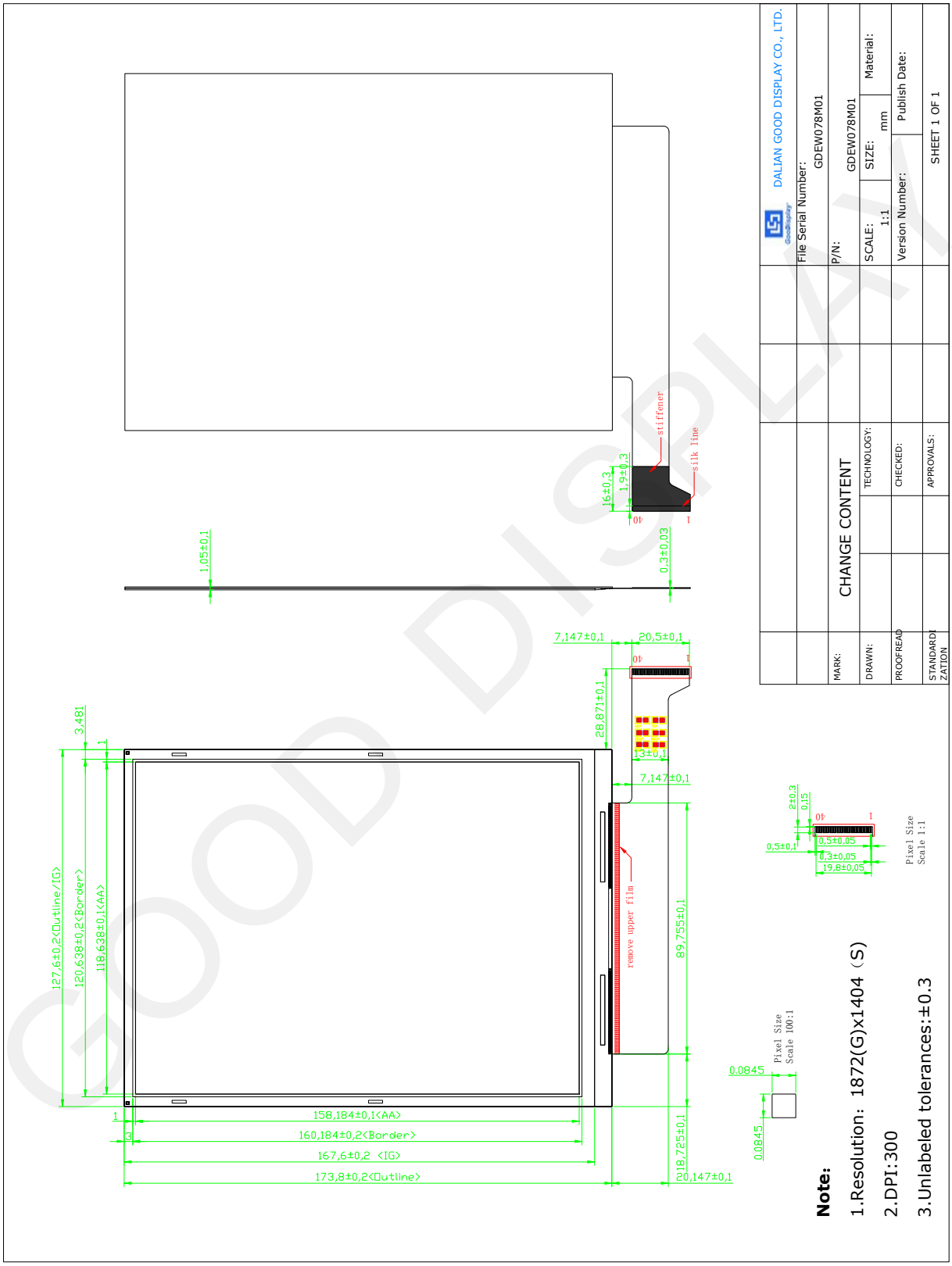
## 1.2 Features

- Carta high contrast reflective/electrophoretic technology
- 1404 x 1872 resolution
- Ultra wide viewing angle
- Low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode

## 1.3 Mechanical Specifications

| Parameter | Specifications | Unit | Remark |
|---|---|---|---|
| Screen Size | 7.8 | Inch | |
| Display Resolution | 1404(V)×1872 (H) | Pixel | Dpi: 300 |
| Active Area | 118.638(V)×158.184(H) | mm | |
| Pixel Pitch | 0.0845×0.0845 | mm | |
| Pixel Configuration | Square | | |
| Outline Dimension | 127.6(V)×173.8(H) ×1.05(D) | mm | |
| Weight | 54.2±0.2 | g | |

## 1.4 Mechanical Drawing of DES module



## 1.5 Input/Output Terminals

### 1.5.1 Pin out List

| Pin # | Single | Description |
|---|---|---|
| **1** | VGL | Negative power supply gate driver |
| **2** | NC | No connection |
| **3** | VGH | Positive power supply gate driver |
| **4** | NC | No connection |
| **5** | VDD | Digital power supply drivers |
| **6** | Mode | Output mode selection gate driver |
| **7** | CKV | Clock gate driver |
| **8** | SPV | Start pulse gate driver |
| **9** | VSS | Ground |
| **10** | VCOM | Common connection |
| **11** | VDD | Digital power supply drivers |
| **12** | VSS | Ground |
| **13** | XCL | Clock source driver |
| **14** | D0 | Data signal source driver |
| **15** | D1 | Data signal source driver |
| **16** | D2 | Data signal source driver |
| **17** | D3 | Data signal source driver |
| **18** | D4 | Data signal source driver |
| **19** | D5 | Data signal source driver |
| **20** | D6 | Data signal source driver |
| **21** | D7 | Data signal source driver |
| **22** | VSS | Ground |
| **23** | D8 | Data signal source driver |
| **24** | D9 | Data signal source driver |
| **25** | D10 | Data signal source driver |
| **26** | D11 | Data signal source driver |
| **27** | D12 | Data signal source driver |
| **28** | D13 | Data signal source driver |
| **29** | D14 | Data signal source driver |
| **30** | D15 | Data signal source driver |
| **31** | XSTL | Start pulse gate driver |
| **32** | XLE | Latch enable source driver |
| **33** | XOE | Output enable source driver |
| **34** | TEST | Internal test pin (Note 1) |
| **35** | NC | No connection |
| **36** | VPOS | Positive power supply source driver |
| **37** | NC | No connection |

| | | |
|---|---|---|
| **38** | VNEG | Negative power supply source driver |
| **39** | NC | No connection |
| **40** | Border | Border connection |

**Note 1:** Please connect to VDD voltage.

# 2. Environmental

## 2.1 Handling, Safety and Environmental Requirements

| Warning |
| --- |
| The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap. |

| Caution |
| --- |
| The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. |
| Disassembling the display module can cause permanent damage and invalidate the warranty agreements. |

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

| Data sheet status | |
| --- | --- |
| Product specification | The data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134).<br>Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and dose not form part of the specification. | |

| Product environmental certification |
| --- |
| RoHS |

## 2.2 Reliability test

| | TEST | CONDITION | METHOD | REMARK |
|---|---|---|---|---|
| 1 | High-Temperature Operation | T = 60℃, RH=20% for 240 hrs | When the experimental cycle finished, the DES samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As DESs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Bp. | When experiment finished, the DES must meet electrical and optical performance standards. |
| 2 | Low-Temperature Operation | T = -20℃ for 240 hrs | When the experimental cycle finished, the DES samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As DESs return room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Ab. | When experiment finished, the DES must meet electrical and optical performance standards. |
| 3 | High-Temperature Storage | T = +70℃, RH=20% for 240 hrs Test in white pattern | When the experimental cycle finished, the DES samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As DESs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Bp. | When experiment finished, the DES must meet electrical and optical performance standards. |
| 4 | Low-Temperature Storage | T = -25℃ for 240 hrs Test in white pattern | When the experimental cycle finished, the DES samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As DESs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Ab | When experiment finished, the DES must meet electrical and optical performance standards. |
| 5 | High Temperature, High-Humidity Operation | T=+40℃, RH=90% for240hrs | When the experimental cycle finished, the DES samples will be taken out from the environmental chamber and set aside for a few minutes. As DESs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-3CA. | When experiment finished, the DES must meet electrical and optical performance standards. |
| 6 | High Temperature, High-Humidity Storage | T=+60℃, RH=80% for 240 hrs Test in white pattern | When the experimental cycle finished, the DES samples will be taken out from the environmental chamber and set aside for a few minutes. As DESs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-3CA. | When experiment finished, the DES must meet electrical performance standards. |
| 7 | Temperature Cycle | [-25℃ 30mins]→ [+70℃, RH=20% 30mins], | 1. Samples are put in the Temp & Humid. Environmental Chamber. Temperature cycle starts with -25℃, storage period 30 minutes. After 30 minutes, it needs 30min to | When experiment finished, the DES must meet electrical |

| | | | | |
|---|---|---|---|---|
| | | 70cycles,<br>Test in white pattern | let temperature rise to 75℃. After 30min, temperature will be adjusted to 75℃, RH=20% and storage period is 30 minutes. After 30 minutes, it needs 30min to let temperature rise to -25℃. One temperature cycle (2hrs) is complete.<br>2. Temperature cycle repeats 70 times.<br>3. When 70 cycles finished, the samples will be taken out from experiment chamber and set aside a few minutes. As DESs return to room temperature, tests will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-14NB. | and optical performance standards. |
| 8 | UV exposure Resistance | 765 W/m$^2$ for 168 hrs,40℃ | Standard # IEC 60 068-2-5 Sa | |
| 9 | Electrostatic discharge | Machine model:<br>+/-250V,<br>0Ω,200pF | Standard # IEC61000-4-2 | |
| 10 | Package Vibration | 1.04G,Frequency : 10~500Hz<br>Direction : X,Y,Z<br>Duration:1hours in each direction | Full packed for shipment | |
| 11 | Package Drop Impact | Drop from height of 122 cm on Concrete surface<br>Drop sequence:1 corner, 3edges, 6face<br>One drop for each. | Full packed for shipment | |

Actual EMC level to be measured on customer application.

**Note :**

(1) The protective film must be removed before temperature test.

(2) In order to make sure the display module can provide the best display quality, the update should be made after putting the display module in stable temperature environment for 4 hours at 25℃.

# 3. Electrical Characteristics

## 3.1 Absolute maximum rating

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Logic Supply Voltage | VDD | -0.3 to +5 | V |
| Positive Supply Voltage | $V_{POS}$ | -0.3 to +18 | V |
| Negative Supply Voltage | $V_{NEG}$ | -0.3 to -18 | V |
| Max .Drive Voltage Range | $V_{POS}$ -$V_{NEG}$ | 36 | V |
| Supply Voltage | VGG | -0.3 to +45 | V |
| Supply Voltage | VEE | -25.0 to +0.3 | V |
| Supply Range | VGG-VGL | -0.3 to +45 | V |
| Operating Temp. range | $T_{OPR}$ | -20 to +60 | ℃ |
| Storage Temp. range | $T_{STG}$ | -25 to +75 | ℃ |

## 3.2 Panel DC Characteristics

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Single ground | $V_{SS}$ | | - | 0 | - | V |
| Logic Supply Voltage | $V_{DD}$ | | 1.7 | 3.0 | 3.6 | V |
| | $I_{VDD}$ | $V_{DD}$=3.0V | - | 3.1 | 7.8 | mA |
| Gate Negative Supply | VGL | | -20 | - | VNEG-4 | V |
| | $I_{GL}$ | VGL=-20V | - | 1.2 | 12 | mA |
| Gate Positive Supply | VGH | | 7 | VGL+42 | VGL+45 | V |
| | $I_{GH}$ | VGH=22V | - | 1.2 | 2.5 | mA |
| Source Negative Supply | $V_{NEG}$ | | -15.4 | - | -10 | V |
| | $I_{NEG}$ | $V_{NEG}$ = -15V | - | 8.5 | 160 | mA |
| Source Positive Supply | $V_{POS}$ | | 10 | - | 15 | V |
| | $I_{POS}$ | $V_{POS}$ = 15V | - | 8.2 | 166 | mA |
| Border Supply | $V_{com}$ | | -4 | Adjusted | -0.2 | V |
| Asymmetry Source | $V_{ASYM}$ | $V_{POS}$ + $V_{NEG}$ | -800 | 0 | 800 | mV |
| Common voltage | $V_{COM}$ | | -4 | Adjusted | -0.2 | V |
| | $I_{COM}$ | | - | 0.2 | - | mA |
| Panel Power | P | | - | 285 | 4680 | mW |
| Standby power panel | $P_{STBY}$ | | - | - | 1.3 | mW |

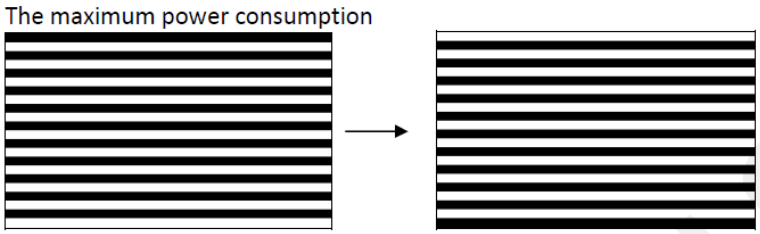
- The maximum power consumption is measured using 85 Hz waveform with following pattern transition: from pattern of repeated 1 consecutive black scan lines followed by 1 consecutive white scan line to that of repeated 1 consecutive white scan lines followed by 1 consecutive black scan lines. (Note 1)

- The Typical power consumption is measured using 85 Hz waveform with following pattern transition: from horizontal 4 gray scale pattern to vertical 4 gray scale pattern. (Note 2)

- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display.
- Vcom is recommended to be set in the range of assigned value ± 0.1 V
- The maximum $I_{COM}$ inrush current is about 1000 mA
- Customer need to use decoupling capacitors on each power rail at system board as below table to keep EPD driving power stable. (Note 3)

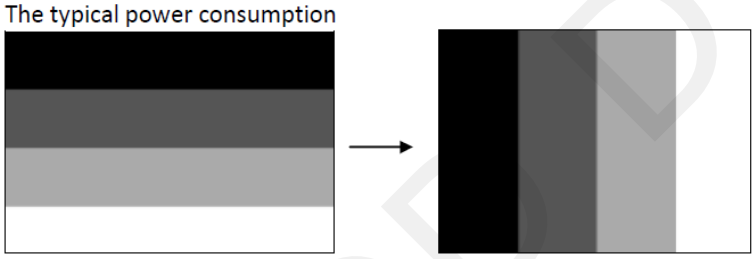
**Note 1**

The maximum power consumption




Note 2

The typical power consumption



**Note 3**

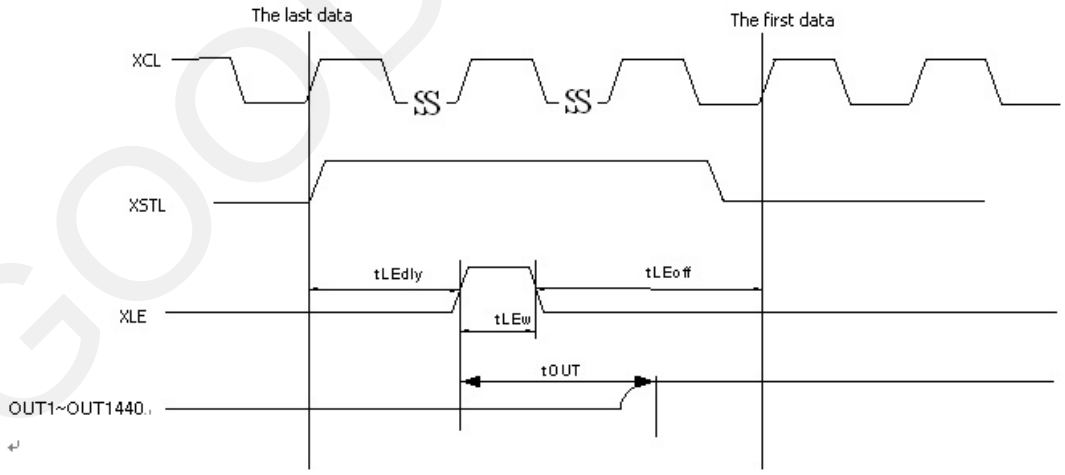
The decoupling capacitors on each power rail at customer system side

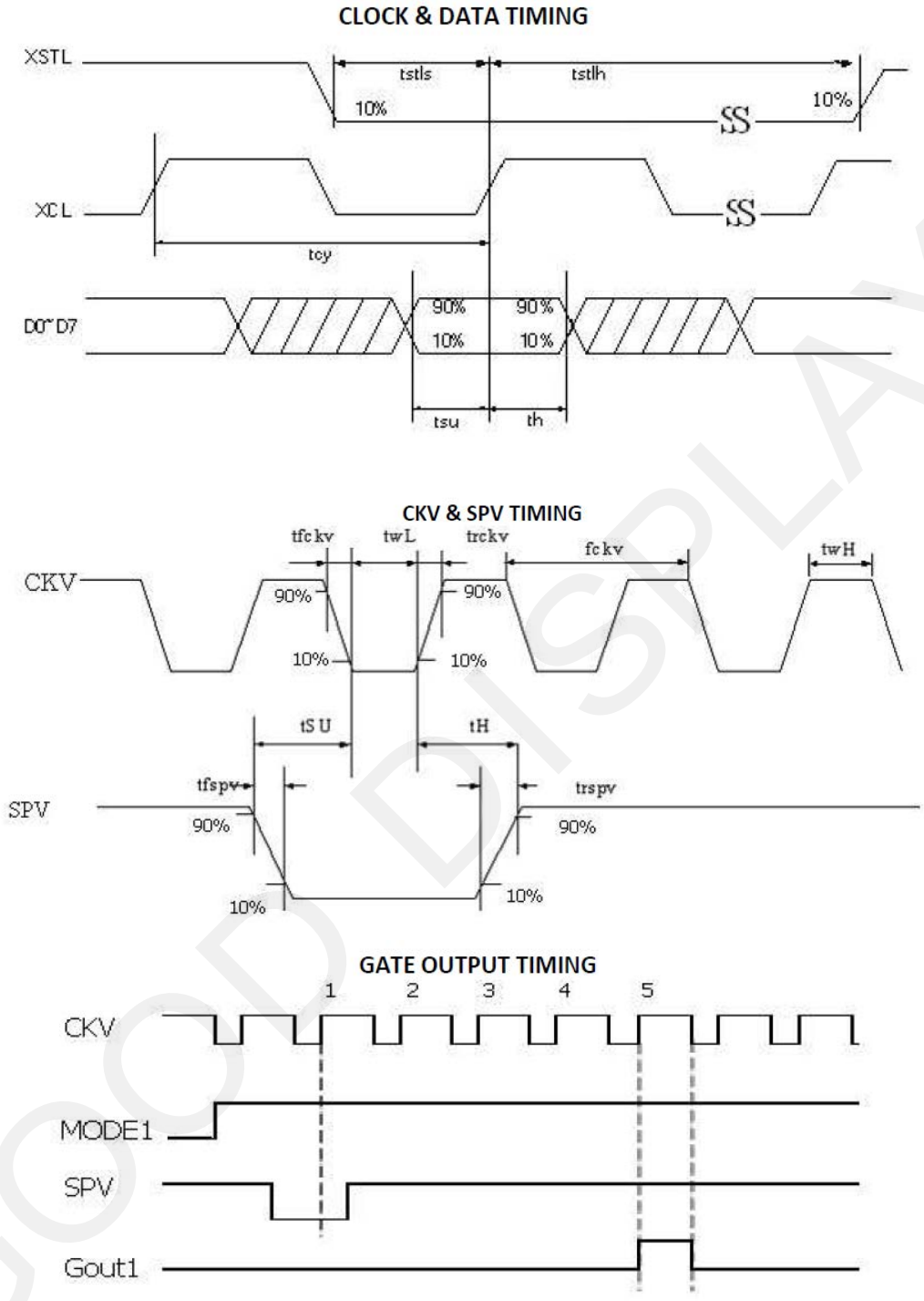
| Power rail | Capacitors suggested ( uF / Tolerance) |
|---|---|
| IPOS | 4.7uF x 2pcs / ±10% |
| INEG | 4.7uF x 2pcs / ±10% |
| IGH | 4.7uF x 1pcs / ±10% |
| IGL | 4.7uF x 1pcs / ±10% |
| IDD | 4.7uF x 1pcs / ±10% |

## 3.3 Panel AC Characteristics

VDD=3.0V, unless otherwise specified.

| Parameter | Symbol | Min. | Typ. | Max. | unit |
|---|---|---|---|---|---|
| Clock frequency | fckv | - | - | 200 | kHz |
| Minimum ”L” clock pulse width | twL | 1 | - | - | us |
| Minimum ”H” clock pulse width | twH | 1 | - | - | us |
| Clock rise time | trckv | - | - | 100 | ns |
| Clock fall time | tfckv | - | - | 100 | ns |
| SPV setup time | tSU | 100 | - | twH-100 | ns |
| SPV hold time | tH | 100 | - | twH-100 | ns |
| Pulse rise time | trspv | - | - | 100 | ns |
| Pulse fall time | tfspv | - | - | 100 | ns |
| Clock XCL cycle time | tcy | 22.22 | - | - | ns |
| D0..D7setup time | tsu | 11 | - | - | ns |
| D0..D7 hold time | th | 11 | - | - | ns |
| XSTL setup time | tstls | 0.5*tcy | - | 0.8*tcy | ns |
| XSTL hold time | tstlh | 0.5*tcy | - | - | ns |
| XLE on delay time | tLEdly | 4.5*tcy | - | - | ns |
| LEH high-level pulse width （When VDD=1.7V to 2.1V） | tLEW | 400 | - | - | ns |
| XLE off delay time | tLEoff | 250 | - | - | ns |
| Output setting time to +/-30mV ($C_{load}$=200pF) | tout | - | - | 20 | us |






**Note 1:** First gate line on timing . After 5 CKV, gate line be on.

## 3.4 Refresh rate

The module applied at a maximum refresh rate of 85 Hz.

| | Min | Max |
|---|---|---|
| Refresh rate | - | 85Hz |

## 3.5 Controller Timing

This timing mode is depicted on Figure 1 and Figure 2 and it refers to timing of Source Driver Output Enable (SDOE) and Gate Driver Clock (GDCK). Note, that in this mode LGON follows GDCK timing.

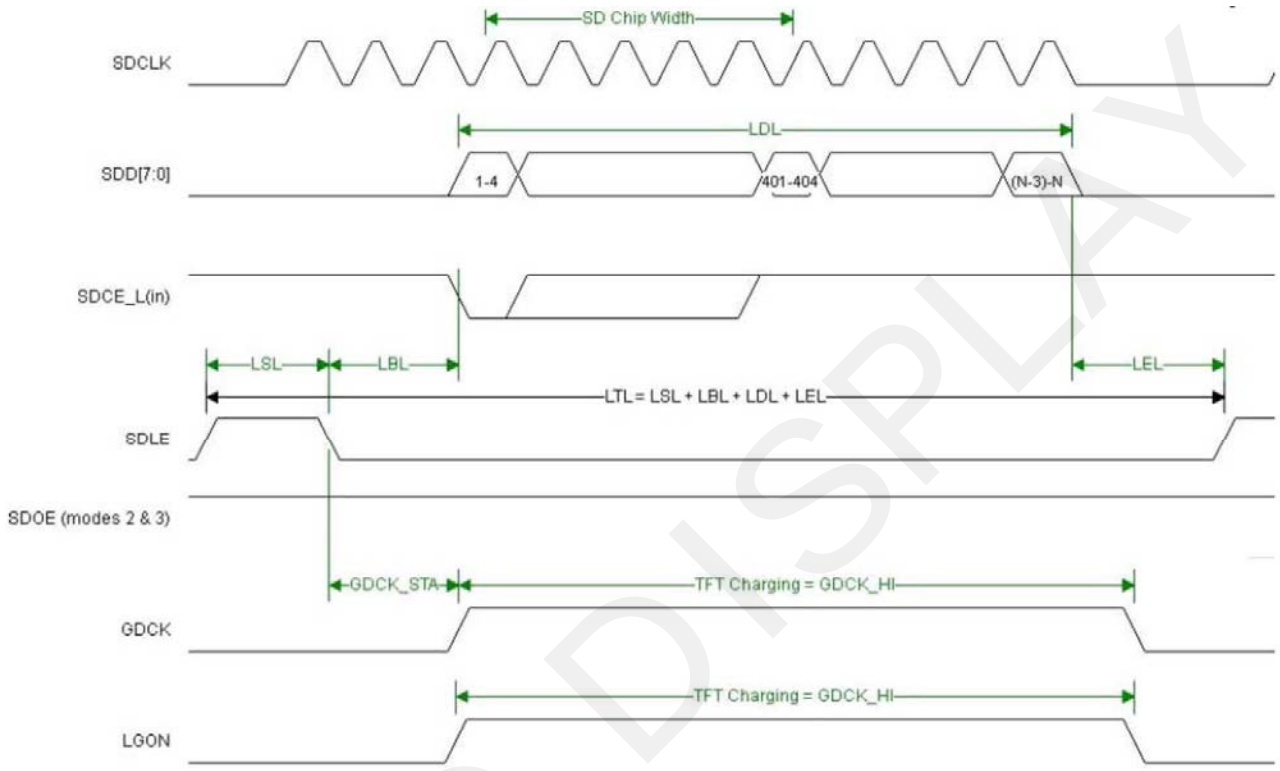



Figure 1 Line Timing in Mode 3

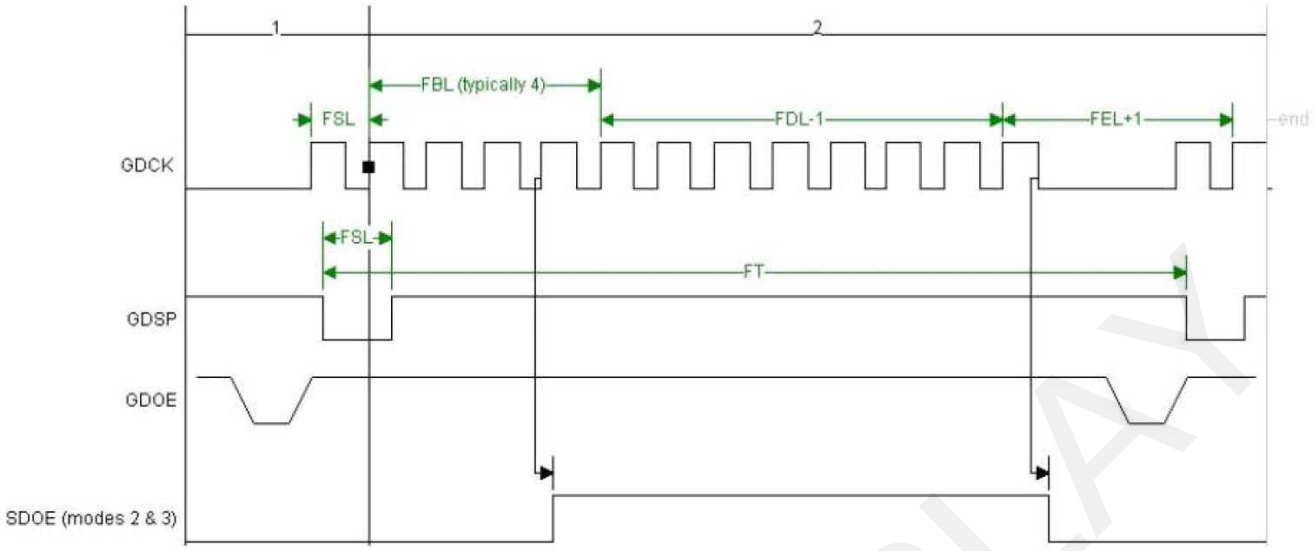



Figure 2 Frame Timing in Mode 3

| Mode | 3 | | | | | |
|---|---|---|---|---|---|---|
| SDCK(MHz) | 33.33 | | | | | |
| Pixel per SDCK | 8 | | | | | |
| Line Parameters | LSL | LBL | LDL | LEL | GDCK_STA | LGONL |
| (SDCK) | 18 | 17 | 234 | 7 | 34 | 192 |
| Line Parameters | - | - | - | - | - | - |
| (us) | 0.54 | 0.51 | 7.02 | 0.21 | 1.02 | 5.76 |
| Frame parameters | FSL | FBL | FDL | FEL | - | FR(Hz) |
| (lines) | 1 | 4 | 1404 | 12 | - | 84.99 |
| Frame parameters | | | | | - | - |
| (us) | 8.28 | 33.12 | 11625.12 | 99.36 | - | - |

**Note 1:** For parameters definition , see Section 6. Active Matrix Electronic Paper Display Timings

**Note 2:** For Isis Controller GDCK_STA and LGONL are not settable parameters ; GDCK_STA=LBL, LGONL=LDL+0.5

**Note 3:** For Freescale SoC GDOE Low pulse represent FSL and GDSP pulses with the first period of FBL

**Note 4:** SDCLK = XCL

SDD[7:0] = D0~D7

SDCE_L(in) = XSTL

GDCK = CKV

GDSP = SPV

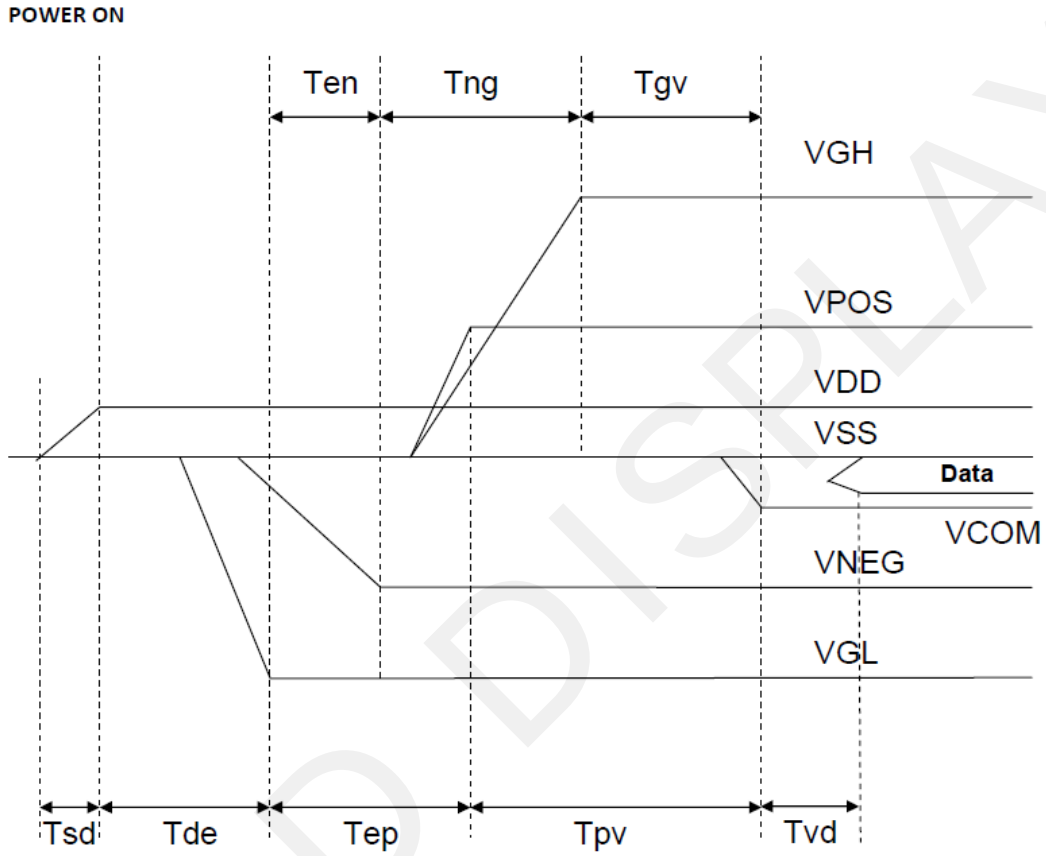
GDOE = Mode 1

SDOE = XOE

## 4. Power on sequence

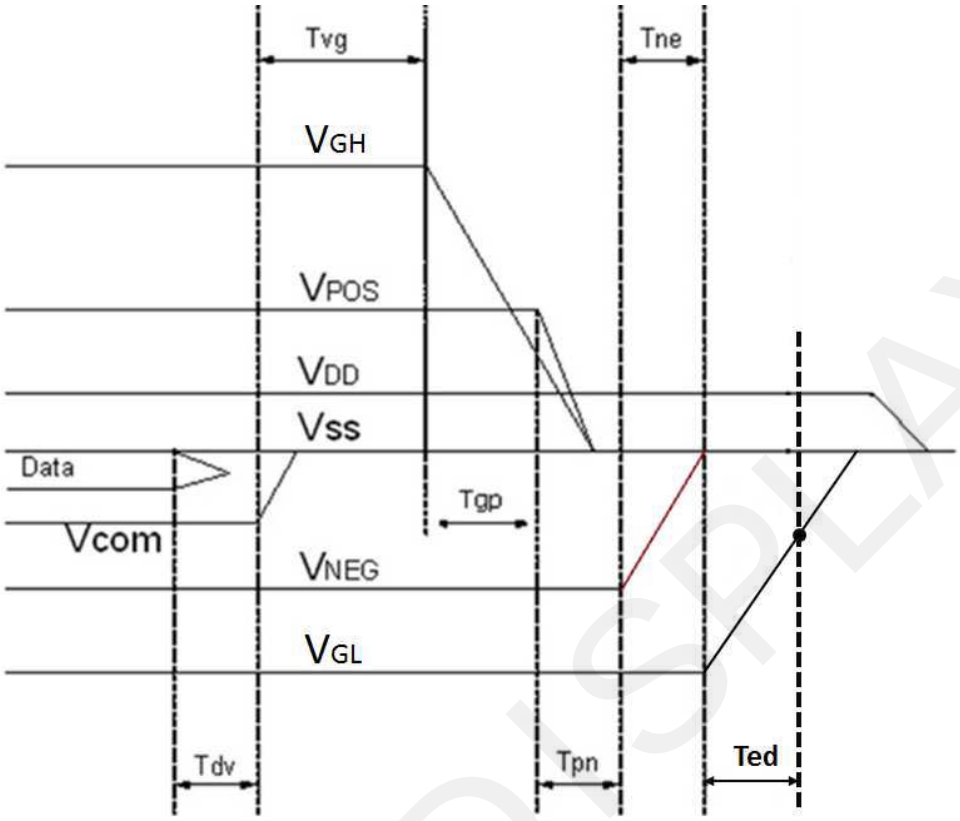
Power Rails must be sequenced in following order:

1. VSS→VDD→VNEG→VPOS (Source driver) →VCOM
2. VSS→VDD→VGL→VGH(Gate drive)




| | Min | Max |
|---|---|---|
| Tsd | 30us | - |
| Tde | 100us | - |
| Tep | 1000us | - |
| Tpv | 100us | - |
| Tvd | 100us | - |
| Ten | 0us | - |
| Tng | 1000us | - |
| Tgv | 100us | - |

Power OFF




| | Min | Max | Remark |
|---|---|---|---|
| Tdv | 100us | - | - |
| Tvg | 0us | - | - |
| Tgp | 0us | - | - |
| Tpn | 0us | - | - |
| Tne | 0us | - | - |
| Ted | 0.5s | - | Discharged point @ -7.4 Volt |

**Note 1:** Supply voltages decay through pull-down resistors.

**Note 2:** Turn off VGL power after VNEG and VPOS power discharged to GND state.

**Note 3:** VGL must remain negative of Vcom during decay period.

# 5. Optical Characteristics

## 5.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25℃

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYPE | MAX | UNIT | Note |
|---|---|---|---|---|---|---|---|
| R | Reflectance | White | 30 | 35 | - | % | Note 5-1 |
| Gn | $N_{th}$ Grey Level | - | - | DS+(WS-DS)×n/(m-1) | - | L* | - |
| CR | Contrast Ratio | indoor | 8 | | - | - | - |
| $T_{update}$ | Update time | 25℃ | - | 1 | - | Sec | - |
| Panel's life | | -20℃~60℃ | | 1000000 times or 5 years | - | - | Note 5-2 |

WS : White state; DS : Dark state, Gray state from Dark to White :

DS、G1、G2…、Gn…、Gm-2、WS

m : 4、8、16 when 2、3、4 bit mode.

**Note 5-1:** Luminance meter: Eye – One Pro Spectrophotometer

**Note 5-2:** Each update interval time should be minimum at 180 seconds.

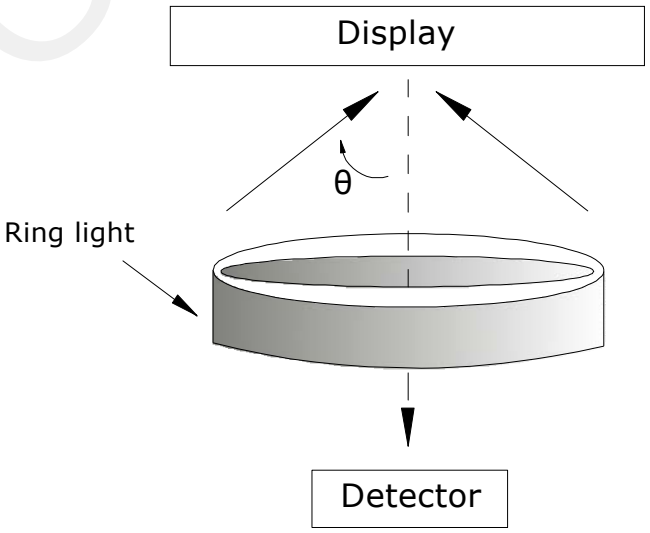
**Note 5-3:** When work in temperature 60 degree, suggest update once every 1hours.

## 5.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd)() :

R1: white reflectance Rd: dark reflectance

CR = R1/Rd

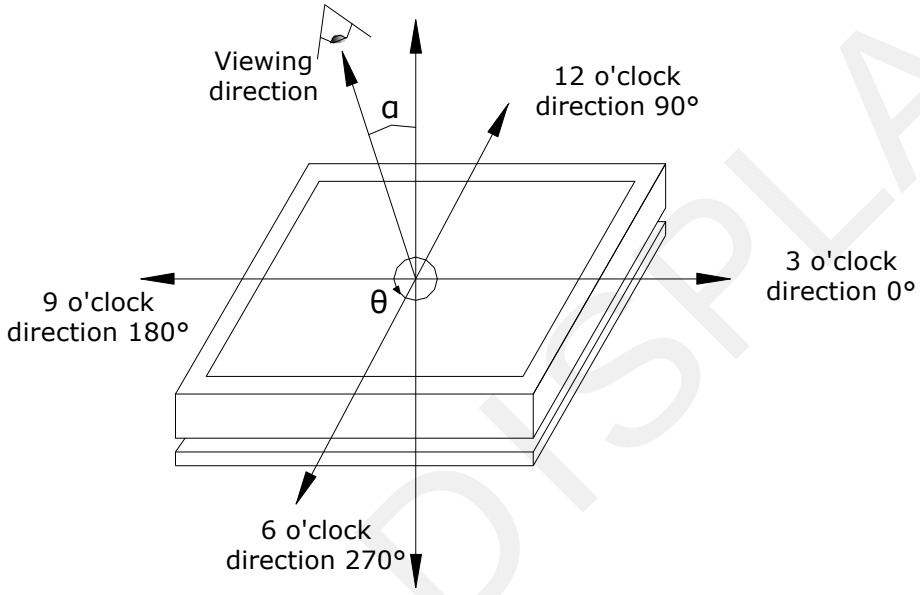


## 5.3 Reflection Ratio

The reflection ratio is expressed as :

R = Reflectance Factor $_{\text{white board}}$ x ($L_{\text{center}}$ / $L_{\text{white board}}$ )

$L_{\text{center}}$ is the luminance measured at center in a white area (R=G =B=1) . $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



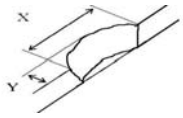
# 6. Point and line standard

## Shipment Inseption Standard

Part-A：Active area　　Part-B：Border area

Equipment：Electrical test fixture, Point gauge

Outline dimension：
127.6(V)×173.8(H) ×1.05(D)　　Unit：mm

<table>
<tr><td rowspan="2">Environment</td><td>Temperature</td><td>Humidity</td><td>Illuminance</td><td>Distance</td><td>Time</td><td>Angle</td></tr>
<tr><td>23±2℃</td><td>55± 5%RH</td><td>1200～ 1500Lux</td><td>300 mm</td><td>35 Sec</td><td></td></tr>
<tr><td>Name</td><td>Causes</td><td colspan="3">Spot size</td><td>Part-A</td><td>Part-B</td></tr>
<tr><td rowspan="4">Spot</td><td rowspan="4">B/W spot in glass or protection sheet, foreign mat. Pin hole</td><td colspan="3">D ≤ 0.25mm</td><td>Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td colspan="3">0.25mm ＜ D ≤ 0.4mm</td><td>4</td></tr>
<tr><td colspan="3">0.4mm ＜ D ≤ 0.5mm</td><td>2</td></tr>
<tr><td colspan="3">0.5mm ＜ D</td><td>0</td></tr>
<tr><td rowspan="4">Scratch or line defect</td><td rowspan="4">Scratch on glass or Scratch on FPL or Particle is Protection sheet.</td><td>Length</td><td>Width</td><td></td><td>Part-A</td><td rowspan="4">Ignore</td></tr>
<tr><td>L ≤3mm</td><td>W≤0.1 mm</td><td></td><td>Ignore</td></tr>
<tr><td>3 mm < L≤ 6mm</td><td>0.1 mm<W≤ 0.2mm</td><td></td><td>2</td></tr>
<tr><td>6 mm < L</td><td>0.2mm < W</td><td></td><td>0</td></tr>
<tr><td rowspan="3">Air bubble</td><td rowspan="3">Air bubble</td><td colspan="3">D1, D2 ≤ 0.3 mm</td><td>Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td colspan="3">0.3 mm < D1,D2 ≤ 0.5mm</td><td>4</td></tr>
<tr><td colspan="3">0.5mm < D1, D2</td><td>0</td></tr>
<tr><td rowspan="2">Side Fragment</td><td colspan="6">  </td></tr>
<tr><td colspan="6">X≤6mm，Y≤1mm & display is ok, Ignore</td></tr>
</table>

Remarks: Spot define: That only can be seen under WS or DS defects.

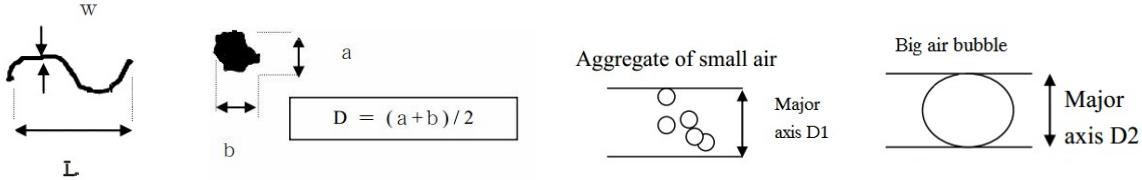
Any defect which is visible under gray pattern or transition process but invisible under black and white is disregarded.

Here is definition of the “Spot” and “Scratch or line defect”.

Spot: W > 1/4L　　Scratch or line defect: W ≤1/4L

Definition for L/W and D (major axis)

FPC bonding area pad doesn’t allowed visual inspection.




**Note** AQL = 0.4

## 7. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as “Ghosting” or “Image Sticking” may occur. It is recommended to refreshed the ESL /EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel’s performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.

(7) For more precautions, please click on the link:
*https://www.good-display.com/news/80.html*