10.2 inch
E-paper Display Series

GDEQ102T90

Dalian Good Display Co., Ltd.

GooDisplay®

Product Specifications

Customer	**Standard**
Description	10.2 ” E-PAPER DISPLAY
Model Name	GDEQ102**T**90
Date	2022/0**5**/**31**
Revision	**1.0**

	Design Engineering		
	Approval	**Check**	**Design**
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Table of Contents

Version	Content	Date	Producer
1.0	New release	2022/05/31	

1. General Description

1.1 Overview

GDEQ102T90 is a reflective electrophoretic display module on an active matrix TFT substrate, The diagonal length of the active area is 10.2 ” and contains 960 x 640 pixels. The panel is capable of displaying 1-bit black and white images depending on the associated lookup table used. The circuitry on the panel includes an integrated gate and source driver, timing controller, oscillator, DC-DC boost circuit, and memory to store the frame buffer and lookup tables, and additional circuitry to control VCOM and border settings.

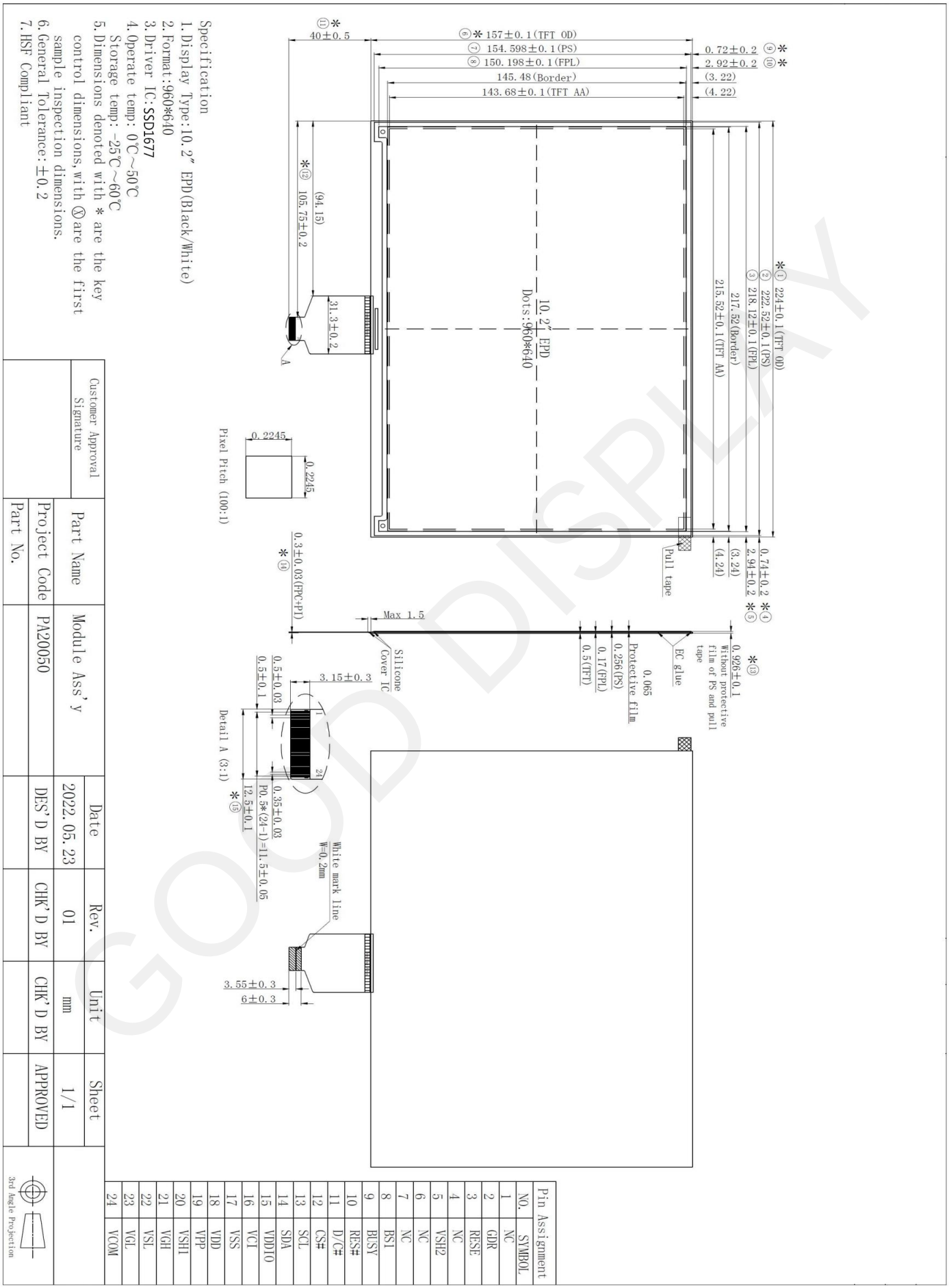
1.2 Features

- Ultra wide viewing angle
- Ultra low power consumption
- I2C Signal Master Interface to read external temperature sensor.
- On chip display RAM
- Interface:4-Wire SPI or 3-Wire SPI
- Wide range of operating temperature: 0℃to 50℃
- Wide range of storage temperature: -25℃ to 60℃
- High reflectance and contrast TFT electrophoretic.

1.3 Mechanical Specifications

NO.	ITEM	SPECIFICATION	UNIT
1	TFT Area	224(H)×157(V)	mm
2	Screen Size	10.2	Inch
3	Active Area	215.52(H) ×143.68(V)	mm
4	Pixel Pitch	0.2245×0.2245	mm
5	Pixels Per Inch	113	-
6	Outline Dimension	224 x 197 x 0.926	mm
7	Resolution	960(V) ×640(H)	-
8	Pixel Configuration	Square	-
9	Driver IC	SSD1677	-
10	Module Weight	63.3±10%	gram

1.4 Mechanical Drawing of EPD module



1.5 Module Interface

PIN NO.	PIN NAME	DESCRIPTION
1	NC	No Connection
2	GDR	This pin is N-Channel MOSFET gate drive control pin.
3	RESE	Current Sense Input for the control loop
4	NC	No Connection
5	VSH2	This pin is Positive Source driving voltage, VSH2 connect a stabilizing capacitor between VSH2 and VSS in the application circuit.
6	NC	No Connection
7	NC	No Connection
8	BS1	This pin is for selecting 3-wire(H active) or 4-wire(L active) SPI interface.
9	BUSY	This pin indicates the driver status. BUSY= ”0” : Driver is busy, data/VCOM is transforming. BUSY= ”1” : non-busy. Host side can send command/data to driver.
10	RES#	This pin is reset signal input (Active Low).
11	D/C#	This pin is Data/Command control pin connecting to the MCU
12	CS#	This pin is the chip select input connecting to the MCU.
13	SCL	This pin is serial clock pin for interface.
14	SDA	This pin is serial data pin for interface.
15	VDDIO	Power input pin for the Interface. Connect to VCI in the application circuit.
16	VCI	Power input pin for the chip.
17	VSS	Ground
18	VDD	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS under all circumstances
19	VPP	Power Supply for OTP Programming.
20	VSH1	This pin is Positive Source driving voltage, VSH1 Connect a stabilizing capacitor between VSH1 and VSS in the application circuit.
21	VGH	This pin is Positive Gate driving voltage. Connect a stabilizing capacitor between VGH and VSS in the application circuit.
22	VSL	This pin is Negative Source driving voltage. Connect a stabilizing capacitor between VSL and VSS in the application circuit.
23	VGL	This pin is Negative Gate driving voltage. Connect a stabilizing capacitor between VGL and VSS in the application circuit.
24	VCOM	This pins is VCOM driving voltage Connect a stabilizing capacitor between VCOM and VSS in the application circuit.

1.6 Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display and three-color (black, white and red/Yellow) Good Display 's E-paper Display. And it is also added the functions of USB serial port, Raspberry Pi and LED indicator light ect.

DESPI Development Kit consists of the development board and the pinboard. More details about the Development Kit, please click to the following link:

https://www.good-display.com/product/219.html

2. Environmental

2.1 HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged.

Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions	
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.	
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.	
(3) You should adopt radiation structure to satisfy the temperature specification.	
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.	
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)	
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.	
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.	
Product specification	The data sheet contains final product specifications.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and dose not form part of the specification.

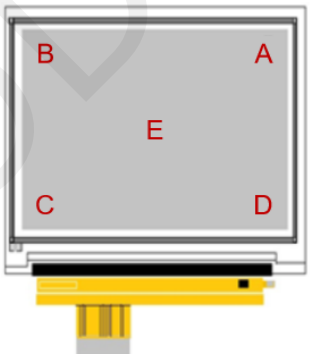
Product Environmental certification
ROHS

REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

2.2 Reliability test

NO	Test items	Test condition	QUANTITY
1	Low-Temperature Storage	T = -25℃ , low temperature film T= -30℃; White screen state, for 240h.	5pcs
2	Low-Temperature Operation	T = 0°C, 240 h; Put the product into the experimental procedure, run it in the temperature box, and check it every 24 hours.	5pcs
3	High-Temperature Operation	T = 50°C, RH = 35%, 240 h; Put the product into the experimental procedure, run it in the temperature box, and check it every 24 hours.	5pcs
4	High-Temperature Storage	T=60ºC，RH=35%; White screen state, for 240h.	5pcs
5	Temperature Cycle	1 cycle:[-25°C 30min]→[+60 °C 30 min]; 100 cycles.	5pcs
6	High-Temperature/ High- humidity Storage	T=60ºC，RH=90%; White screen state, for 240h.	5pcs
7	UV exposure Resistance	765W/m²for 168hrs,T = 50°C, RH=35%;	5pcs
8	ESD Contact discharge	±200V, Test 5 point; Each point discharge 10 times. Time interval is not less than 1 second.	5pcs

ESD test location



Test and measurement conditions

After the end of the experiment, the sample was taken out of the temperature chamber, and stood at room temperature for 1h, and then the sample was inspected for appearance, function and optical inspection.

Criteria for qualification (pass the test if all qualified) :

(1) The product can be normal refresh.

(2) There are no new point defects or line defects in the display screen.

(3) No discoloration, blurred handwriting and barcode can be read on the complex screen.

2.3 Outgoing Quality Control Specifications

2.3.1 Sampling Method

(1)GB/T2828.1, inspection level, normal inspection, single sample inspection

(2)AQL:Major 0.65; Minor 1.0

2.3.2 Inspection Conditions

The environmental conditions for test and measurement are performed as follows.

Temperature:23±3C

Humidity:55±15%R.H

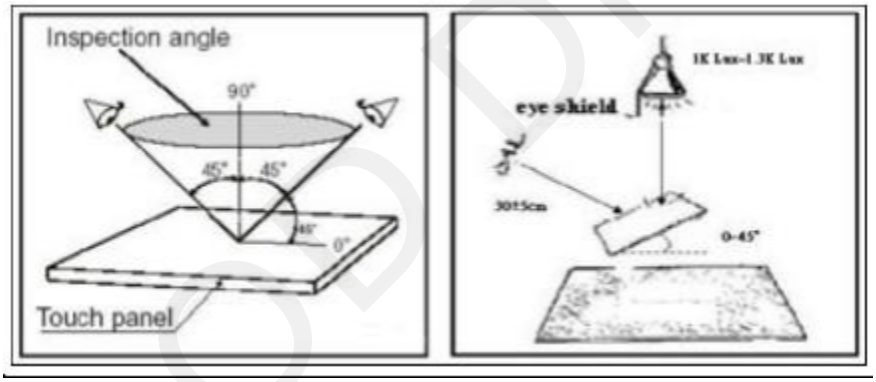
Inspection of illuminance:800~1200Lux

Inspection time:signal face 5S-10S

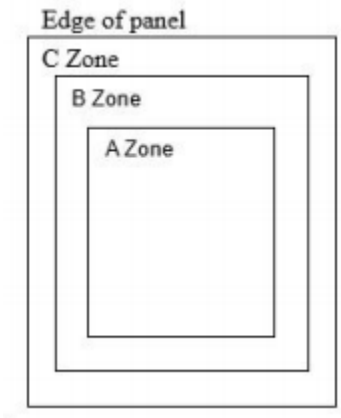
Distance between the Panel & Eyes:30±10cm

Viewing angle from the vertical in each direction:±45°

(See the sketch below)



2.3.3 Quality Assurance Zones



Zone A：Active Area

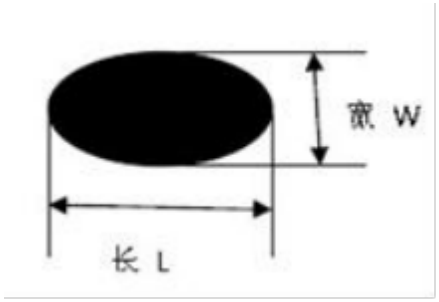
Zone B:Black Frame Area

Zone C:Outside Black Frame Area

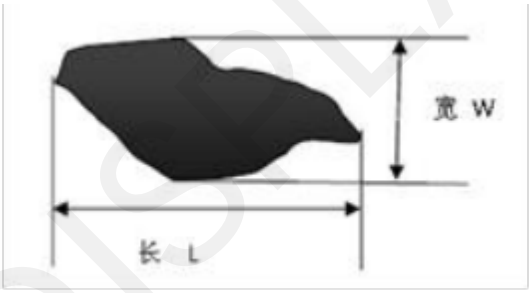
2.4 Inspection Standard

Defects Definition of Φ&L&W (Unit:mm)

2.4.1 Dot defects:

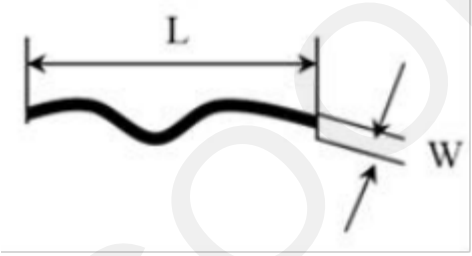


ÖD=Max(L,W)

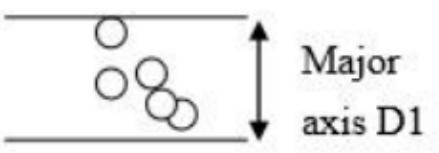


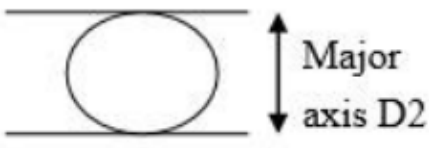
ÖD=Max(L,W)

2.4.2 Line defect:

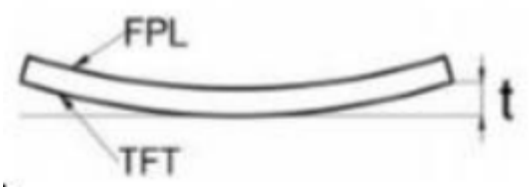


2.4.3 Small bubble aggregation and large bubble definition:



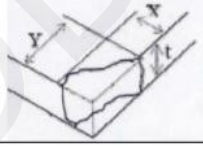


2.4.4 TFT warpage:



Appearance Defects

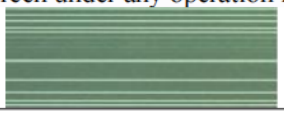
NO.	ITEM	CRITERIA	Acceptable range	Method	Defect level	Area
1	3.5inches below Dot defects (Black or White spot, Dirty spot, Foreign matter, Bubble)	D≦0.25mm	Ignore	Film Card	Minor	Zone A
		0.25mm < D≦0.4 mm, Distance≥5mm	N≦4			
		D>0.4 mm	N=0			
	3.5~7.5inches Dot defects (Black or White spot, Dirty spot, Foreign matter, Bubble)	D≦0.25mm	Ignore	Film Card	Minor	Zone A
		0.25mm < D≦0.4 mm, Distance≥5mm	N≦4			
		0.4mm < D≦0.5 mm, Distance≥5mm (Black and white module)	N≦1			
		D>0.4 mm, D>0.5 mm(Black and white module)	N=0			
	7.5inches above Dot defects (Black or White spot, Dirty spot, Foreign matter, Bubble)	D≦0.3mm	Ignore	Film Card	Minor	Zone A
		0.3mm < D≦0.5 mm, Distance≥5mm	N≦4			
		D>0.5 mm	N=0			
2	3.5inches below Line defect (Foreign material,Scratch)	L≦2mm, W≦0.2mm	Ignore	Film Card	Minor	Zone A
		2mm<L≦5mm, 0.2<W≦0.3mm	N≦2			
		L>5mm, W>0.3mm	N=0			

NO.	ITEM	CRITERIA	Acceptable range	Method	Defect level	Area
	3.5~7.5inches Line defects (Foreign material, Scratch)	L≦2mm, W≦0.2mm	Ignore	Film Card	Minor	Zone A
		2mm<L≦8mm, 0.2<W≦0.5mm	N≦2			
		L>8mm, W>0.5mm	N=0			
	7.5inches above Line defects (Foreign material, Scratch)	L≦2mm, W≦0.2mm	Ignore	Film Card	Minor	Zone A
		2mm<L≦8mm, 0.2<W≦0.5mm	N≦5			
		L>8mm, W>0.5mm	N=0			
3	Glass Crack	Extensional cracks are not allowed 	N=0	Sight Check	Major	Zone B,C
4	Edge breakage	X≤3mm,Y≤0.5mm, It does not affect the electrode 	N≦2	Sight Check/ Microscope	Minor	Zone C
5	Chip Package Chip Off	X≤2mm · Y≤2mm, It does not affect the electrode(FPC edge) X≤1mm · Y≤1mm, It does not affect the electrode((Not FPC edge) 	N≦2	Sight Check/ Microscope	Minor	Zone C
6	Squalidity	Can wipe dirt.	Ignore	Sight Check	Minor	Zone A,B
7	Silicone	The maximum diameter of a single bubble cannot exceed 2mm	N≤2	Sight Check/ Film card	Minor	Zone C
		Crack is not allowed and there are no visible impurities in the glue of the lead part (Determination of impurities outside IC region by point deficiency)	N=0			
		The adhesive must completely cover the ACF, lead area and IC and should be applied evenly	N=0			
		No glue leakage, no obvious lack of glue in the lead area	N=0			
		Glue height exceeds PS surface	N=0			

NO.	ITEM	CRITERIA	Acceptable range	Method	Defect level	Area
		FPC Front overflow glue width>0.5mm or Back side overflow glue width>1mm	N=0			
8	Edge Sealing Adhesive	No glue leakage	N=0	Sight Check/ Film card	Major	Zone C
		The height of sealant exceeds PS surface	N=0		Minor	
		Bubbles 0.2mm<D1,D2≦0.5mm	N=3		Minor	
9	Protective film	Foreign body in protective film	N=0	Sight Check	Minor	Zone A
		The protective film punctures and injures FPL	N=0			
10	Pull Tape	Attachment position is wrong Cannot tear up the protective film	N=0	Sight Check	Minor	Zone C
11	FPC	FPC has break, scratch, gold finger stripping or oxidation, dirty, residual glue	N=0	Sight Check	Major	Zone C
12	Glass edge bulge	X≤3mm · Y≤0.3mm	N≦1	Sight Check	Minor	Zone C
13	Warping	t > 1mm (3.5inch below) t > 1.5mm (3.5inch~7.5inch) t > 2mm (7.5inch above)	N=0	Plug Gage	Minor	Zone C
14	Chromatism	Color difference in silver paste area (Not in Zone A)	Ignore	Sight Check	Minor	Zone C
		FPL Peeling occurs, chromatic aberration occurs	N=0	Sight Check	Major	Zone A,B
15	Silver pulp point	FPL and TFT substrate conduction, silver point <1.0mm	N=0	Film card	Major	Zone C

Displaying Defects

NO.	ITEM	CRITERIA	Acceptable range	Method	Defect level	Area
1	3.5inches below Dot defects (Black or White spot）	D≦0.25mm	Ignore	Film Card	Major	Zone A
		0.25mm < D≦0.4 mm, Distance≥5mm	N≦4			
		D>0.4 mm	N=0			
	3.5~7.5inches Dot defects (Black or White spot）	D≦0.25mm	Ignore	Film Card	Major	Zone A
		0.25mm < D≦0.4 mm, Distance≥5mm	N≦4			
		0.4mm < D≦0.5 mm, Distance≥5mm (Black and white module)	N≦1			
		D>0.4 mm, D>0.5 mm(Black and white module)	N=0			
	7.5inches above Dot defects (Black or White spot）	D≦0.3mm	Ignore	Film Card	Major	Zone A
		0.3mm < D≦0.5 mm, Distance≥5mm	N≦4			
		D>0.5 mm	N=0			

NO.	ITEM	CRITERIA	Acceptable range	Method	Defect level	Area
2	Line defects	White or black lines running through the entire screen under any operation interface 	N=0	Sight Check	Major	Zone A
3	ghost	Ghosts appear only during screen switching	Ignore	Sight Check	Major	Zone A
4	Flash Point	Flash point occurs during screen switching only	Ignore	Sight Check	Major	Zone A
5	Display screen error	Unable to display a fixed screen correctly	N=0	Sight Check	Major	Zone A
6	Display abnormal	No display, The red matrix darkens, Note fuzzy, bar code can not be scanned, After refresh, the previous template remains	N=0	Sight Check	Major	Zone A

Identification and packaging inspection

NO.	ITEM	CRITERIA	Method	Defect level
1	Package	(1). The products are completely placed in the anti-static tray without overlapping. (2). Products with different models cannot be mixed in one internal packaging bag. (3) There is a desiccant in the packaging bag, with good internal packaging and no expansion of the packaging bag. (4) The Tray model, quantity and way used for packaging meet the requirements of product specifications.	Sight Check	Minor
2	Inner and outer packing	(1) No obvious deformation, damage, dampness or dirt on the packing case; (2) The type, quantity and method of the packing case used shall meet the requirements of the product specification. (3) There is no font or unclear design in the outer packing box.	Sight Check	Minor
3	Labels for inner and outer cases	(1). Any unnecessary marks or marks are not allowed to exist; (2). The label information such as model, specification, quantity, weight, material number, month label and environmental protection label should be clear and correct, which should be in line with product specifications or marked according to customer requirements.	Sight Check	Minor

3. ELECTRICAL CHARACTERISTICS

3.1 ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	MIN	MAX	UNIT	REMARK
Logic supply voltage	VCI	-0.5	+4.0	V	-
Logic Input voltage	V_{IN}	-0.5	VDDIO+0.5	V	-
Logic Output voltage	V_{OUT}	-0.3	VDDIO+0.5	V	-
Operating Temp.	Top	0	+50	℃	-
Storage Temp	Tstg	-25	+60	℃	-

Note(1):All of the voltages are on the basis of "VSS=0V".

Note(2):Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

3.2 DC Characteristics

The following specifications apply for: V_{SS}=0V, V_{CI}=3.3V, T_{OPR} =23ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Ma	Unit
Logic supply voltage	V_{CI}	-	V_{CI}	2.2	3.0	3.3	V
High level input voltage	V_{IH}	-	-	$0.8V_{VDDIO}$	-	-	V
Low level input voltage	V_{IL}	-		-	-	$0.2V_{VDDIO}$	V
High level output voltage	V_{OH}	IOH = -100uA	-	$0.9V_{VDDIO}$	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	$0.1V_{VDDIO}$	V
OTP Program voltage	V_{PP}	-	VPP	7.25	-	7.75	V
Typical power panel	P_{TYP}	-	-	-	40		mW
Standby power panel	P_{STPY}	-	-	-	TBD		mW
Typical operating current(Complex state)	Iopr_VCI	-	-	-	12	-	mA
Image update time	-	23 °C	-	-	5	-	sec
Sleep mode current	Islp_VCI	VCI=3.3V DC/DC OFF No clock No output load Ram data	VCI	-	40	70	uA
Deep sleep mode current	Idslp_VCI	VCI=3.3V DC/DC OFF No clock No output load Ram data not retain	VCI	-	2	6	uA

Note: The VPP, VCI, VDDIO input must be kept in a stable value; ripple and noise are not allowed.

3.3 Panel DC Characteristics (Driver IC Internal Regulators)

The following specifications apply for: V_{SS}=0V, V_{CI}=3.3V, T_{OPR} =23ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM	-	-2.0	-	V
Positive Source output voltage	V_{SH}	-	S_0~S_{959}	-	+15	-	V
Negative Source output voltage	V_{SL}	-	S_0~S_{959}	-	-15	-	V
Positive gate output voltage	Vgh	-	G_0~G_{639}	19.5	+20	20.5	V
Negative gate output voltage	Vgl	-	G_0~G_{639}	-	-20	-	V

3.4 Optical Specification

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	3-1
CR	Contrast Ratio	indoor	8:1	-	-		3-2
T update	Image update time	23 °C	-	5	-	sec	
Tlife	Life	Topr	-	1000000 times or 5years	-		

Notes 3-1: Luminance meter: Eye-One Pro Spectrophotometer.

Notes 3-2:CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

3.5 AC Electrical Characteristics

(1) Serial Peripheral Interface The following specifications apply for:

VDDIO – VSS = 2.2V to 3.7V, T_{OPR} = 23°C CL = 20pF

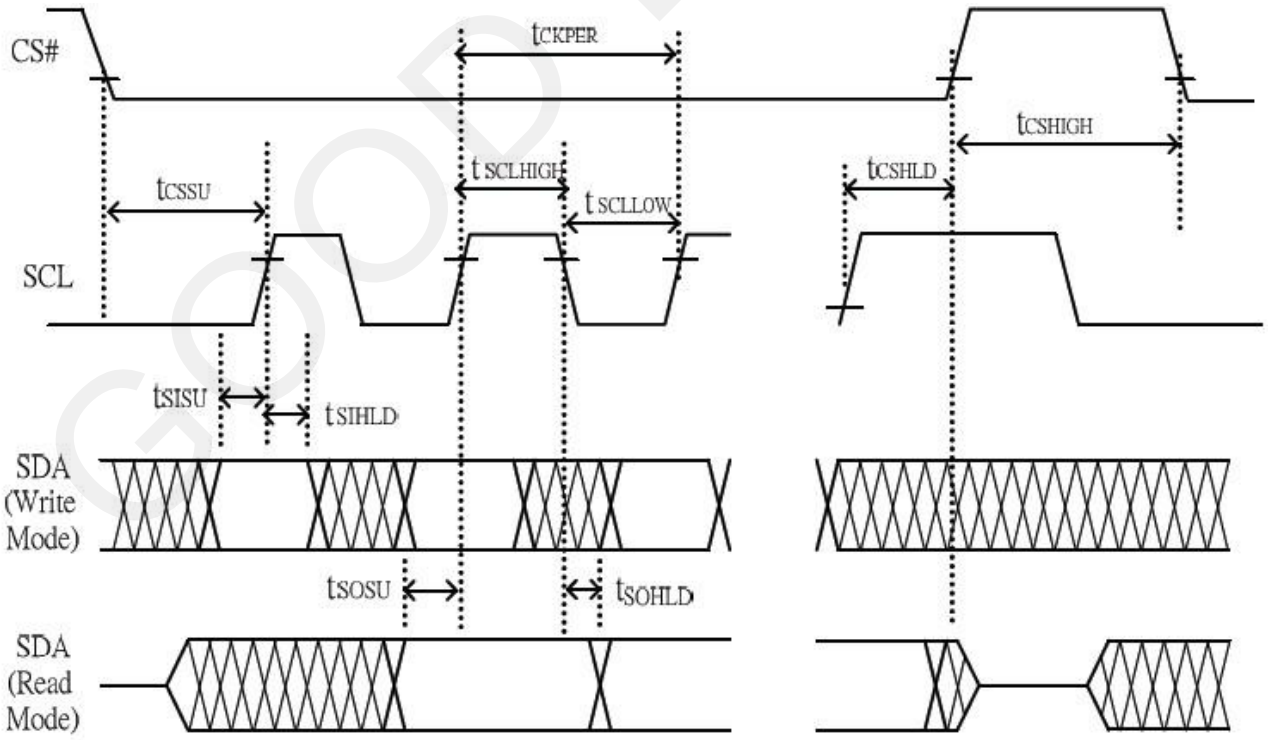
Write mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL frequency (Write Mode)			20	MHz
t_{CSSU}	Time CS# has to be low before the first rising edge of SCLK	60			ns
t_{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	65			ns
t_{CSHIGH}	Time CS# has to remain high between two transfers	100			ns
$t_{SCLHIGH}$	Part of the clock period where SCL has to remain high	25			ns
t_{SCLLOW}	Part of the clock period where SCL has to remain low	25			ns
t_{SISU}	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
t_{SIHLD}	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCL}	SCL frequency (Read Mode)			2.5	MHz
t_{CSSU}	Time CS# has to be low before the first rising edge of SCLK	100			ns
t_{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	50			ns
t_{CSHIGH}	Time CS# has to remain high between two transfers	250			ns
$t_{SCLHIGH}$	Part of the clock period where SCL has to remain high	180			ns
t_{SCLLOW}	Part of the clock period where SCL has to remain low	180			ns
t_{SOSU}	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
t_{SOHLD}	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

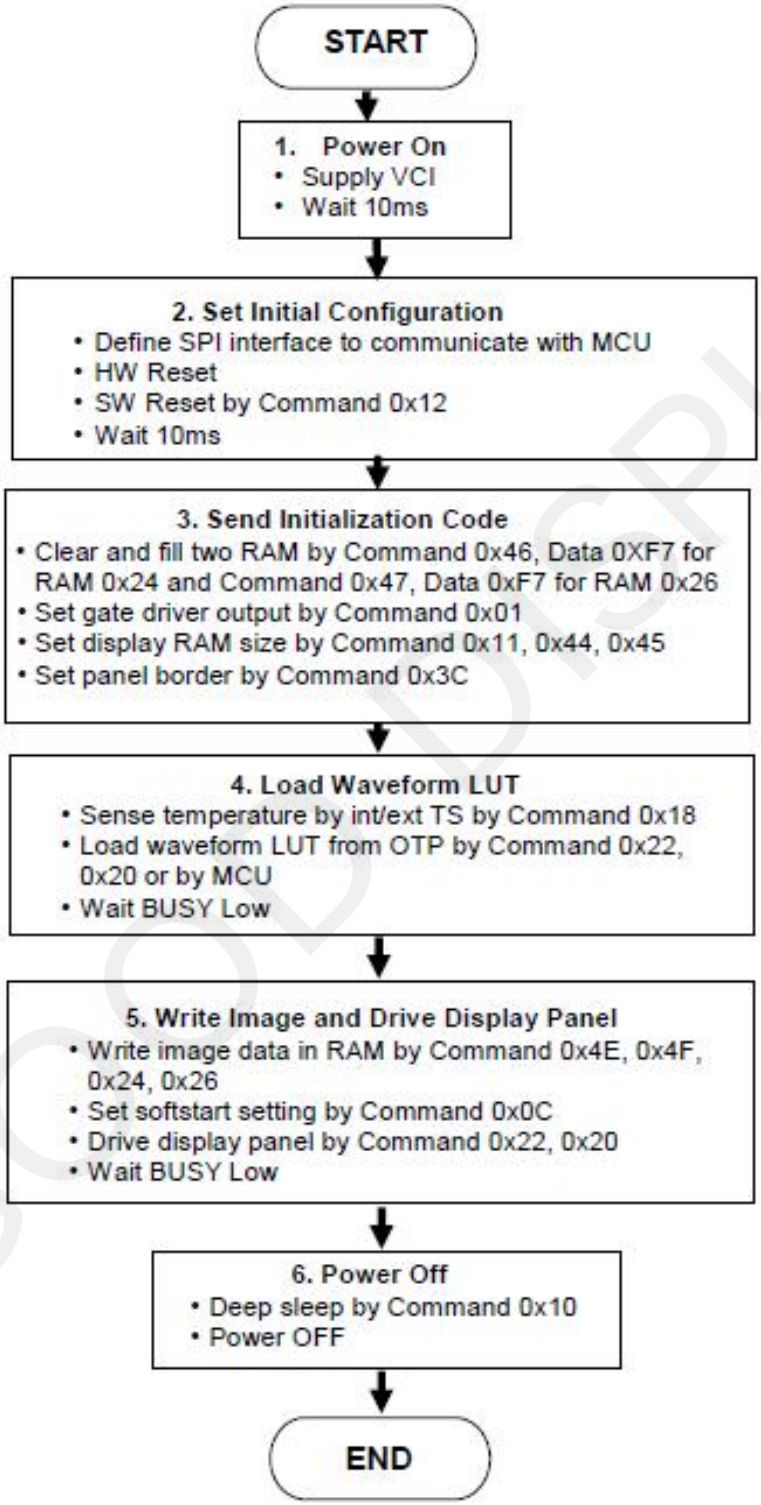
SPI timing diagram



3.6 Functional Specification and Application Circuit

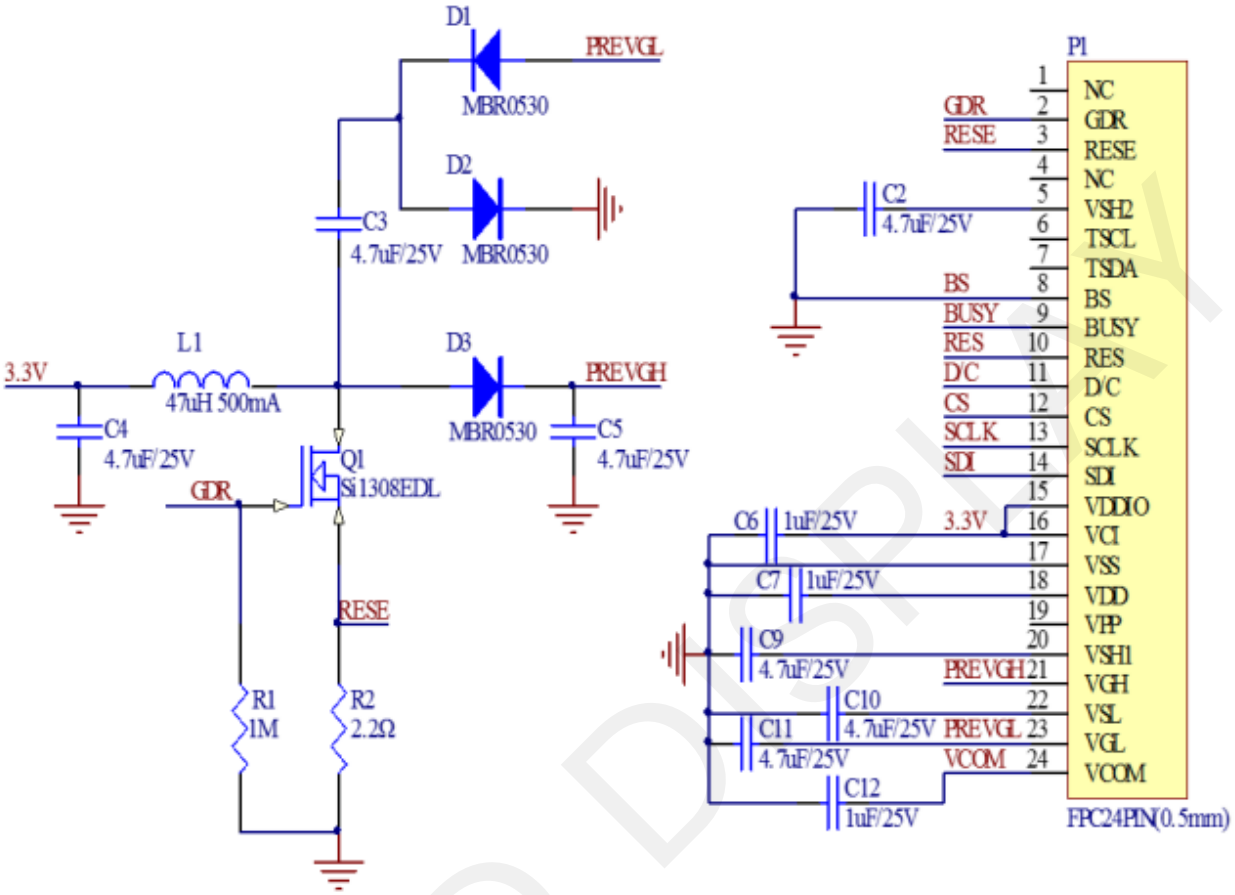
3.6.1 Operation Flow and Code Sequence

General operation flow to drive display panel



3.6.2 Typical Application Circuit with SPI Interface

(1) Schematic of application circuit:



3.7 Command Table

<table>
<tr><td colspan="12">Command Table</td></tr>
<tr><td>R/W#</td><td>D/C#</td><td>Hex</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Command</td><td>Description</td></tr>
<tr><td>0</td><td>0</td><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="4">Driver Output control</td><td rowspan="4">Gate setting
A[9:0]= 2A7h [POR], 680 MUX
MUX Gate lines setting as (A[9:0] + 1).

B[2:0] = 000 [POR].
Gate scanning sequence and direction

B[2]: GD
Selects the 1st output Gate
GD=0 [POR],
G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, …
GD=1,
G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, …

B[1]: SM
Change scanning order of gate driver.
SM=0 [POR],
G0, G1, G2, G3…679 (left and right gate interlaced)
SM=1,
G0, G2, G4 …G678, G1, G3, …G679

B[0]: TB
TB = 0 [POR], scan from G0 to G679
TB = 1, scan from G679 to G0.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A9</td><td>A8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td></td><td>0</td><td>0</td><td>0</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>03</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>Gate Driving voltage Control</td><td>Set Gate driving voltage
A[4:0] = 00h [POR]
VGH setting from 12V to 20V
<table>
<tr><th>A[4:0]</th><th>VGH</th><th>A[4:0]</th><th>VGH</th></tr>
<tr><td>00h</td><td>20</td><td>10h</td><td>16.5</td></tr>
<tr><td>07h</td><td>12</td><td>11h</td><td>17</td></tr>
<tr><td>08h</td><td>12.5</td><td>12h</td><td>17.5</td></tr>
<tr><td>09h</td><td>13</td><td>13h</td><td>18</td></tr>
<tr><td>0Ah</td><td>13.5</td><td>14h</td><td>18.5</td></tr>
<tr><td>0Bh</td><td>14</td><td>15h</td><td>19</td></tr>
<tr><td>0Ch</td><td>14.5</td><td>16h</td><td>19.5</td></tr>
<tr><td>0Dh</td><td>15</td><td>17h</td><td>20</td></tr>
<tr><td>0Eh</td><td>15.5</td><td>Other</td><td>NA</td></tr>
<tr><td>0Fh</td><td>16</td><td></td><td></td></tr>
</table></td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
</table>

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source driving voltage A[7:0] = 41h [POR], VSH1 at 15V B[7:0] = A8h [POR], VSH2 at 5V. C[7:0] = 32h [POR], VSL at -15V
0	1		A7	A6	A5	A4	A3	A2	A1	A2		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		C7	C6	C5	C4	C3	C2	C1	C0		

B[7] = 1,
VSH2 voltage setting from 2.4V to 8.8V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
8Eh	2.4	AFh	5.7
8Fh	2.5	B0h	5.8
90h	2.6	B1h	5.9
91h	2.7	B2h	6
92h	2.8	B3h	6.1
93h	2.9	B4h	6.2
94h	3	B5h	6.3
95h	3.1	B6h	6.4
96h	3.2	B7h	6.5
97h	3.3	B8h	6.6
98h	3.4	B9h	6.7
99h	3.5	BAh	6.8
9Ah	3.6	BBh	6.9
9Bh	3.7	BCh	7
9Ch	3.8	BDh	7.1
9Dh	3.9	BEh	7.2
9Eh	4	BFh	7.3
9Fh	4.1	C0h	7.4
A0h	4.2	C1h	7.5
A1h	4.3	C2h	7.6
A2h	4.4	C3h	7.7
A3h	4.5	C4h	7.8
A4h	4.6	C5h	7.9
A5h	4.7	C6h	8
A6h	4.8	C7h	8.1
A7h	4.9	C8h	8.2
A8h	5	C9h	8.3
A9h	5.1	CAh	8.4
AAh	5.2	CBh	8.5
ABh	5.3	CCh	8.6
ACh	5.4	CDh	8.7
ADh	5.5	CEh	8.8
AEh	5.6	Other	NA

A[7]/B[7] = 0,
VSH1/VSH2 voltage setting from 9V to 17V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
23h	9	3Ch	14
24h	9.2	3Dh	14.2
25h	9.4	3Eh	14.4
26h	9.6	3Fh	14.6
27h	9.8	40h	14.8
28h	10	41h	15
29h	10.2	42h	15.2
2Ah	10.4	43h	15.4
2Bh	10.6	44h	15.6
2Ch	10.8	45h	15.8
2Dh	11	46h	16
2Eh	11.2	47h	16.2
2Fh	11.4	48h	16.4
30h	11.6	49h	16.6
31h	11.8	4Ah	16.8
32h	12	4Bh	17
33h	12.2	Other	NA
34h	12.4		
35h	12.6		
36h	12.8		
37h	13		
38h	13.2		
39h	13.4		
3Ah	13.6		
3Bh	13.8		

C[7] = 0,
VSL setting from -9V to -17V

C[7:0]	VSL
1Ah	-9
1Ch	-9.5
1Eh	-10
20h	-10.5
22h	-11
24h	-11.5
26h	-12
28h	-12.5
2Ah	-13
2Ch	-13.5
2Eh	-14
30h	-14.5
32h	-15
34h	-15.5
36h	-16
38h	-16.5
3Ah	-17
Other	NA

Remark:
VSH1> VSH2

0	0	0F	0	0	0	0	1	1	1	1	Gate scan start position	Set the scanning start position of the gate driver. The valid range is from 0 to 679. A[9:0] = 000h [POR] When TB=0: SCN [9:0] = A[9:0] When TB=1: SCN [9:0] = 679 - A[9:0]
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	A9	A8		

<table>
<tr><td colspan="12">Command Table</td></tr>
<tr><td>R/W#</td><td>D/C#</td><td>Hex</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Command</td><td>Description</td></tr>
<tr><td>0</td><td>0</td><td>10</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td rowspan="2">Deep Sleep mode</td><td rowspan="2">Deep Sleep mode Control:
<table><tr><td>A[1:0] :</td><td>Description</td></tr><tr><td>00</td><td>Normal Mode [POR]</td></tr><tr><td>01</td><td>Enter Deep Sleep Mode 1</td></tr><tr><td>11</td><td>Enter Deep Sleep Mode 2</td></tr></table>After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high.
Remark:
To Exit Deep Sleep mode, User required to send HWRESET to the driver</td></tr>
<tr><td>0</td><td>0</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>11</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="2">Data Entry mode setting</td><td rowspan="2">Define data entry sequence
A[2:0] = 011 [POR]
A [1:0] = ID[1:0]
Address automatic increment / decrement setting
The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address.
00 –Y decrement, X decrement,
01 –Y decrement, X increment,
10 –Y increment, X decrement,
11 –Y increment, X increment [POR]
A[2] = AM
Set the direction in which the address counter is updated automatically after data are written to the RAM.
AM= 0, the address counter is updated in the X direction. [POR]
AM = 1, the address counter is updated in the Y direction.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>12</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>SW RESET</td><td>It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode
During operation, BUSY pad will output high.
Note: RAM are unaffected by this command.</td></tr>
</table>

<table>
<tr><td colspan="12">Command Table</td></tr>
<tr><td>R/W#</td><td>D/C#</td><td>Hex</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Command</td><td>Description</td></tr>
<tr><td>0</td><td>0</td><td>14</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>HV Ready Detection</td><td>HV ready detection
A[6:0] = 00h [POR]
The command required CLKEN=1 and ANALOGEN=1.
Refer to Register 0x22 for detail.
After this command initiated, HV Ready detection starts.
BUSY pad will output high during detection.
The detection result can be read from the Status Bit Read (Command 0x2F).</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>15</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td rowspan="2">VCI Detection</td><td rowspan="2">VCI Detection
A[2:0] = 100 [POR] , Detect level at 2.3V
A[2:0] : VCI level Detect
<table><tr><td>A[2:0]</td><td>VCI level</td></tr><tr><td>011</td><td>2.2V</td></tr><tr><td>100</td><td>2.3V</td></tr><tr><td>101</td><td>2.4V</td></tr><tr><td>110</td><td>2.5V</td></tr><tr><td>111</td><td>2.6V</td></tr><tr><td>Other</td><td>NA</td></tr></table>The command required CLKEN=1 and ANALOGEN=1
Refer to Register 0x22 for detail.
After this command initiated, VCI detection starts.
BUSY pad will output high during detection.
The detection result can be read from the Status Bit Read (Command 0x2F).</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>18</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td rowspan="2">Temperature Sensor Control</td><td rowspan="2">Temperature Sensor Selection
A[7:0] = 48h [POR], external temperatrure sensor
A[7:0] = 80h Internal temperature sensor</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>1A</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="3">Temperature Sensor Control (Write to temperature register)</td><td rowspan="3">Write to temperature register.
A[11:0] = 7FFh[POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A11</td><td>A10</td><td>A9</td><td>A8</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>1B</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="3">Temperature Sensor Control (Read from temperature register)</td><td rowspan="3">Read from temperature register.</td></tr>
<tr><td>1</td><td>1</td><td></td><td>A11</td><td>A10</td><td>A9</td><td>A8</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td></tr>
<tr><td>1</td><td>1</td><td></td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>

<table>
<tr><td colspan="12">Command Table</td></tr>
<tr><td>R/W#</td><td>D/C#</td><td>Hex</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Command</td><td>Description</td></tr>
<tr><td>0</td><td>0</td><td>1C</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td rowspan="4">Temperature Sensor Control (Write Command to External temperature sensor)</td><td rowspan="4">Write Command to External temperature sensor.
A[7:0] = 00h [POR],
B[7:0] = 00h [POR],
C[7:0] = 00h [POR],
A[7:6]
<table><tr><td>A[7:6]</td><td>Select no of byte to be sent</td></tr><tr><td>00</td><td>Address + pointer</td></tr><tr><td>01</td><td>Address + pointer + 1st arameter</td></tr><tr><td>10</td><td>Address + pointer + 1st parameter +2nd pointer</td></tr><tr><td>11</td><td>Address</td></tr></table>A[5:0] – Pointer Setting
B[7:0] – 1st parameter
C[7:0] – 2nd parameter
The command required CLKEN=1.
Refer to Register 0x22 for detail.
After this command initiated, Write Command to external temperature sensor starts. BUSY pad will output high during operation.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>C7</td><td>C6</td><td>C5</td><td>C4</td><td>C3</td><td>C2</td><td>C1</td><td>C0</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>20</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Master Activation</td><td>Activate Display Update Sequence
The Display Update Sequence Option is located at R22h.
BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.</td></tr>
<tr><td colspan="13"></td></tr>
<tr><td>0</td><td>0</td><td>21</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="2">Display Update Control 1</td><td rowspan="2">RAM content option for Display Update
A[7:0] = 00h [POR]
A[7:4] Red RAM option
<table><tr><td>0000</td><td>Normal</td></tr><tr><td>0100</td><td>Bypass RAM content as 0</td></tr><tr><td>1000</td><td>Inverse RAM content</td></tr></table>A[3:0] BW RAM option
<table><tr><td>0000</td><td>Normal</td></tr><tr><td>0100</td><td>Bypass RAM content as 0</td></tr><tr><td>1000</td><td>Inverse RAM content</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Display Update Control 2</td><td rowspan="2">Display Update Sequence Option:
Enable the stage for Master Activation
A[7:0]= FFh (POR)
<table><tr><td></td><td>Parameter (in Hex)</td></tr><tr><td>Enable Clock Signal,
Then Enable ANALOG
Then DISPLAY with DISPLAY Mode 1
Then Disable ANALOG
Then Disable OSC</td><td>C7</td></tr><tr><td>Enable Clock Signal,
Then Enable ANALOG
Then DISPLAY with DISPLAY Mode 2
Then Disable ANALOG
Then Disable OSC</td><td>CF</td></tr><tr><td colspan="2"></td></tr><tr><td>Enable Clock Signal,
Then Load LUT with DISPLAY Mode 1</td><td>90</td></tr><tr><td>Enable Clock Signal,
Then Load Temperature value from I2C
Single Master Interface
Then Load LUT with DISPLAY Mode 1</td><td>B0</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
</table>

Enable Clock Signal, Then Load LUT with DISPLAY Mode 2	98
Enable Clock Signal, Then Load Temperature value from I2C Single Master Interface Then Load LUT with DISPLAY Mode 2	B8
Enable Clock Signal, Then Load LUT with DISPLAY Mode 1 To Disable Clock Signal	91
Enable Clock Signal, Then Load Temperature value from I2C Single Master Interface Then Load LUT with DISPLAY Mode 1 To Disable Clock Signal	B1
Enable Clock Signal, Then Load LUT with DISPLAY Mode 2 To Disable Clock Signal	99
Enable Clock Signal, Then Load Temperature value from I2C Single Master Interface Then Load LUT with DISPLAY Mode 2 To Disable Clock Signal	B9
Enable ANALOG Then DISPLAY with DISPLAY Mode 1 Then Disable ANALOG Then Disable OSC	47
Enable ANALOG Then DISPLAY with DISPLAY Mode 2 Then Disable ANALOG Then Disable OSC	4F
To Enable Clock Signal (CLKEN=1)	80
To Enable Clock Signal, then Enable ANALOG (CLKEN=1, ANALOGEN=1)	C0
Enable ANALOG Then DISPLAY with DISPLAY Mode 1	44
Enable ANALOG Then DISPLAY with DISPLAY Mode 2	4C
To DISPLAY with DISPLAY Mode 1	04
To DISPLAY with DISPLAY Mode 2	0C
To Disable ANALOG, then Disable Clock Signal (CLKEN=0, ANALOGEN=0)	03
o Disable Clock Signal (CLKEN=0)	01

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	24	0	0	1	0	0	1	0	0	Write RAM (BW)	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly For Write pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED)	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0
0	0	27	0	0	1	0	0	1	1	1	Read RAM	After this command, data read on the MCU bus will fetch data from RAM [According to parameter of Register 41h to select reading RAM(BW) / RAM(RED)], until another command is written. Address pointers will advance accordingly. The 1st byte of data read is dummy data.
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. A[6]=1, Normal Mode A[6]=0, Reserve A[3:0] = 09h, duration = 10s. VCOM sense duration = Setting + 1 Seconds
0	1		0	A6	0	0	A3	A2	A1	A0		
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2B	0	0	1	0	1	0	1	1	Write Register for VCOM Control	This command is used to reduce glitch when ACVCOM toggle. Two data bytes D04h and D63h should be set for this command.
0	1		0	0	0	0	0	1	0	0		
0	1		0	1	1	0	0	0	1	1		
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Write VCOM register from MCU interface A[7:0] = 00h [POR]
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read forDisplay Option	Read Register for Display Option: A[7:0]: VCOM OTP Selection (Command 0x37, Byte A) B[7:0]: VCOM Register (Command 0x2C) C[7:0]~G[7:0]: Display Mode (Command 0x37, Byte B to Byte G) [5 bytes] H[7:0]~K[7:0]: Waveform Version (Command 0x37, Byte H to Byte K) [4 bytes]
1	1		A7	A6	A5	A4	A3	A2	A1	A0		
1	1		B7	B6	B5	B4	B3	B2	B1	B0		
1	1		C7	C6	C5	C4	C3	C2	C1	C0		
1	1		D7	D6	D5	D4	D3	D2	D1	D0		
1	1		E7	E6	E5	E4	E3	E2	E1	E0		
1	1		F7	F6	F5	F4	F3	F2	F1	F0		
1	1		G7	G6	G5	G4	G3	G2	G1	G0		
1	1		H7	H6	H5	H4	H3	H2	H1	H0		
1	1		I7	I6	I5	I4	I3	I2	I1	I0		
1	1		J7	J6	J5	J4	J3	J2	J1	J0		
1	1		K7	K6	K5	K4	K3	K2	K1	K0		

A[7:0]	VCOM	A[7:0]	VCOM
08h	-0.2	58h	-2.2
0Ch	-0.3	5Ch	-2.3
10h	-0.4	60h	-2.4
14h	-0.5	64h	-2.5
18h	-0.6	68h	-2.6
1Ch	-0.7	6Ch	-2.7
20h	-0.8	70h	-2.8
24h	-0.9	74h	-2.9
28h	-1	78h	-3
2Ch	-1.1	7Ch	-3.1
30h	-1.2	80h	-3.2
34h	-1.3	84	-3.3
38h	-1.4	88	-3.4
3Ch	-1.5	8C	-3.5
40h	-1.6	90	-3.6
44h	-1.7	94	-3.7
48h	-1.8	98	-3.8
4Ch	-1.9	9C	-3.9
50h	-2	A0	-4
54h	-2.1		

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	34	0	0	1	1	0	1	0	0	CRC calculation	CRC calculation command for OTP content validation. BUSY pad will output high during operation.
0	0	35	0	0	1	1	0	1	0	1	CRC Status Read	CRC Status Read A[15:0] is the CRC readout Value
1	1		A15	A14	A13	A12	A11	A10	A9	A8		
1	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R37h and R38h] The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	37	0	0	1	1	0	1	1	1	Write Register for Display Option	Write Register for Display Option B[7:0] Display Mode for WS[7:0] C[7:0] Display Mode for WS[15:8] D[7:0] Display Mode for WS[23:16] E[7:0] Display Mode for WS[31:24] F[3:0] Display Mode for WS[35:32] 0: Display Mode 1 1: Display Mode2 F[6]: PingPong for Display Mode 2 F[7]: PingPong for Display Mode 1 1: Ping-Pong 0: Default G[7:0]~J[7:0] module ID /waveform version. Remarks: A[7:0]~J[7:0] can be stored in OTP
0	1		0	0	0	0	0	0	0	0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		C7	C6	C5	C4	C3	C2	C1	C0		
0	1		D7	D6	D5	D4	D3	D2	D1	D0		
0	1		E7	E6	E5	E4	E3	E2	E1	E0		
0	1		F7	F6	F5	F4	F3	F2	F1	F0		
0	1		G7	G6	G5	G4	G3	G2	G1	G0		
0	1		H7	H6	H5	H4	H3	H2	H1	H0		
0	1		I7	I6	I5	I4	I3	I2	I1	I0		
0	1		J7	J6	J5	J4	J3	J2	J1	J0		
0	0	38	0	0	1	1	1	0	0	0	Write Register for User ID	Write Register for User ID A[7:0]]~J[7:0]: UserID [10 bytes] Remarks: A[7:0]~J[7:0] can be stored in OTP
0	1	A7	A6	A5	A4	A3	A2	A1	A0	A7		
0	1	B7	B6	B5	B4	B3	B2	B1	B0	B7		
0	1	C7	C6	C5	C4	C3	C2	C1	C0	C7		
0	1	D7	D6	D5	D4	D3	D2	D1	D0	D7		
0	1	E7	E6	E5	E4	E3	E2	E1	E0	E7		
0	1	F7	F6	F5	F4	F3	F2	F1	F0	F7		
0	1	G7	G6	G5	G4	G3	G2	G1	G0	G7		
0	1	H7	H6	H5	H4	H3	H2	H1	H0	H7		
0	1	I7	I6	I5	I4	I3	I2	I1	I0	I7		
0	1	J7	J6	J5	J4	J3	J2	J1	J0	J7		

<table>
<tr><td colspan="12">Command Table</td></tr>
<tr><td>R/W#</td><td>D/C#</td><td>Hex</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Command</td><td>Description</td></tr>
<tr><td>0</td><td>0</td><td>39</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td rowspan="2">OTP program mode</td><td rowspan="2">OTP program mode
A[1:0] = 00: Normal Mode [POR]
A[1:0] = 11: Internal generated OTP programming voltage
Remark: User is required to EXACTLY follow the reference code sequences</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A1</td><td>A0</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>3A</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>3B</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>3C</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td rowspan="2">Border Waveform Control</td><td rowspan="2">Select border waveform for VBD
A[7:0] = C0h [POR], set VBD as HIZ.
A [7:6] :Select VBD option
<table>
<tr><td>A[7:6]</td><td>Select VBD as</td></tr>
<tr><td>00</td><td>GS Transition,
Defined in A[1:0]</td></tr>
<tr><td>01</td><td>Fix Level,
Defined in A[5:4]</td></tr>
<tr><td>10</td><td>VCOM</td></tr>
<tr><td>11[POR]</td><td>HiZ</td></tr>
</table>
A [5:4] Fix Level Setting for VBD
<table>
<tr><td>A[5:4]</td><td>VBD level</td></tr>
<tr><td>00[POR]</td><td>VSS</td></tr>
<tr><td>01</td><td>VSH1</td></tr>
<tr><td>10</td><td>VSL</td></tr>
<tr><td>11</td><td>VSH2</td></tr>
</table>
A [1:0] GS Transition setting for VBD
<table>
<tr><td>A[1:0]</td><td>VBD Transition</td></tr>
<tr><td>00[POR]</td><td>LUT0</td></tr>
<tr><td>01</td><td>LUT1</td></tr>
<tr><td>10</td><td>LUT2</td></tr>
<tr><td>11</td><td>LUT3</td></tr>
</table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>41</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="2">Read RAM Option</td><td rowspan="2">Read RAM Option
A[0]= 0 [POR]
0: Read RAM corresponding to 24h
1: Read RAM corresponding to 26h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A0</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>44</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td rowspan="5">Set RAM X - address Start / End position</td><td rowspan="5">Specify the start/end positions of the window address in the X direction by an address unit for RAM
A[9:0]: XSA[9:0], XStart, POR = 000h
B[5:0]: XEA[9:0], XEnd, POR = 3BFh</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>A9</td><td>A8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>B9</td><td>B8</td></tr>
</table>

<table>
<tr><td colspan="12">Command Table</td></tr>
<tr><td>R/W#</td><td>D/C#</td><td>Hex</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>Command</td><td>Description</td></tr>
<tr><td>0</td><td>0</td><td>45</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td rowspan="5">Set RAM Y-address Start / End position</td><td rowspan="5">Specify the start/end positions of the window address in the Y direction by an address unit for RAM
A[8:0]: YSA[8:0], YStart, POR = 000h
B[8:0]: YEA[8:0], YEnd, POR = 2A7h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>A9</td><td>A8</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>B9</td><td>B8</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>46</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td rowspan="2">Auto Write RED RAM for Regular Pattern</td><td rowspan="2">Auto Write RED RAM for Regular Pattern
A[7:0] = 00h [POR]
A[7]: The 1st step value, POR = 0
A[6:4]: Step Height, POR= 000
Step of alter RAM in Y-direction according to Gate
<table><tr><td>A[6:4]</td><td>Height</td><td>A[6:4]</td><td>Height</td></tr><tr><td>000</td><td>8</td><td>100</td><td>128</td></tr><tr><td>001</td><td>16</td><td>101</td><td>256</td></tr><tr><td>010</td><td>32</td><td>110</td><td>512</td></tr><tr><td>011</td><td>64</td><td>111</td><td>960</td></tr></table>A[2:0]: Step Width, POR= 000
Step of alter RAM in X-direction according to Source
<table><tr><td>A[2:0]</td><td>Width</td><td>A[2:0]</td><td>Width</td></tr><tr><td>000</td><td>8</td><td>100</td><td>128</td></tr><tr><td>001</td><td>16</td><td>101</td><td>256</td></tr><tr><td>010</td><td>32</td><td>110</td><td>512</td></tr><tr><td>011</td><td>64</td><td>111</td><td>680</td></tr></table>BUSY pad will output high during operation.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td colspan="12"></td></tr>
<tr><td>0</td><td>0</td><td>47</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td rowspan="2">Auto Write B/W RAM for Regular Pattern</td><td rowspan="2">Auto Write B/W RAM for Regular Pattern
A[7:0] = 00h [POR]
Auto Write B/W RAM for Regular Pattern
A[7:0] = 00h [POR]
<table><tr><td>A[6:4]</td><td>Height</td><td>A[6:4]</td><td>Height</td></tr><tr><td>000</td><td>8</td><td>100</td><td>128</td></tr><tr><td>001</td><td>16</td><td>101</td><td>256</td></tr><tr><td>010</td><td>32</td><td>110</td><td>512</td></tr><tr><td>011</td><td>64</td><td>111</td><td>960</td></tr></table>A[2:0]: Step Width, POR= 000
Step of alter RAM in X-direction according to Source
<table><tr><td>A[2:0]</td><td>Width</td><td>A[2:0]</td><td>Width</td></tr><tr><td>000</td><td>8</td><td>100</td><td>128</td></tr><tr><td>001</td><td>16</td><td>101</td><td>256</td></tr><tr><td>010</td><td>32</td><td>110</td><td>512</td></tr><tr><td>011</td><td>64</td><td>111</td><td>680</td></tr></table>uring operation, BUSY pad will output high.</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
</table>

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[9:0]: 000h [POR].
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	A9	A8		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[9:0]: 000h [POR].
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	A9	A8		
0	0	7F	0	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However, it can be used to terminate Frame Memory Write or Read Commands.

3.8 MCU Interface

3.8.1 MCU interface selection

GDEQ102T90 can support 4-wire or 3-wire serial peripheral MCU interface, which is pin selectable by BS1 pin. The interface pin assignment for different MCU interfaces is shown in Table 3.8-1.

Note

(1) L is connected to VSS

(2) H is connected to VDDIO

Table 3.8-1: Interface pin assignment for different MCU interfaces

	Pin Name						
MCU Interface	**BS1**	**RES#**	**CS#**	**D/C#**	**SCL**	**SDI**	**SDO**
4-wire serial peripheral interface (SPI)	L	Required	Required	Required	SCL	SDI	SDO
3-wire serial peripheral interface (SPI) – 9 bits SPI	H	Required	Required	L	SCL	SDI	SDO

3.8.2 MCU Serial Peripheral Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data input SDI, D/C# and CS#. The control pins status in 4-wire SPI in writing command/data is shown in Table 3.8-2 and the write procedure in 4-wire SPI is shown in Figure 3.8-1..

Table 3.8-2 : Control pins status of 4-wire SPI

Function	SCL pin	SDI pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Note:

(1) L is connected to VSS and H is connected to VDDIO

(2) ↑ stands for rising edge of signal

(3) SDI is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

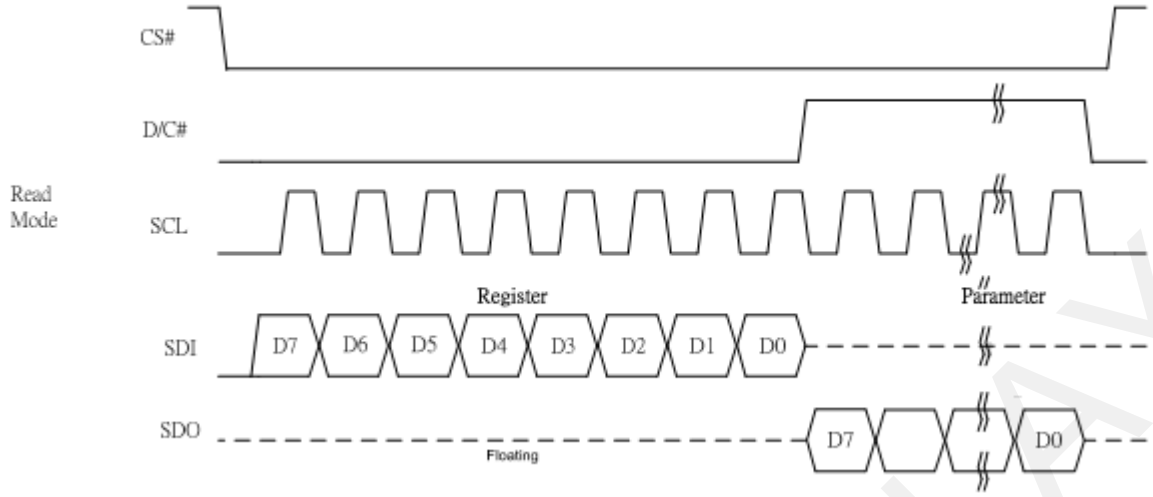


Figure 3.8-1: Read procedure in 4-wire SPI mode

In the read operation, after CS# is pulled low, the first byte sent is command byte, D/C# is pulled low. After command byte sent, the following byte(s) read are data byte(s), so D/C# bit is then pulled high. An 8-bit data will be shifted out on every clock falling edge. The serial data output SDO bit shifting sequence is D7, D6, to D0 bit. Figure 6-2 shows the read procedure in 4-wire SPI.

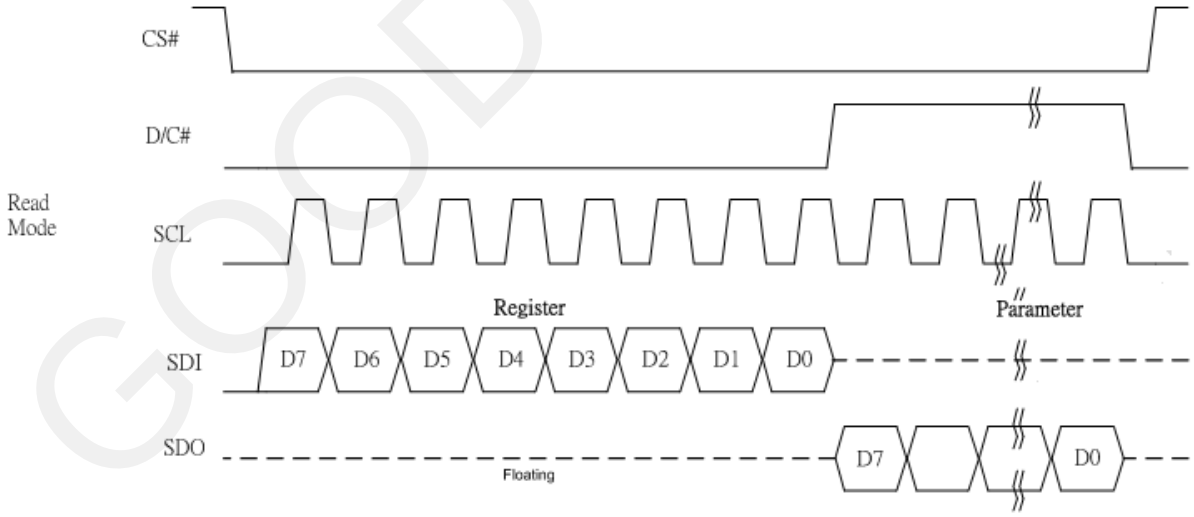


Figure 3.8-2: Read procedure in 4-wire SPI mode

3.8.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data input SDI, and CS#. The operation is similar to 4- wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 7-3.
In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Table 3.8 -3 shows the write procedure in 3-wire SPI

Table 3.8-3 : Control pins status of 3-wire SPI

Function	SCL pin	SDI pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:
(1) L is connected to VSS and H is connected to VDDIO
(2) ↑ stands for rising edge of signal

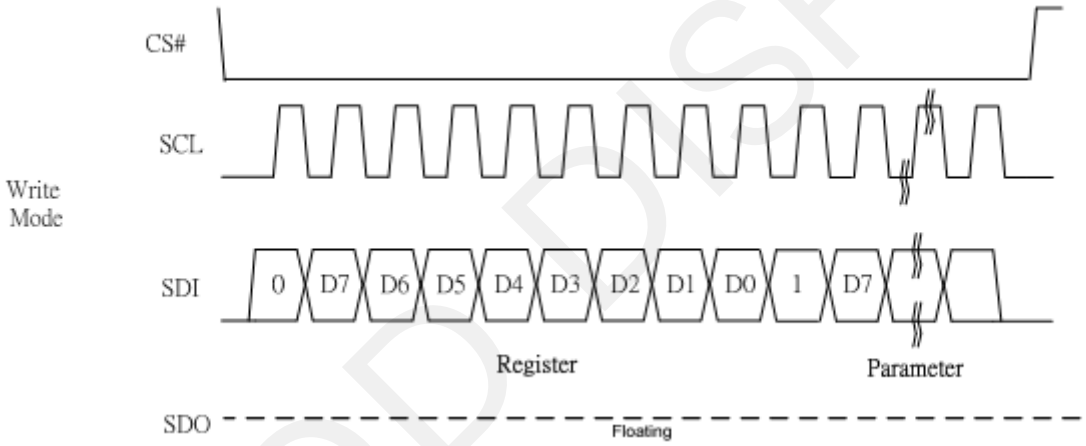


Figure 3.8-3: Write procedure in 3-wire SPI mode

In the read operation, serial data are transferred in the unit of 9 bits. After CS# pull low, the first byte is command byte, the D/C# bit is as 0 and following with the register byte. After command byte send, the following byte(s) are data byte(s), with D/C# bit is 1. After D/C# bit sending from MCU, an 8-bit data will be shifted out on every clock falling edge. The serial data output SDO bit shifting sequence is D7, D6, to D0 bit. Figure 3.8-4 shows the read procedure in 3-wire SPI.

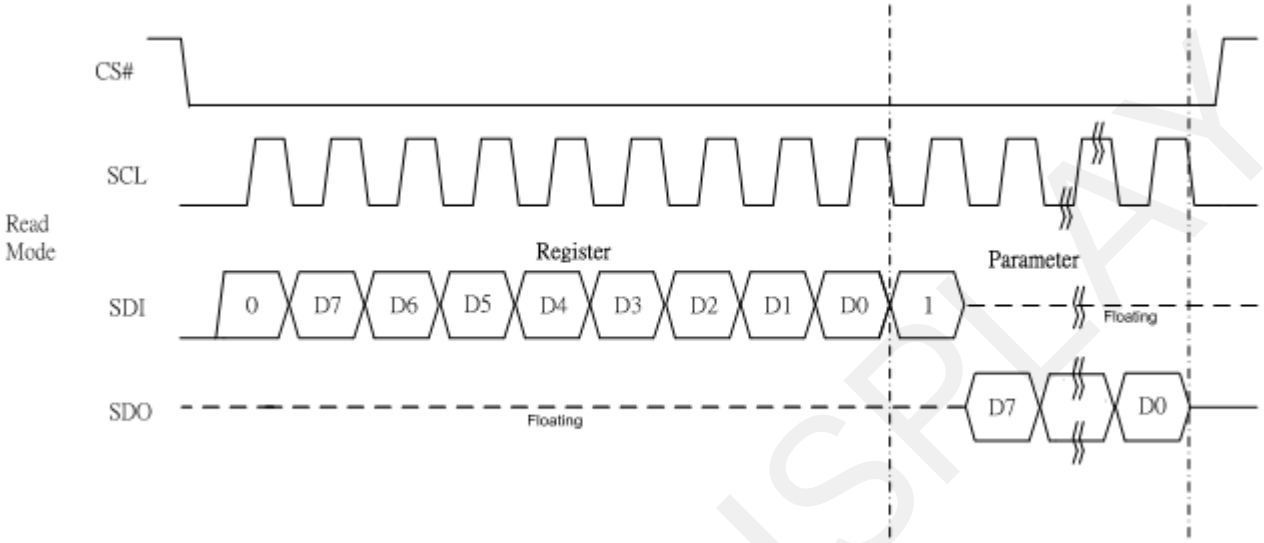


Figure 3.8-4: Read procedure in 3-wire SPI mode

4. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL /EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent li ght may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.

(7) For more precautions, please click on the link:
https://www.good-display.com/news/80.html