31.2 inch
E-paper Display Series

GooDisplay®

GDEP312TT2-C

Dalian Good Display Co., Ltd.

Product Specifications

Customer	**Standard**
Description	**31.2” E-PAPER DISPLAY**
Model Name	**GDEP312TT2-C**
Date	**2021/08/09**
Revision	**0.1**

	Design Engineering		
	Approval	**Check**	**Design**
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Revision History

Rev.	Issued Date	Revised Contents
0.1	2021-08-09	Preliminary

CONTENTS

1. General Description

GDEP312TT2-C is a reflective electrophoretic E Ink® technology display module based on TFT active matrix with color filter design. It has 31.2” active area with 1280*720 pixels, the display is capable to display 4096 colors depending on the display controller and the associated waveform file it used.

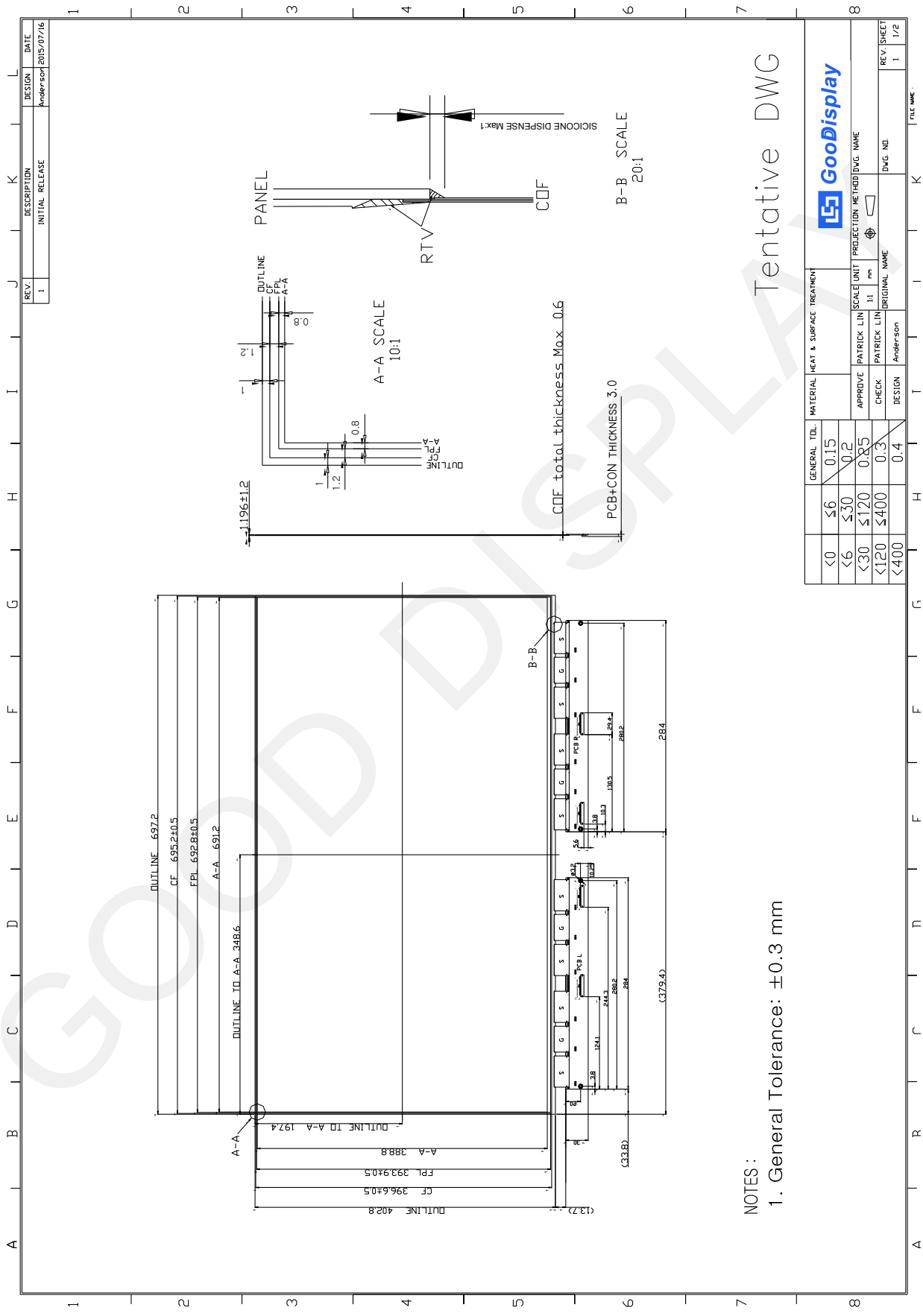
2. Features

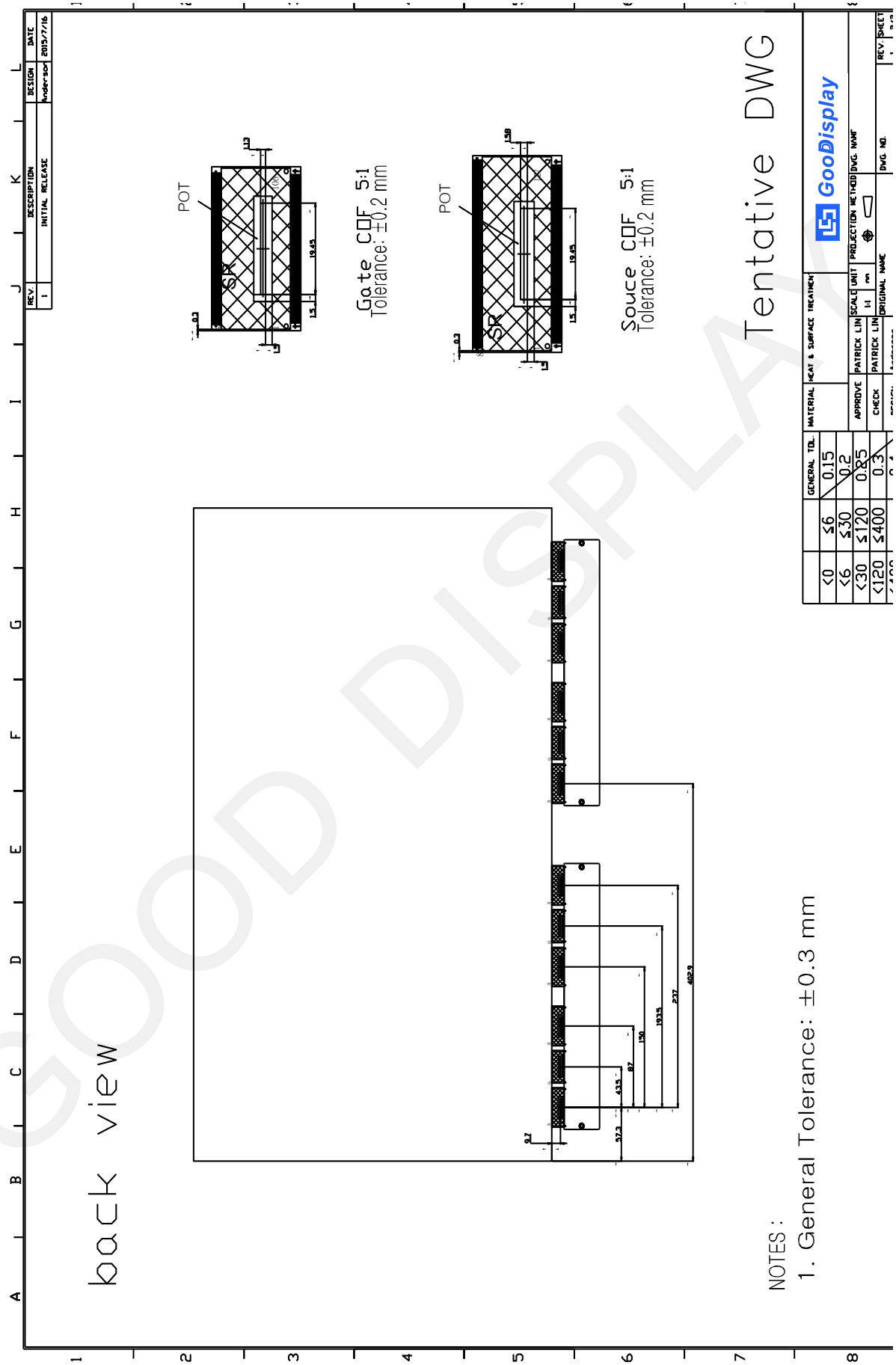
- High contrast reflective/electrophoretic technology
- 1280 x 720 display
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	31.2	Inch	
Display Resolution	1280 (H) × 720 (V)	Pixel	
Display colors	4096		
Active Area	691.2 (H) × 388.8 (V)	mm	
Outline Dimension	697.2(H) × 402.8(V) × 1.35(D)	mm	
Pixel Pitch	0.54 (H) × 0.54 (V)	mm	
Pixel Configuration	Square	mm	
Module Weight	800	g	
Number of Gray	16 Gray Level	mm	
Glass Substrate	0.5	mm	
Surface Treatment	Hard Coating		
FPL	E Ink Triton Ⓡ		

4. Mechanical Drawing of EPD Module





5. Input/Output Interface

5-1)Connector type：196033-50041

Pin Assignment

1) FPC L2

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	NO Connection
3	VGH	Positive power supply gate driver
4	Mode2	Output mode selection gate driver
5	VDD	Digital power supply drivers
6	Mode1	Output mode selection gate driver
7	CKV	Clock gate driver
8	STV	Start pulse gate driver
9	VSS	Ground
10	VCOM_TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL	Clock source driver
14	D0	Data signal source driver
15	D1	Data signal source driver
16	D2	Data signal source driver
17	D3	Data signal source driver
18	D4	Data signal source driver
19	D5	Data signal source driver
20	D6	Data signal source driver
21	D7	Data signal source driver
22	VSS	Ground
23	D8	Data signal source driver
24	D9	Data signal source driver
25	D10	Data signal source driver
26	D11	Data signal source driver
27	D12	Data signal source driver
28	D13	Data signal source driver
29	D14	Data signal source driver
30	D15	Data signal source driver
31	XSTL	Start pulse source driver
32	XLE	Latch enable source driver
33	XOE	Output enable source driver
34	ISEL	L: input data bus width is 8-bit, i.e., D7 ~ D0 are valid
35	NC	NO Connection
36	VPOS	Positive power supply source driver
37	NC	NO Connection
38	VNEG	Negative power supply source driver
39	VCOM_FPL	Common Voltage
40	NC	NO Connection
41	STV2	Start pulse gate driver
42	G640	Detect IC function
43	S400	Detect IC function
44	S320	Detect IC function
45	NC	NO Connection
46	G640	Detect IC function
47	S400	Detect IC function
48	S320	Detect IC function
49	NC	NO Connection
50	STL2	Data shift start pulse 2

2) FPC L1

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	NO Connection
3	VGH	Positive power supply gate driver
4	Mode2	Output mode selection gate driver
5	VDD	Digital power supply drivers
6	Mode1	Output mode selection gate driver
7	CKV	Clock gate driver
8	STV	Start pulse gate driver
9	VSS	Ground
10	VCOM_TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL	Clock source driver
14	D0	Data signal source driver
15	D1	Data signal source driver
16	D2	Data signal source driver
17	D3	Data signal source driver
18	D4	Data signal source driver
19	D5	Data signal source driver
20	D6	Data signal source driver
21	D7	Data signal source driver
22	VSS	Ground
23	D8	Data signal source driver
24	D9	Data signal source driver
25	D10	Data signal source driver
26	D11	Data signal source driver
27	D12	Data signal source driver
28	D13	Data signal source driver
29	D14	Data signal source driver
30	D15	Data signal source driver
31	XSTL	Start pulse source driver
32	XLE	Latch enable source driver
33	XOE	Output enable source driver
34	ISEL	L: input data bus width is 8-bit, i.e., D7 ~ D0 are valid
35	NC	NO Connection
36	VPOS	Positive power supply source driver
37	NC	NO Connection
38	VNEG	Negative power supply source driver
39	VCOM_FPL	Common Voltage
40	NC	NO Connection
41	STV2	Start pulse gate driver
42	NC	NO Connection
43	NC	NO Connection
44	NC	NO Connection
45	NC	NO Connection
46	NC	NO Connection
47	NC	NO Connection
48	NC	NO Connection
49	NC	NO Connection
50	STL2	Data shift start pulse 2

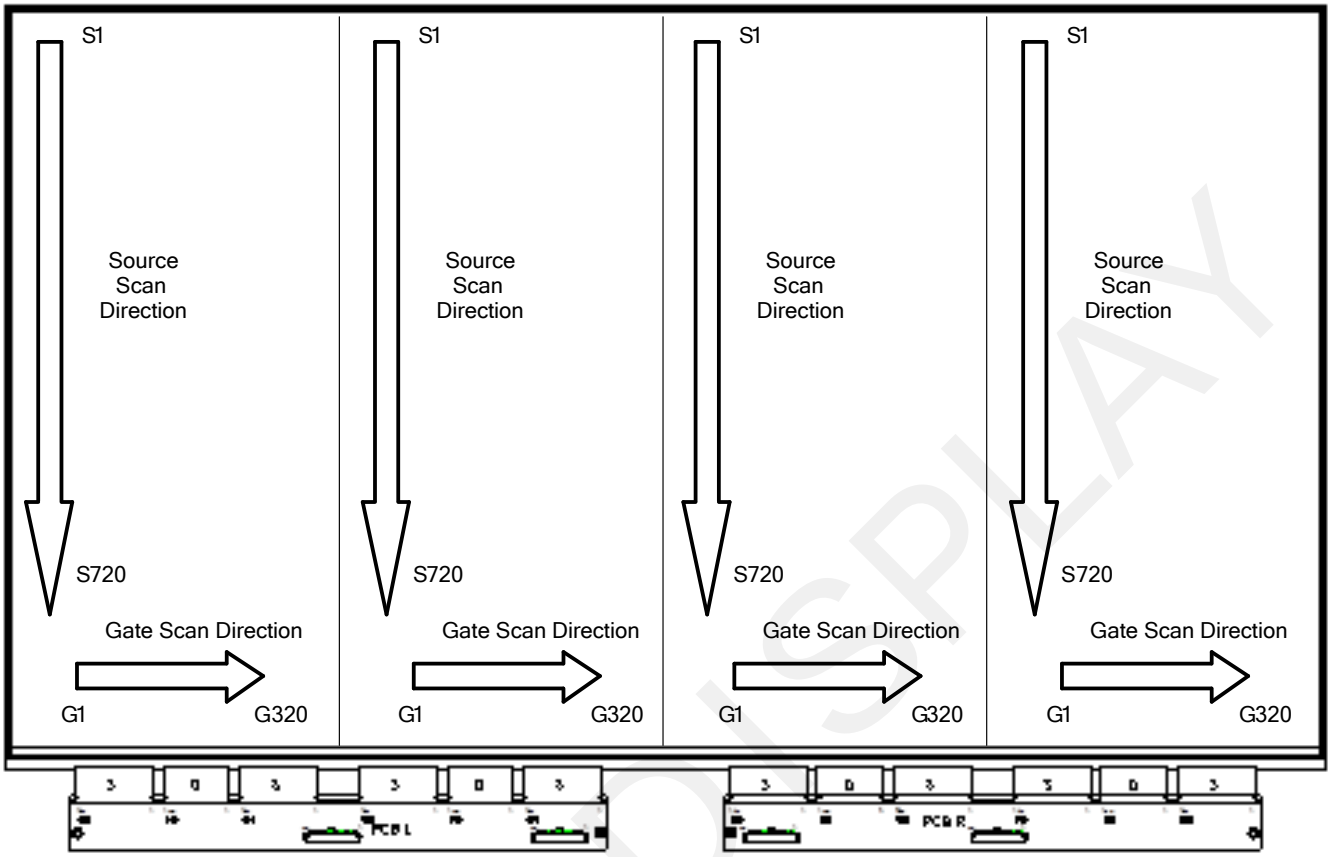
3) FPC R1

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	NO Connection
3	VGH	Positive power supply gate driver
4	Mode2	Output mode selection gate driver
5	VDD	Digital power supply drivers
6	Mode1	Output mode selection gate driver
7	CKV	Clock gate driver
8	STV	Start pulse gate driver
9	VSS	Ground
10	VCOM_TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL	Clock source driver
14	D0	Data signal source driver
15	D1	Data signal source driver
16	D2	Data signal source driver
17	D3	Data signal source driver
18	D4	Data signal source driver
19	D5	Data signal source driver
20	D6	Data signal source driver
21	D7	Data signal source driver
22	VSS	Ground
23	D8	Data signal source driver
24	D9	Data signal source driver
25	D10	Data signal source driver
26	D11	Data signal source driver
27	D12	Data signal source driver
28	D13	Data signal source driver
29	D14	Data signal source driver
30	D15	Data signal source driver
31	XSTL	Start pulse source driver
32	XLE	Latch enable source driver
33	XOE	Output enable source driver
34	ISEL	L: input data bus width is 8-bit, i.e., D7 ~ D0 are valid
35	NC	NO Connection
36	VPOS	Positive power supply source driver
37	NC	NO Connection
38	VNEG	Negative power supply source driver
39	VCOM_FPL	Common Voltage
40	NC	NO Connection
41	STV2	Start pulse gate driver
42	NC	NO Connection
43	NC	NO Connection
44	NC	NO Connection
45	NC	NO Connection
46	NC	NO Connection
47	NC	NO Connection
48	NC	NO Connection
49	NC	NO Connection
50	STL2	Data shift start pulse 2

4) FPC R2

Pin #	Signal	Description
1	VGL	Negative power supply gate driver
2	NC	NO Connection
3	VGH	Positive power supply gate driver
4	Mode2	Output mode selection gate driver
5	VDD	Digital power supply drivers
6	Mode1	Output mode selection gate driver
7	CKV	Clock gate driver
8	STV	Start pulse gate driver
9	VSS	Ground
10	VCOM_TFT	Common voltage
11	VDD	Digital power supply drivers
12	VSS	Ground
13	XCL	Clock source driver
14	D0	Data signal source driver
15	D1	Data signal source driver
16	D2	Data signal source driver
17	D3	Data signal source driver
18	D4	Data signal source driver
19	D5	Data signal source driver
20	D6	Data signal source driver
21	D7	Data signal source driver
22	VSS	Ground
23	D8	Data signal source driver
24	D9	Data signal source driver
25	D10	Data signal source driver
26	D11	Data signal source driver
27	D12	Data signal source driver
28	D13	Data signal source driver
29	D14	Data signal source driver
30	D15	Data signal source driver
31	XSTL	Start pulse source driver
32	XLE	Latch enable source driver
33	XOE	Output enable source driver
34	ISEL	L: input data bus width is 8-bit, i.e., D7 ~ D0 are valid
35	NC	NO Connection
36	VPOS	Positive power supply source driver
37	NC	NO Connection
38	VNEG	Negative power supply source driver
39	VCOM_FPL	Common Voltage
40	NC	NO Connection
41	STV2	Start pulse gate driver
42	G640	Detect IC function
43	S400	Detect IC function
44	S320	Detect IC function
45	NC	NO Connection
46	NC	NO Connection
47	S320	Detect IC function
48	S400	Detect IC function
49	G640	Detect IC function
50	STL2	Data shift start pulse 2

5-2) Panel Scan direction



6.Electrical Characteristics

6-1) Absolute maximum rating

Parameter	Symbol	Rating	Unit	Remark
Logic Supply Voltage	VDD	-0.3 to +7	V	--
Positive Supply Voltage	V_{POS}	-0.3 to +18	V	--
Negative Supply Voltage	V_{NEG}	+0.3 to -18	V	--
Max .Drive Voltage Range	V_{POS} - V_{NEG}	36	V	--
Supply Voltage	VGH	-0.3 to +55	V	--
Supply Voltage	VGL	-32 to +0.3	V	--
Supply Range	VGH-VGL	-0.3 to +55	V	--
Operating Temp. Range	TOTR	0 to +50	℃	--
Storage Temperature	TSTG	-25 to +70	℃	--

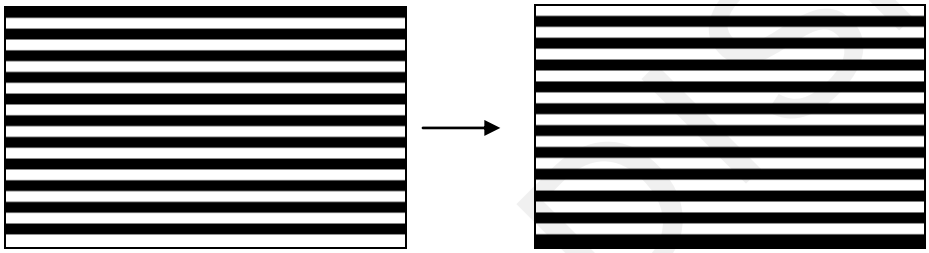
6-2) Panel DC characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	V_{SS}		-	0	-	V
Logic Voltage supply	V_{DD}		2.7	-	3.6	V
	I_{VDD}	V_{DD}=3.3V	-	TBD	TBD	mA
Gate Negative supply	V_{GL}		-21	-	-19	V
	I_{GL}	V_{GL} = -20V	-	TBD	TBD	mA
Gate Positive supply	V_{GH}		21	-	23	V
	I_{GH}	V_{GH} = 22V	-	TBD	TBD	mA
Source Negative supply	V_{NEG}		-15.4	-	-14.6	V
	I_{NEG}	V_{NEG} = -15V	-	TBD	TBD	mA
Source Positive supply	V_{POS}		14.6	-	15.4	V
	I_{POS}	V_{POS} = 15V	-	TBD	TBD	mA
Asymmetry source	V_{Asym}	V_{POS}+V_{NEG}	TBD	TBD	TBD	mV
Common voltage	V_{COM}		TBD	Adjusted	TBD	V
	I_{COM}		-	TBD	-	mA
Panel power	P		-	TBD	TBD	mW
Standby power panel	P_{STBY}		-	-	TBD	mW

- The maximum power consumption is measured using 50Hz waveform with following pattern transition: from pattern of repeated 1 consecutive black scan lines followed by 1 consecutive white scan line to that of repeated 1 consecutive white scan lines followed by 1 consecutive black scan lines. (Note 6-1)
- The Typical power consumption is measured using 50Hz waveform with following pattern transition: from horizontal 4 gray scale pattern to vertical 4 gray scale pattern. (Note 6-2)
- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by E Ink.
- Vcom is recommended to be set in the range of assigned value ± 0.1V.
- The maximum I_{COM} inrush current is about TBD mA

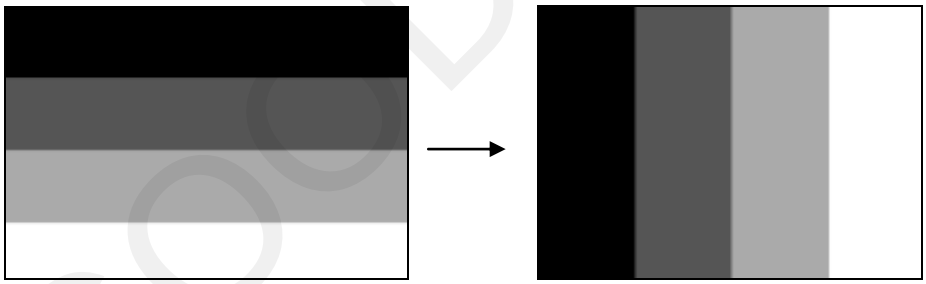
Note 6-1

The maximum power consumption



Note6-2

The Typical power consumption



6-3)Refresh Rate

The module GDEP312TT2-C is applied at a maximum screen refresh rate of 50Hz.

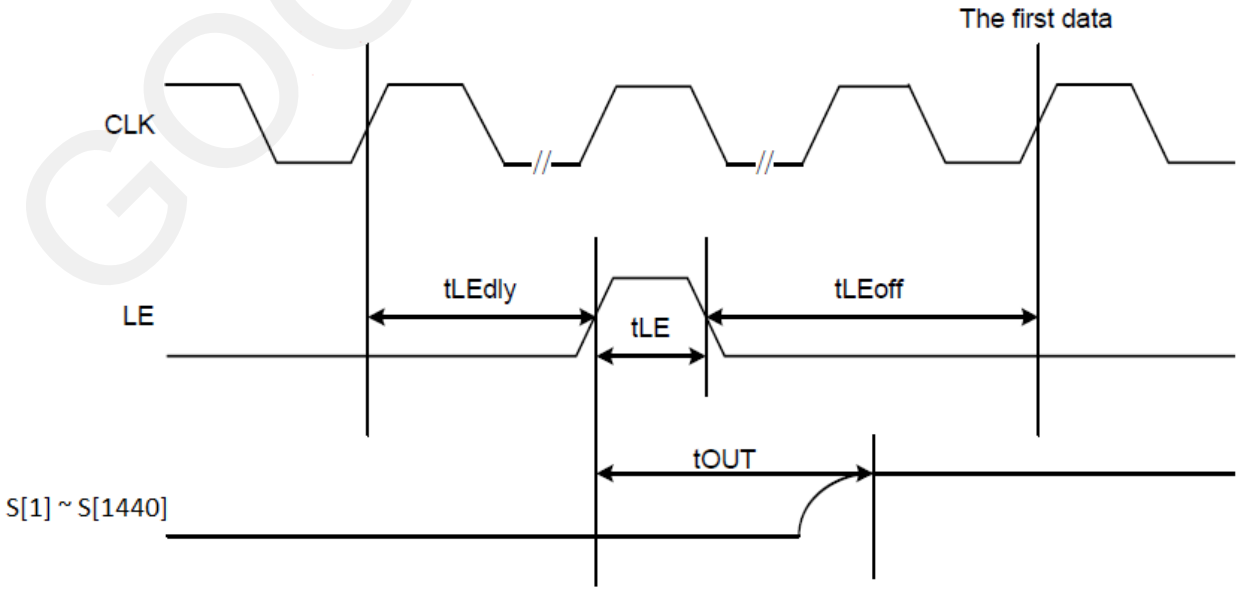
	Min	Max
Refresh Rate	-	50Hz

6-4)Panel AC characteristics

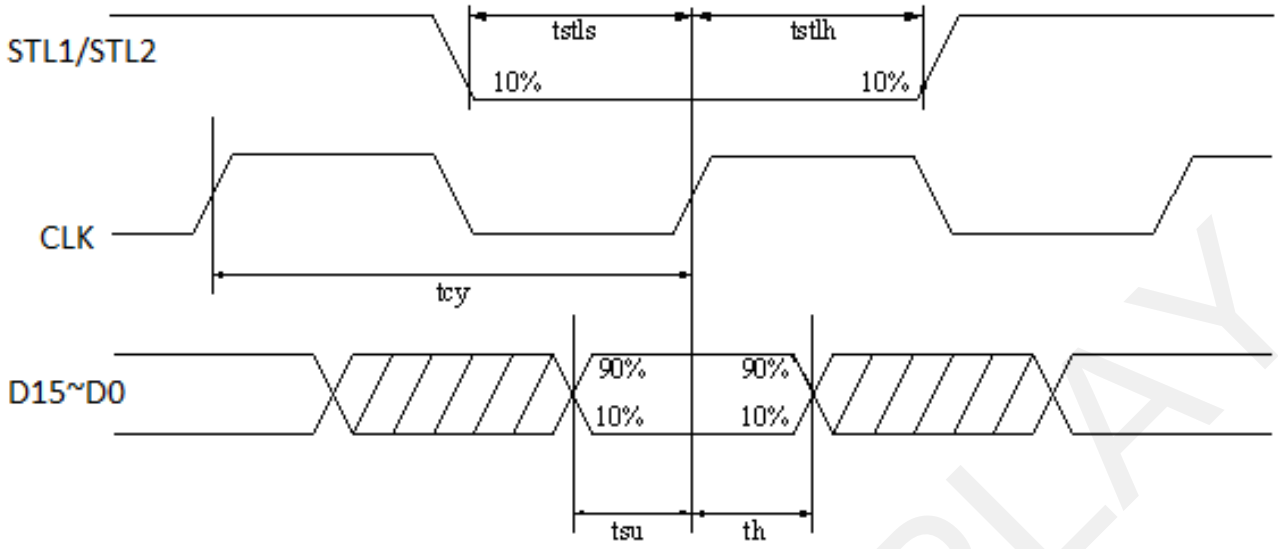
VDD=2.7V to 3.6V, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	fckv	-	-	200	kHz
Minimum “L” clock pulse width	twL	1	-	-	us
Clock rise time	trckv	-	-	100	ns
Clock fall time	tfckv	-	-	100	ns
SPV setup time	tSU	100	-	-	ns
SPV hold time	tH	100	-	-	ns
Pulse rise time	trspv	-	-	100	ns
Pulse fall time	tfspv	-	-	100	ns
Clock XCL cycle time	tcy	16.7	20	-	ns
D0 .. D7 setup time	tsu	8	-	-	ns
D0 .. D7 hold time	th	8	-	-	ns
XSTL setup time	tstls	8	-	-	ns
XSTL hold time	tstlh	8	-	-	ns
XLE on delay time	tLEdly	40	-	-	ns
XLE high-level pulse width (When VDD=2.7V to 3.6V)	tLEw	40	-	-	ns
XLE off delay time	tLEoff	200	-	-	ns
Output setting time to +/-30mV(C_{load}=200pF)	tout	-	-	12	us

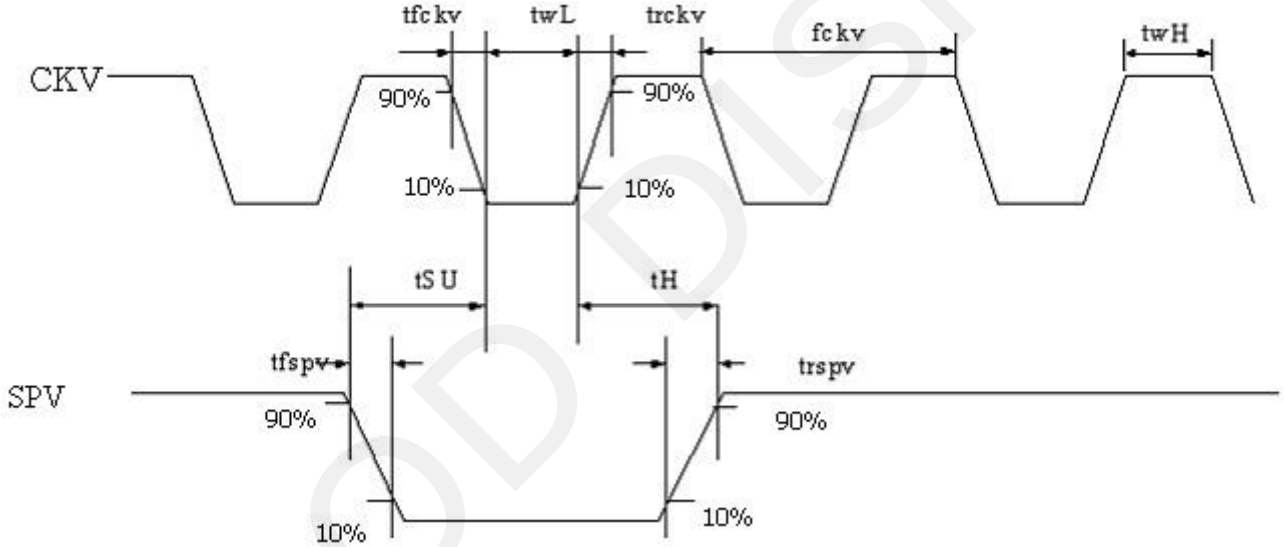
OUTPUT LATCH CONTROL SIGNALS



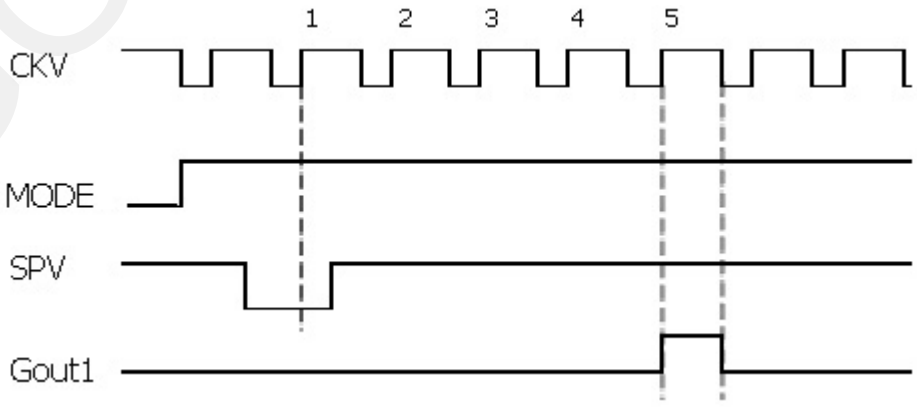
CLOCK & DATA TIMING



CKV & SPV TIMING



GATE OUTPUT TIMING

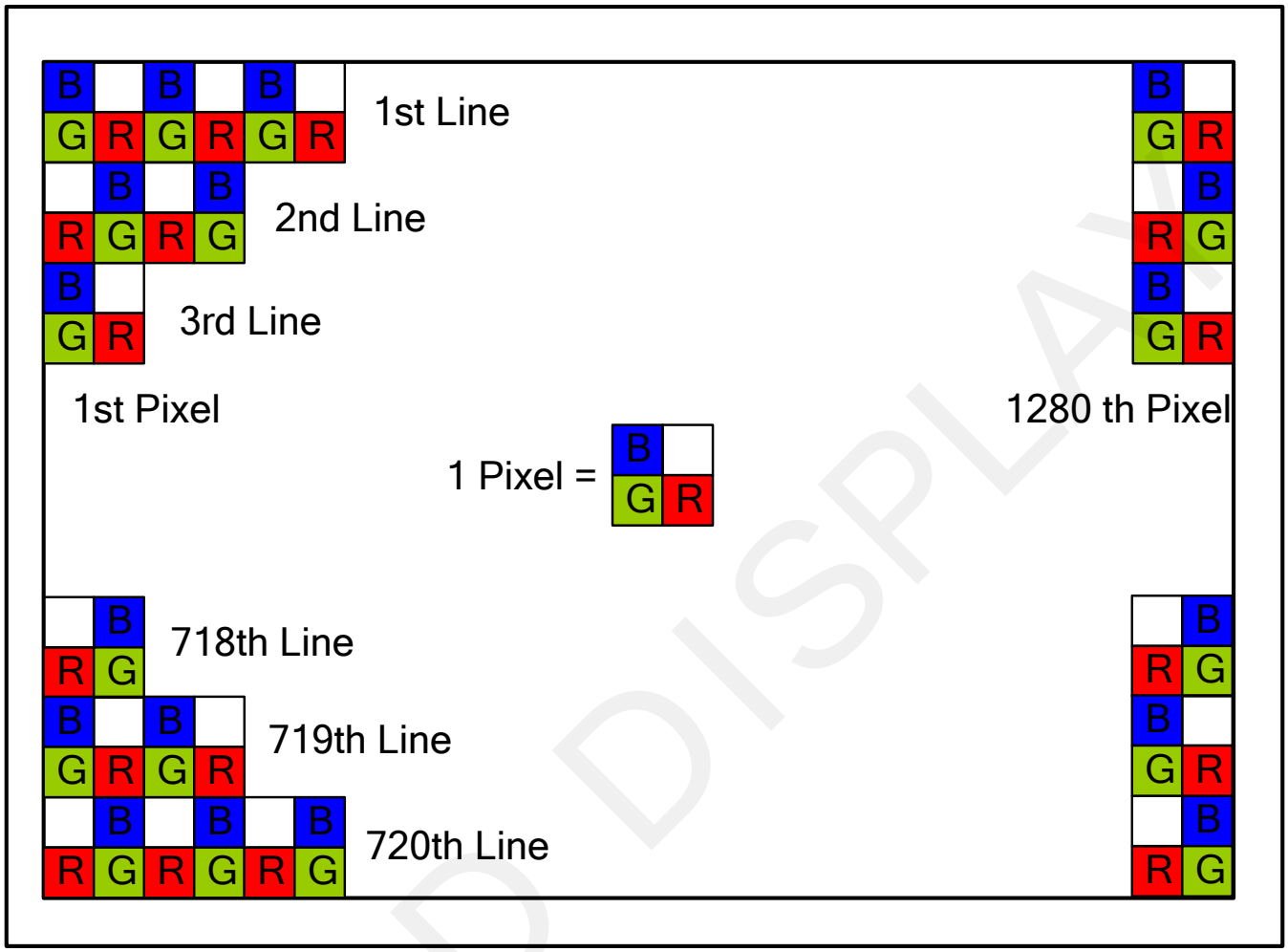


Note：First gate line on timing

After 5CKV，gate line is on .

7. Pixel Arrangement

The Color EPD module pixel arrangement is Square, with RGBW mosaic pattern in a unit pixel.

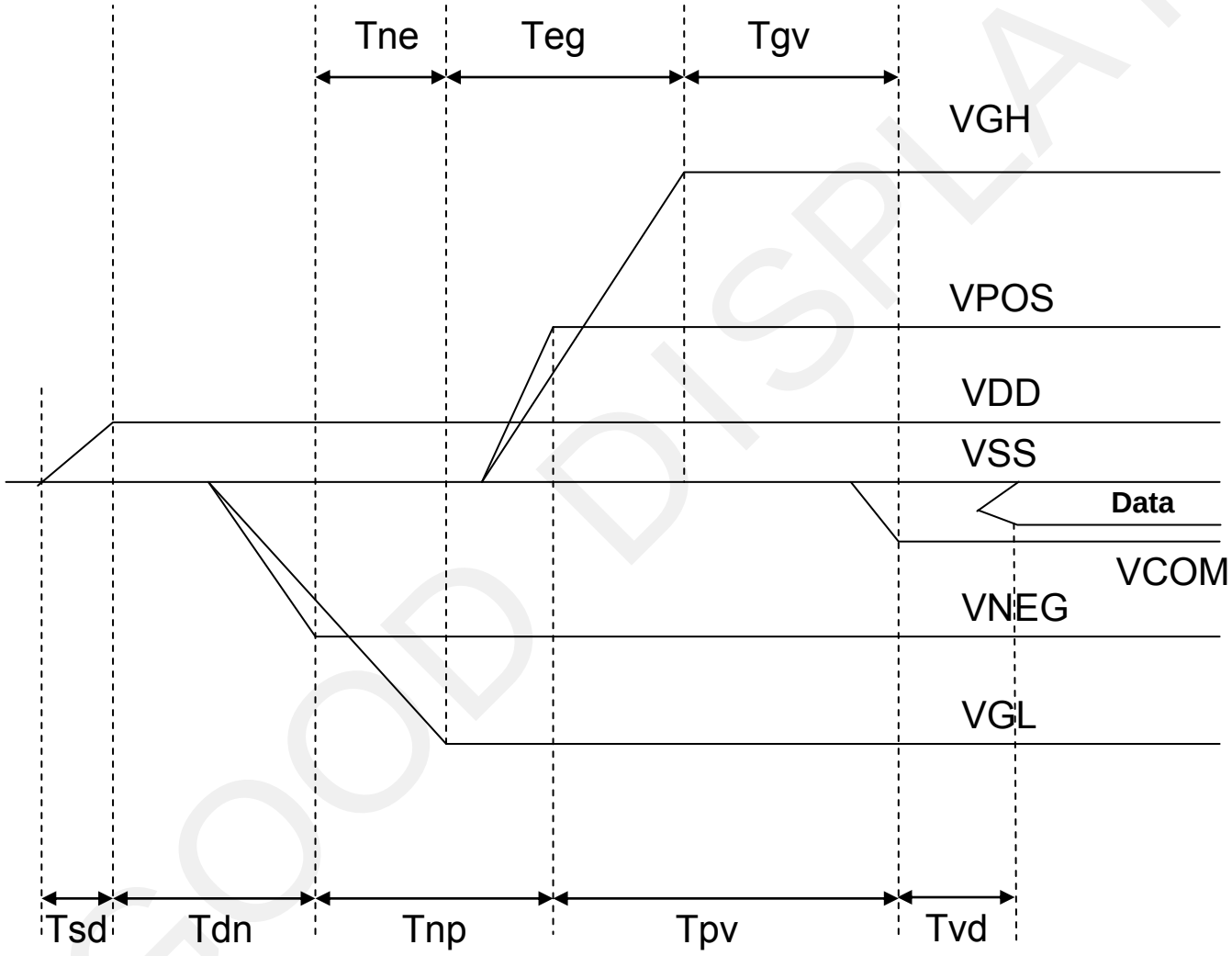


8. Power on Sequence

Power Rails must be sequenced in the following order：
1. VSS → VDD → VNEG → VPOS (Source driver) → VCOM

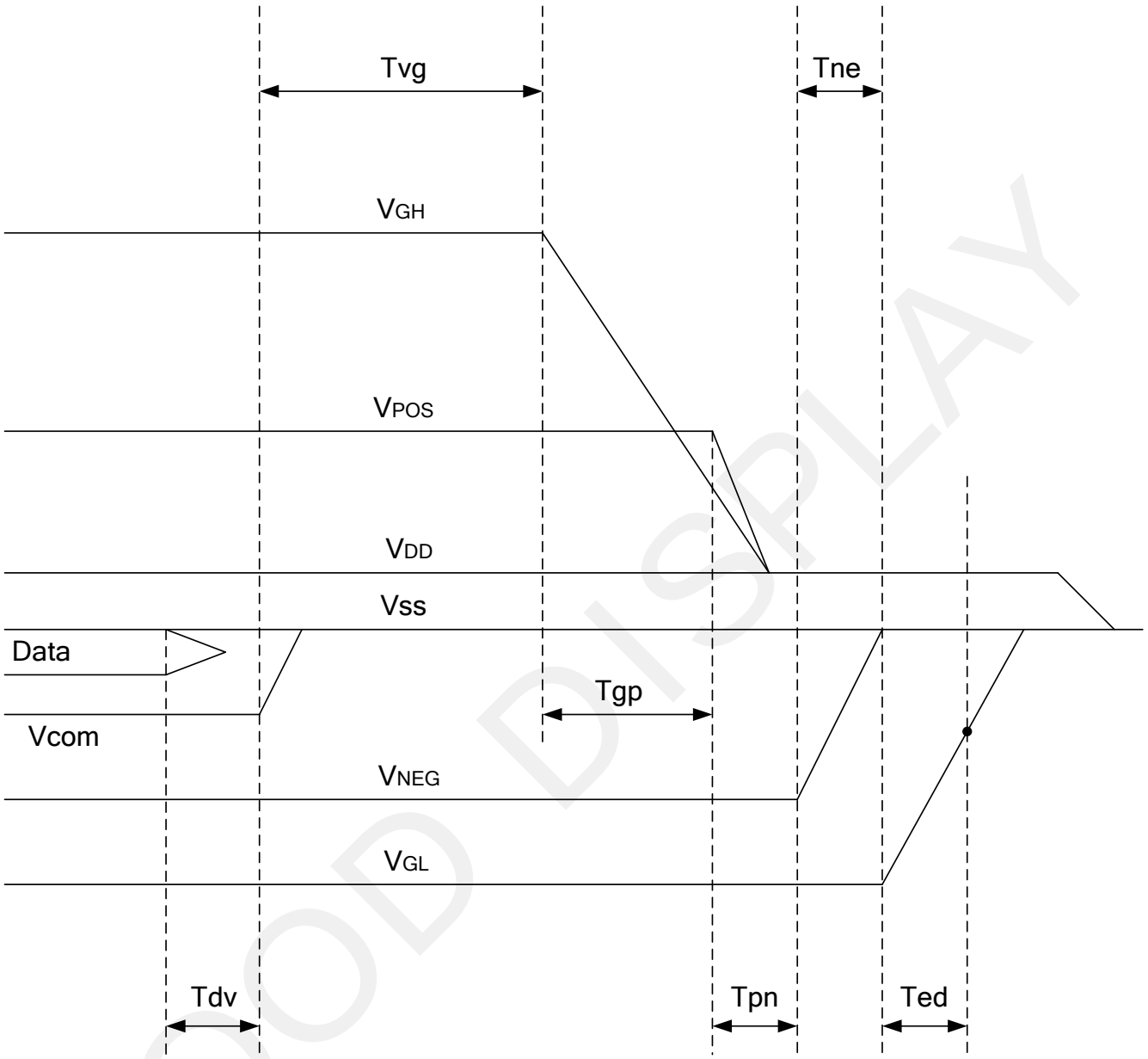
2. VSS → VDD → VGL → VGH (Gate driver)

Power on



	Min	Max
Tsd	30us	-
Tdn	100us	-
Tnp	1000us	-
Tpv	100us	-
Tvd	100us	-
Tne	0us	-
Teg	1000us	-
Tgv	100us	-

Power off



	Min	Max	
Tdv	100 μs	-	
Tvg	0 μs	-	
Tgp	0 μs	-	
Tpn	0 μs	-	
Tne	0 μs	-	
Ted	0.5s	-	Discharged point @ -7.4 Volt

Note1：Supply voltages decay through pull-down resistors.
Note2：Begin to turn off VGL power after VNEG and VPOS are completely or almost discharged to GND state.
Note3：VGL must remain negative of Vcom during decay period

9. Optical characteristics

9-1) Specifications

T = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
R	Reflectance	White	12 %	14 %	-	%	
NTSC ratio		-	-	13%	-	-	
Gn	N_{th} Grey Level	-	-	DS+(WS-DS)×n/(m-1)	-	L*	-
CR	Contrast Ratio	-	10	13	-	-	
Color/Chromaticity Coordinates		Wx	0.277	0.304	0.331	-	-
		Wy	0.301	0.328	0.355		
		Rx	0.401	0.428	0.455		
		Ry	0.314	0.341	0.368		
		Gx	0.260	0.287	0.314		
		Gy	0.432	0.459	0.486		
		Bx	0.201	0.228	0.255		
		By	0.184	0.211	0.238		

WS: White state , DS: Dark state, Gray state from Dark to White :DS、G1、G2…、Gn…、Gm-2、WS

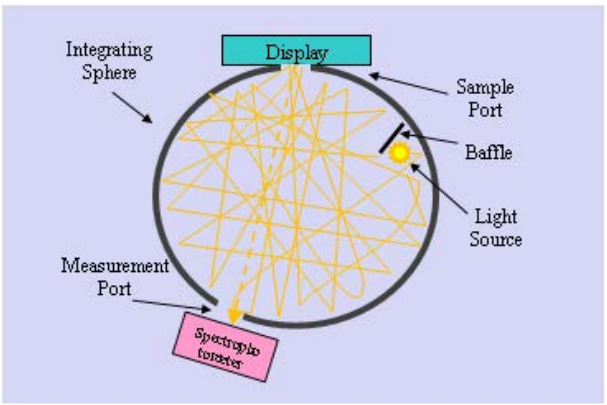
m:4、8、16 when 2、3、4 bits mode

Note ：Measurement Tool：Minolta 2600d optical geometry

9-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd)：

CR = Rl/Rd



9-3) Reflection Ratio

The reflection ratio is expressed as:

$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$

L_{center} is the luminance measured at center in a white area (R=G=B=1).

$L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination

source .Please set the illumination for D65 and the observer for 2 degree.

9-4) Definition of NTSC ratio

Here is the description of NTSC ratio calculation:
Calculate GA of triangle area composed of 3 primaries R (Rx, Ry), G (Gx, Gy), B (Bx, By)
Where GA=1/2(Rx*Gy + Ry*Bx + By*Gx – Ry*Gx - Gy*Bx -By*Rx)
Then NTSC ratio (%) = GA/NTSC Area
Where the NTSC Area is made by primary red (0.67,0.33), primary green(0.21,0.71) and primary blue of the original 1953 color NTSC specification in CIE 1931 color space

10. HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS AND REMARK

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	This data sheet contains Preliminary product specifications.
Limiting values	

Data sheet status
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and does not form part of the specification.
Remark
All the specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any post-assembly operation.

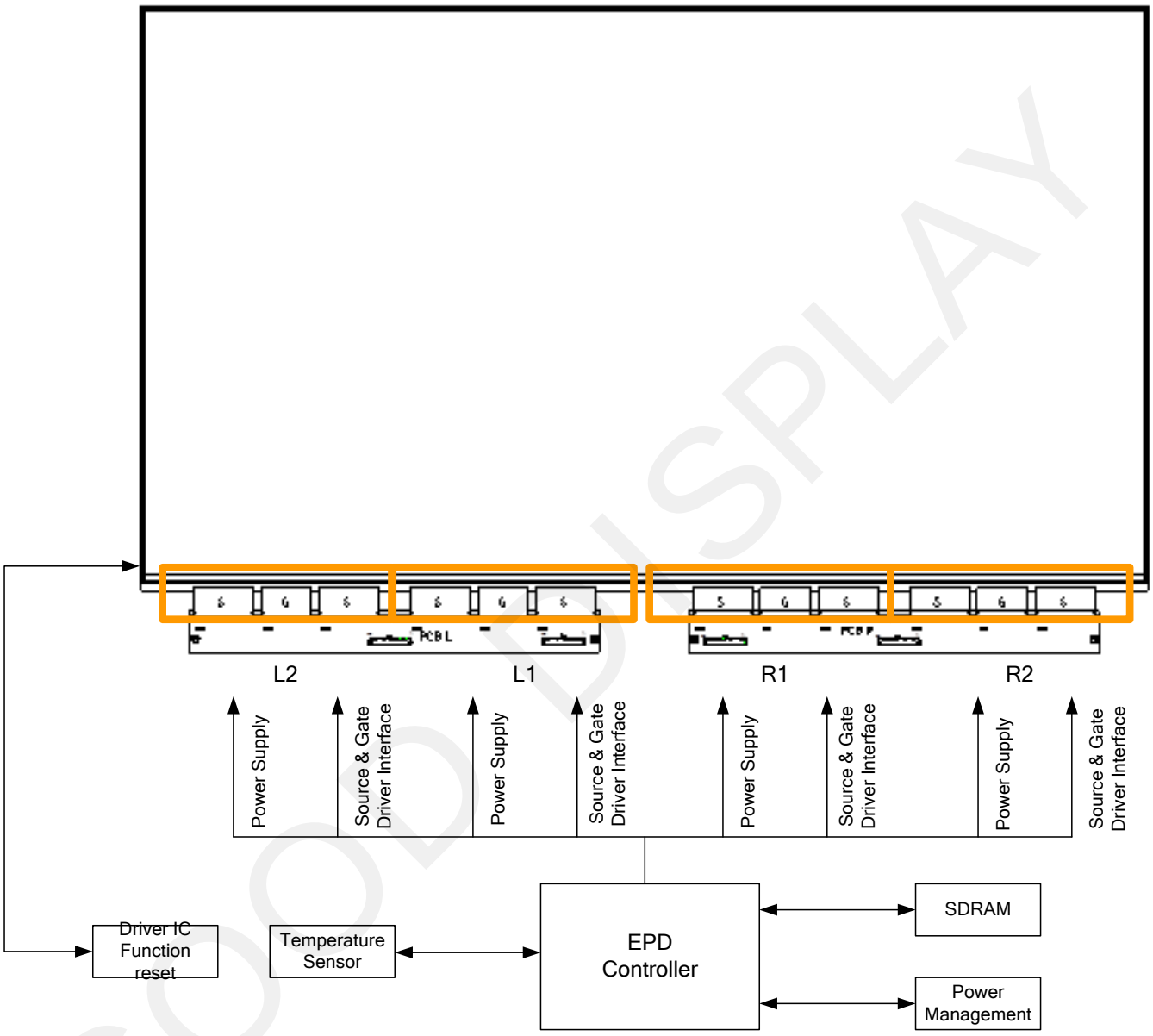
11. Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = +50°C, RH = 30% for 240 hrs	IEC 60 068-2-2Bp	
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T = +70°C, RH=23% for 240 hrs Test in white pattern	IEC 60 068-2-2Bp	
4	Low-Temperature Storage	T = -25°C for 240 hrs Test in white pattern	IEC 60 068-2-1Ab	
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	
6	High Temperature, High- Humidity Storage	T = +60℃, RH=80% for 168hrs Test in white pattern	IEC 60 068-2-3CA	
7	Temperature Cycle	-25℃→+70℃, 100 Cycles 30min 30min Test in white pattern	IEC 60 068-2-14	
9	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	
10	Package Drop Impact	Drop from height of 122 cm on concrete surface. Drop sequence: 1 corner, 3 edges, 6 faces One drop for each.	Full packed for shipment	
11	Electrostatic Effect (non-operating)	(Machine model)+/- 250V 0Ω, 200pF	IEC 62179, IEC 62180	

Actual EMC level to be measured on customer application
Note: The protective film must be removed before temperature test.

< Criteria >
In the standard conditions, there is not display function NG issue occurred. (including : line defect ,no image). All the cosmetic specification is judged before the reliability stress.

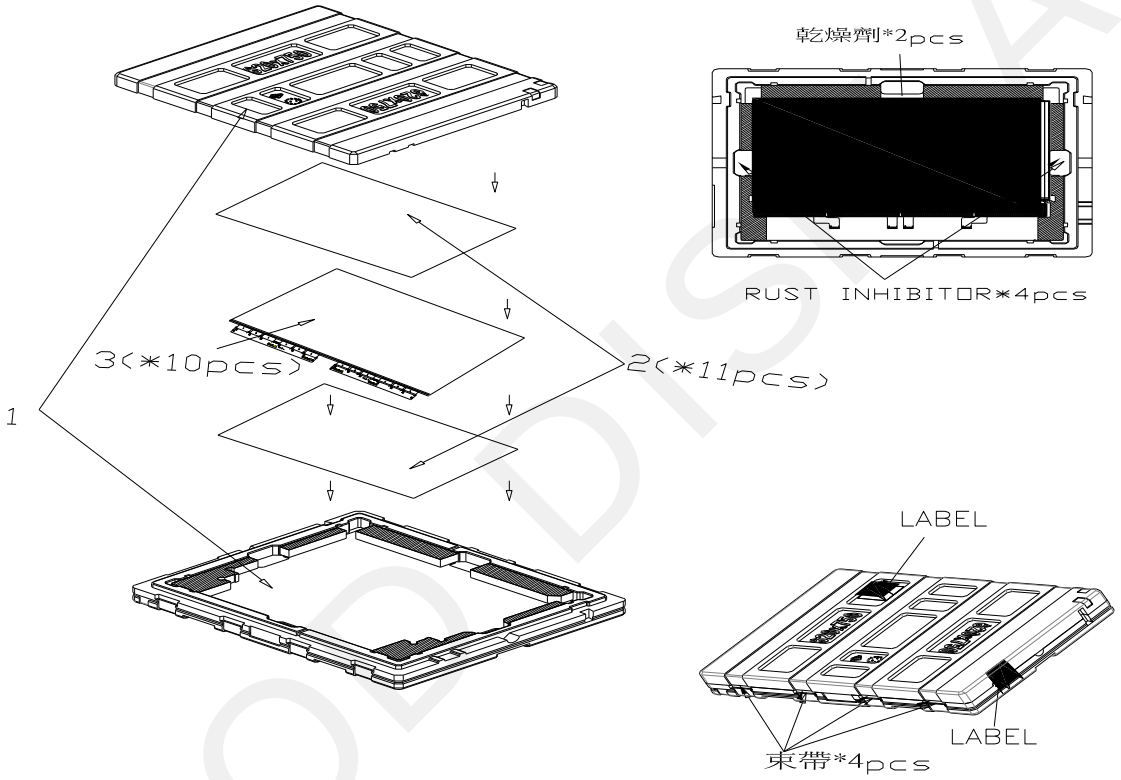
12. Block Diagram



13.Packing

13-1)Packing drawing

REV.	DESCRIPTION	DESIGN	DATE
01	INITIAL RELEASE	Anderson	20150810



NOTE:

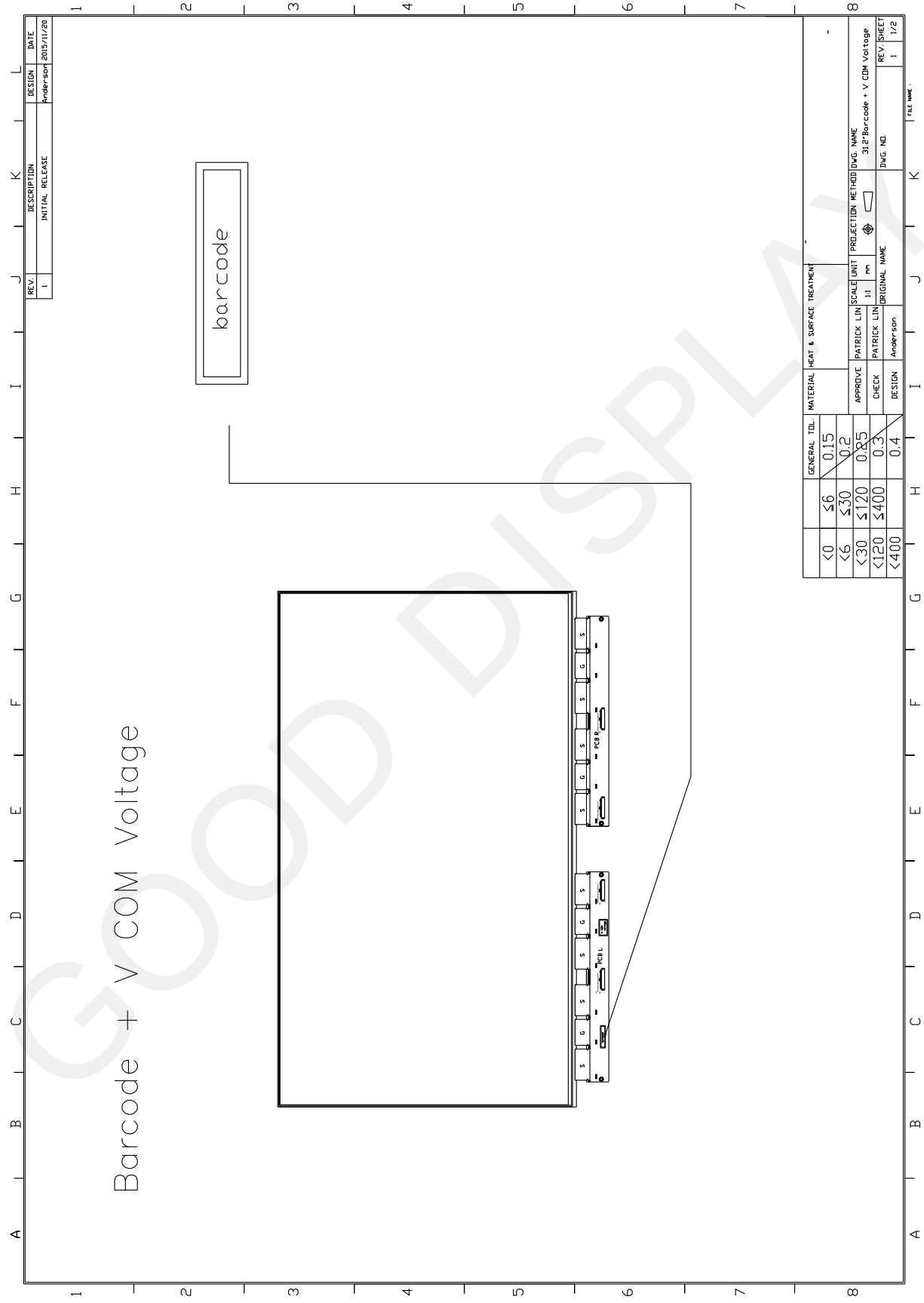
1.Q'TY: 10 pcs panel/carton.
2.Dimension: 890*760*138mm
3.Weight: KG

ITEM	PART NO	PART NAME	Q'ty
1		PP BOX	1
2		Cushion Sheet(2mm)	11
3		EPD Signage B/W	10
4		乾燥劑	2
5		RUST INHIBITOR,25L	4
6		LABEL	2
7		束帶	4
8			

MTL.SPEC.	UNSPECIFIED TOL'S ANGLE ROUGHNESS	REMARK	

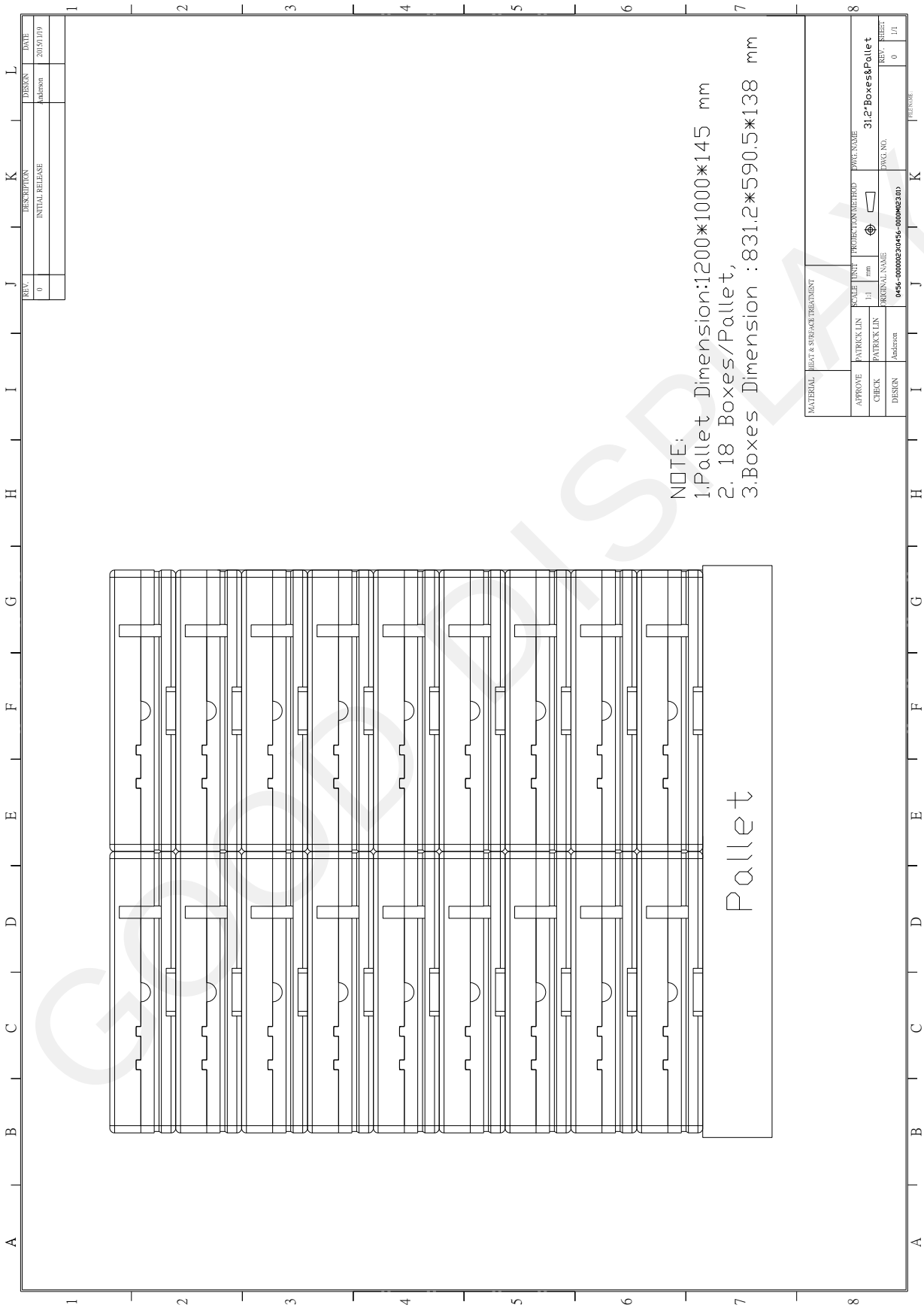
APPROVE	Patrick	20150527	SCALE 1:1	UNIT mm	SHEET 1 OF 1	DWG.TITLE 31.2" Packing Draw
CHECK	Patrick	20150527				
DESIGN	Anderson	20150527	MTL.NO.	DWG.NO.	REV. 01	A4 SIZE

13-2)Label Position



13-3)Pallet Stacking

Note: Stacking layer limination: 18 layers



14.Bar Code definition

EJA	00	7	01	1	I	7	4	00361	A	T
1	2	3	4	2	5	6	2	7	2	8

1：EPD model code

2：Internal control codes

3：Internal control codes

4：Internal control codes

5：Year:

P: 2014 / Q: 2015 / R: 2016 /... / Z: 2024

6：Month:

1:Jan. 2:Feb. ... 9:Sep. A:Oct. B:Nov. C:Dec.

7：Serial number

00000-99999

8：Internal control codes