HIGH-VOLTAGE MIXED-SIGNAL IC

UC8276

All-in-one driver IC w/ Timing Controller for
White/Black/Red Dot-Matrix Micro-Cup ESL

ES Specifications **IC Version: c_A**
Datasheet Revision: 0.6 (for_TFT_Module_Use_only) **November 19, 2019**

ULTRACHIP

The Coolest EPD Driver, Ever!

Table of Content

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All-in-one driver IC with Timing Controller for White/Black/Red Dot-Matrix Micro-Cup ESL

INTRODUCTION

The UC8276 is an all-in-one driver with timing controller for ESL. Its output is of 1-bit white/black and 1-bit red resolution per pixel. The timing controller provides control signals for source driver and gate driver.

The DC-DC controller allows it to generate the source output voltage VSH/VSL (±2.4V~±15.0V) and VDHR (2.4V~15.0V). The chip also includes an output buffer for the supply of the COM electrode (AC-VCOM or DC-VCOM). The system is configurable through a 3-wire/4-wire (SPI) serial interface.

MAIN APPLICATIONS

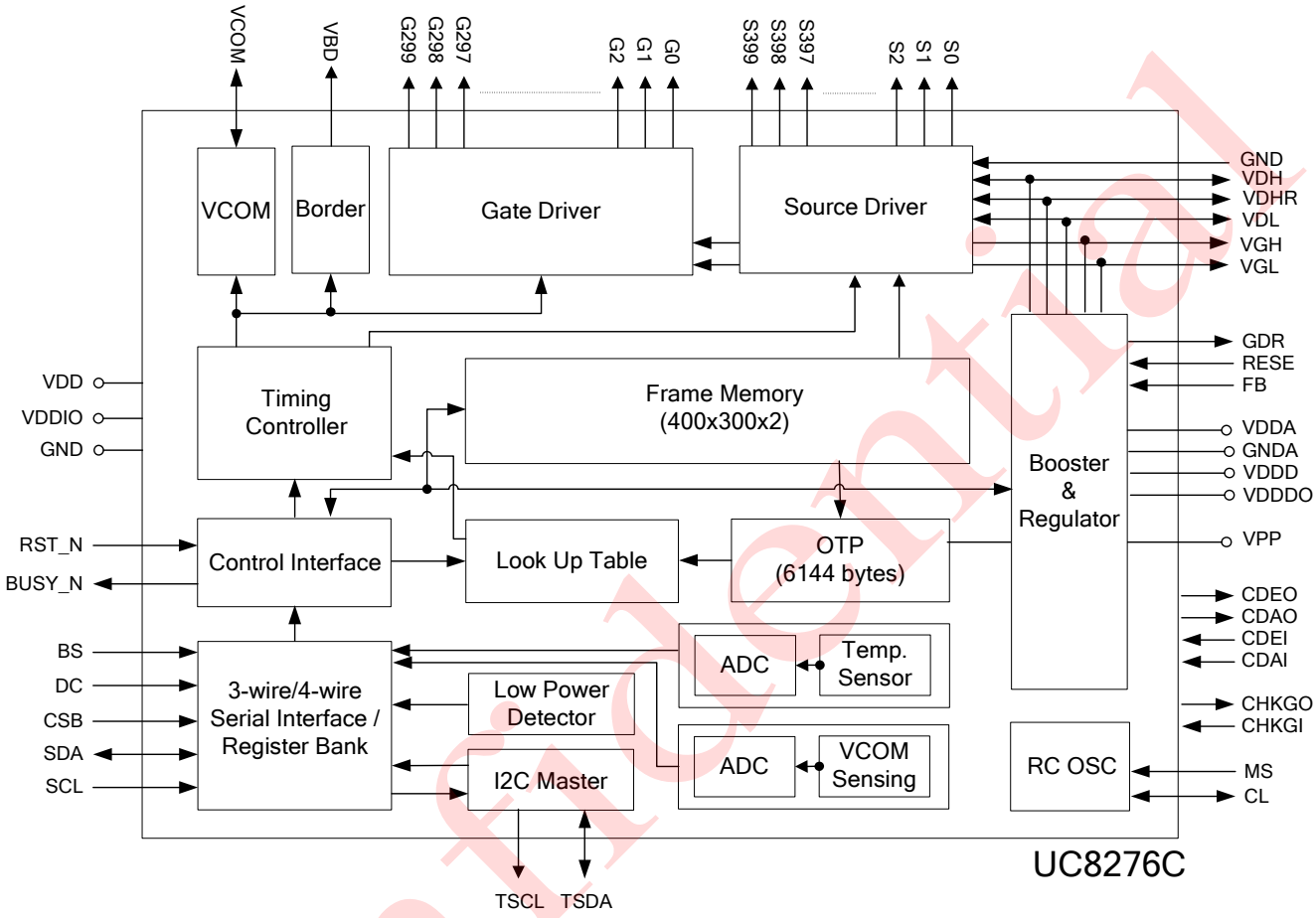
- E-tag application

FEATURE HIGHLIGHTS

- System-on-chip (SOC) for ESL
- Timing controller supports several resolutions
  - Up to 400 source x 300 gate resolution + 1 border + 1 VCOM
  - 1 bit for white/black and 1 bit for red per pixel
- Cascade: 2 or more chips cascade mode
- Memory (Max.): 400 x 300 x 2 bits SRAM
- 3-wire/4-wire (SPI) serial interface
  - Clock rate up to 20MHz
- Temperature sensor:
  - On-Chip: -25~50 °C ± 2.0°C / 8-bit status
  - Off-Chip: -55~125°C ± 2.0°C /11-bit status (I^2C/LM75)
- Support LPD, Low Power Detection (V_{DD}<2.5V)
- OSC / PLL: On-chip RC oscillator
- VCOM:
  - AC-VCOM / DC-VCOM (by LUT)
  - Support VCOM sensing (7-bit digital status)
- Charge Pump: On-chip booster and regulator:
  - VGH: +20V
  - VGL: -20V
  - VSH: +2.4 ~ +15.0V (programmable, black/white)
  - VSL: -2.4 ~ -15.0V (programmable, black/white)
  - VDHR: +2.4 ~ +15.0V (programmable, red)
- Supply voltage: 2.3~ 3.6V
- OTP: 6K-byte OTP for LUTs and Settings
- Package: COG
- Source/Gate bump information
  - Bump pitch: 12 μM ± 3 μM
  - Bump space: 1 μM ± 3 μM
  - Bump surface: 1200 μM^2

Remark: The inspection standard of the product appearance is based on Ultrachip's inspection document.

BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Description
UC8276cGAA-U0P3-3	3-inch tray, wafer thickness 300uM
UC8276cGAA-U0P3-4	4-inch tray, wafer thickness 300uM
UC8276cGAA-U0X3-3	3-inch tray, wafer thickness 300uM
UC8276cGAA-U0X3-4	4-inch tray, wafer thickness 300uM

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

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PIN DESCRIPTION

Type: I: Input, O: Output, I/O: Input/Output, PWR: Power, C: Capacitor pin

Pin (Pad) Name	Pin Count	Type	Description
POWER SUPPLY PINS			
VDD	7	PWR	Digital power
VDDA	10	PWR	Analog power
VDDIO	10	PWR	IO power
VDDDO	5	PWR	Digital power output (1.8V)
VDDD (VDDDI)	5	PWR	Digital power input (1.8V)
VPP	7	PWR	OTP program power (7.75V)
VDM	3	PWR	Analog Ground.
GND	32	PWR	Digital Ground.
GNDA	10	PWR	Analog Ground.
LDO PINS			
VSH	10	I/O	Positive source driver Voltage (+2.4V ~ +15V)
VDHR	8	I/O	Positive source driver voltage for Red (+2.4V ~ +15V)
VSL	10	I/O	Negative source driver voltage (-2.4V ~ -15V)
CONTROL INTERFACE PINS			
BS	1	I	Bus Selection. Select 3-wire / 4-wire SPI interface L: 4-wire interface. **H: 3-wire interface. (Default)**
RST_N	1	I (Pull-up)	Global reset pin. L: active. When RST_N become low, driver will reset. All register will reset to default value. Driver all function will disable. Source/Gate/Border/VCOM will be released to floating. The minimal width of RST_N=low is 50us.
MS	1	I	Cascade setting pin. L: Slave chip. H: Master chip.
CL	1	I/O	Clock input/output pin. Master: Clock output. Slave: Clock input.
CDEI	1	I	Cascade signal input pin. Connect to GND if not used.
CDEO	1	O	Cascade signal output pin. Leave it open if not used.
CDAI	1	I	Cascade data input pin. Connect to GND if not used.
CDAO	1	O	Cascade data output pin. Leave it open if not used.
BUSY_N	1	O	Driver busy flag. L: Driver is Busy. H: Host side can send command/data to driver.

Pin (Pad) Name	Pin Count	Type	Description
MCU INTERFACE (SPI) PINS			
CSB	1	I	Serial communication chip select.
SDA	1	I/O	Serial communication data input/output
SCL	1	I	Serial communication clock input.
DC	1	I	Command/Data input. L: command H: data Connect to GND if BS=High.
I²C INTERFACE			
TSCL	2	O (open-drain)	I²C clock (External pull-up resistor is necessary.) Leave them open if not used.
TSDA	2	I/O (open-drain)	I²C data (External pull-up resistor is necessary.) Leave them open if not used.
OUTPUT PINS			
S0~S399 (S<0>~S<399>)	400	O	Source driver output signals.
G0~G299 (G<0>~G<299>)	300	O	Gate driver output signals.
VCOM	16	O	VCOM output.
VBD (VBD<1>~VBD<2>)	2	O	Border output pins.
BOOSTER PINS			
GDR	8	O	N-MOS gate control
RESE	2	P	Current sense input for control loop.
FB	2	P	(Keep Open.)
VGH	14	I/O	Positive Gate voltage.
VGL	16	I/O	Negative Gate voltage.
CHECK PANEL PINS			
CHKGI	1	I (Pull-down)	Check panel break input.
CHKGO	1	O	Check panel break output.
RESERVED PINS			
VSYNC	1	O	Reserved pins. Leave it floating.
TEST1~TEST3	1x3	I	Reserved pins. Leave it floating or connected to VSS.
TEST5~TEST7	1x3	O	Reserved pins. Leave it floating.
TEST8~13	1x6	O	Reserved pins. Leave it floating.
DUMMY<1> ~ DUMMY<71>	71	-	Reserved pins. Leave it floating.
NC	29	--	Not Connected.
GD<0>~GD<3>	1x4		Reserved pins. Leave it floating.

COMMAND TABLE

W/R: 0: Write Cycle 1: Read Cycle C/D: 0: Command / 1: Data D7~D0: –: Don't Care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00H
		0	1	#	#	#	#	#	#	#	#	RES[1:0],REG,KW/R,UD,SHL, SHD_N,RST_N	0FH
		0	1	--	--	--	#	#	#	#	#	VCMZ ,TS_AUTO,TIEG,NORG,VC_LUTZ	0DH
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01H
		0	1	--	--	--	#	--	--	#	#	BD_EN ,VDS_EN, VDG_EN	03H
		0	1	--	--	--	#	#	#	#	#	VCOM_SLEW,VGHL_LV[3:0]	10H
		0	1	--	--	#	#	#	#	#	#	VSH[5:0]	3FH
		0	1	--	--	#	#	#	#	#	#	VSL[5:0]	3FH
		0	1	#	#	#	#	#	#	#	#	OPTEN,VDHR[6:0]	0DH
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0		02H
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03H
		0	1	--	--	#	#	--	--	--	--	T_VDS_OF[1:0]	00H
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04H
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05H
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06H
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17H
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17H
		0	1	--	--	#	#	#	#	#	#	BT_PHC[5:0]	17H
8	Deep sleep (DSLP)	0	0	0	0	0	0	0	1	1	1		07H
		0	1	1	0	1	0	0	1	0	1	Check code	A5H
9	Display Start Transmission 1 (DTM1, White/Black Data) (x-byte command)	0	0	0	0	0	1	0	0	0	0	B/W or OLD Pixel Data (400x300):	10H
		0	1	#	#	#	#	#	#	#	#	KPXL[1:8]	-
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	KPXL[n-1:n]	-
10	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11H
		1	1	#	--	--	--	--	--	--	--		00H
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12H
12	Display Start transmission 2 (DTM2, Red Data) (x-byte command)	0	0	0	0	0	1	0	0	1	1	Red or NEW Pixel Data (400x300):	13H
		0	1	#	#	#	#	#	#	#	#	RPXL[1:8]	-
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	#	#	#	#	#	RPXL[n-1:n]	-
13	Auto Sequence (AUTO)	0	0	0	0	0	1	0	1	1	1		17H
		0	1	1	0	1	0	0	1	0	1	Check code	A5H
14	VCOM LUT (LUTC) (57-byte command, structure of bytes 2~8 repeated 8 times)	0	0	0	0	1	0	0	0	0	0		20H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-1[1:0], FRAME NUMBER 1-1[5:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-2[1:0], FRAME NUMBER 1-2[5:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-1[1:0], FRAME NUMBER 2-1[5:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-2[1:0], FRAME NUMBER 2-2[5:0]	-
		0	1	#	#	#	#	#	#	#	#	STATE 1 REPEAT TIMES [7:0]	-
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	-

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
15	W2W LUT (LUTWW) (43-byte command, structure of bytes 2~8 repeated 6 times)	0	0	0	0	1	0	0	0	0	1		21H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-1[1:0], FRAME NUMBER 1-1[5:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-2[1:0], FRAME NUMBER 1-2[5:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-1[1:0], FRAME NUMBER 2-1[5:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-2[1:0], FRAME NUMBER 2-2[5:0]	-
		0	1	#	#	#	#	#	#	#	#	STATE 1 REPEAT TIMES [7:0]	-
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	-
16	K2W LUT (LUTKW / LUTR) (57-byte command, structure of bytes 2~8 repeated 8 times)	0	0	0	0	1	0	0	0	1	0		22H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-1[1:0], FRAME NUMBER 1-1[5:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-2[1:0], FRAME NUMBER 1-2[5:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-1[1:0], FRAME NUMBER 2-1[5:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-2[1:0], FRAME NUMBER 2-2[5:0]	-
		0	1	#	#	#	#	#	#	#	#	STATE 1 REPEAT TIMES [7:0]	-
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	-
17	W2K LUT (LUTWK / LUTW) (57-byte command, structure of bytes 2~8 repeated 8 times)	0	0	0	0	1	0	0	0	1	1		23H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-1[1:0], FRAME NUMBER 1-1[5:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-2[1:0], FRAME NUMBER 1-2[5:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-1[1:0], FRAME NUMBER 2-1[5:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-2[1:0], FRAME NUMBER 2-2[5:0]	-
		0	1	#	#	#	#	#	#	#	#	STATE 1 REPEAT TIMES [7:0]	-
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	-
18	K2K LUT (LUTKK / LUTK) (57-byte command, structure of bytes 2~8 repeated 8 times)	0	0	0	0	1	0	0	1	0	0		24H
		0	1	#	#	#	#	#	#	#	#	GROUP REPEAT TIMES [7:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-1[1:0], FRAME NUMBER 1-1[5:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT1-2[1:0], FRAME NUMBER 1-2[5:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-1[1:0], FRAME NUMBER 2-1[5:0]	-
		0	1	:	:	:	:	:	:	:	:	LEVEL SELECT2-2[1:0], FRAME NUMBER 2-2[5:0]	-
		0	1	#	#	#	#	#	#	#	#	STATE 1 REPEAT TIMES [7:0]	-
		0	1	#	#	#	#	#	#	#	#	STATE 2 REPEAT TIMES [7:0]	-
19	LUT option (LUTOPT)	0	0	0	0	1	0	1	0	1	0		2AH
		0	1	#	#	--	--	--	--	--	--	EOPT,ESO	00H
		0	1	#	#	#	#	#	#	#	#	STATE_XON[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	STATE_XON[15:8]	00H
		0	1	#	#	#	#	#	#	#	#	GROUP_KWE[7:0]	FFH
		0	1	--	--	--	--	--	--	#	#	ATRED,NORED	00H
20	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30H
		0	1	--	--	#	#	#	#	#	#	FRS[4:0]	09H
21	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0		40H
		1	1	#	#	#	#	#	#	#	#	D[10:3] / TS[7:0]	00H
		1	1	#	#	#	--	--	--	--	--	D[2:0] / -	00H
22	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1		41H
		0	1	#	--	--	--	#	#	#	#	TSE,TO[3:0]	00H
23	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42H
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00H
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
24	Temperature Sensor Read (TSR)	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**		**43H**
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00H
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00H
25	Panel Break Check (PBC)	0	0	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**		**44H**
		1	1	--	--	--	--	--	--	--	#	PSTA	00H
26	VCOM and data interval setting (CDI)	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**		**50H**
		0	1	#	#	#	#	#	#	#	#	VBD[1:0], DDX[1:0], CDI[3:0]	D7H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
27	Lower Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51H
		1	1	--	--	--	--	--	--	--	#	LPD	01H
28	TCON setting (TCON)	0	0	0	1	1	0	0	0	0	0		60H
		0	1	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	22H
29	Resolution setting (TRES)	0	0	0	1	1	0	0	0	0	1		61H
		0	1	--	--	--	--	--	--	--	#	HRES[8:3]	00H
		0	1	#	#	#	#	#	0	0	0		00H
		0	1	--	--	--	--	--	--	--	#	VRES[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
30	Gate/Source Start setting (GSST)	0	0	0	1	1	0	0	1	0	1		65H
		0	1	--	--	--	--	--	--	--	#	HST[8:3]	00H
		0	1	#	#	#	#	#	0	0	0		00H
		0	1	--	--	--	--	--	--	--	#	VST[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
31	Revision (REV)	0	0	0	1	1	1	0	0	0	0		70H
		1	1	#	#	#	#	#	#	#	#	RESERVED	FFH
		1	1	#	#	#	#	#	#	#	#	CHIP_REV[7:0]	07H
		1	1	#	#	#	#	#	#	#	#	LUT_VER[23:0]	FFH
		1	1	#	#	#	#	#	#	#	#		FFH
		1	1	#	#	#	#	#	#	#	#		FFH
32	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71H
		1	1	--	#	#	#	#	#	#	#	PTL_FLAG ,I²C_ERR, I²C_BUSYN, DATA_FLAG, PON, POF, BUSY_N	13H
33	Cyclic Redundancy Check (CRC)	0	0	0	1	1	0	0	0	1	0		72H
		1	1	#	#	#	#	#	#	#	#	CRC_MSB[7:0]	FFH
		1	1	#	#	#	#	#	#	#	#	CRC_LSB[7:0]	FFH
34	Auto Measurement VCOM (AMV)	0	0	1	0	0	0	0	0	0	0		80H
		0	1	--	--	#	#	#	#	#	#	AMVT[1:0], XON,AMVS, AMV, AMVE	10H
35	Read VCOM Value (VV)	0	0	1	0	0	0	0	0	0	1		81H
		1	1	--	#	#	#	#	#	#	#	VV[6:0]	00H
36	VCOM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82H
		0	1	--	#	#	#	#	#	#	#	VDCS[6:0]	00H
37	Partial Window (PTL)	0	0	1	0	0	1	0	0	0	0		90H
		0	1	--	--	--	--	--	--	--	#	HRST[8:3]	00H
		0	1	#	#	#	#	#	0	0	0		00H
		0	1	--	--	--	--	--	--	--	#	HRED[8:3]	00H
		0	1	#	#	#	#	#	1	1	1		07H
		0	1	--	--	--	--	--	--	--	#	VRST[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
		0	1	--	--	--	--	--	--	--	#	VRED[8:0]	00H
		0	1	#	#	#	#	#	#	#	#		00H
		0	1	--	--	--	--	--	--	--	#	PT_SCAN	01H
38	Partial In (PTIN)	0	0	1	0	0	1	0	0	0	1		91H
39	Partial Out (PTOUT)	0	0	1	0	0	1	0	0	1	0		92H
40	Program Mode (PGM)	0	0	1	0	1	0	0	0	0	0		A0H
41	Active Programming (APG)	0	0	1	0	1	0	0	0	0	1		A1H
42	Read OTP (ROTP)	0	0	1	0	1	0	0	0	1	0		A2H
		1	1	--	--	--	--	--	--	--	--	Read Dummy	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = 000h	N/A

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
		1	1	:	:	:	:	:	:	:	:	:	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = n	N/A
43	Cascade Setting (CCSET)	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**		**E0H**
		0	1	--	--	--	--	--	--	#	#	TSFIX, CCEN	00H
44	Power Saving (PWS)	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**		**E3H**
		0	1	#	#	#	#	#	#	#	#	VCOM_W[3:0], SD_W[3:0]	00H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
45	LVD Voltage Select (LVSEL)	0	0	1	1	1	0	0	1	0	0		E4H
		0	1	--	--	--	--	--	--	#	#	LVD_SEL[1:0]	03H
46	Force Temperature (TSSET)	0	0	1	1	1	0	0	1	0	1		E5H
		0	1	#	#	#	#	#	#	#	#	TS_SET[7:0]	00H

Note: (1) All other register addresses are invalid or reserved by UltraChip, and should NOT be used.

(2) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.

(3) Commands are processed on the 'stop' condition of the interface.

(4) Registers marked 'W/R' can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.

COMMAND DESCRIPTION

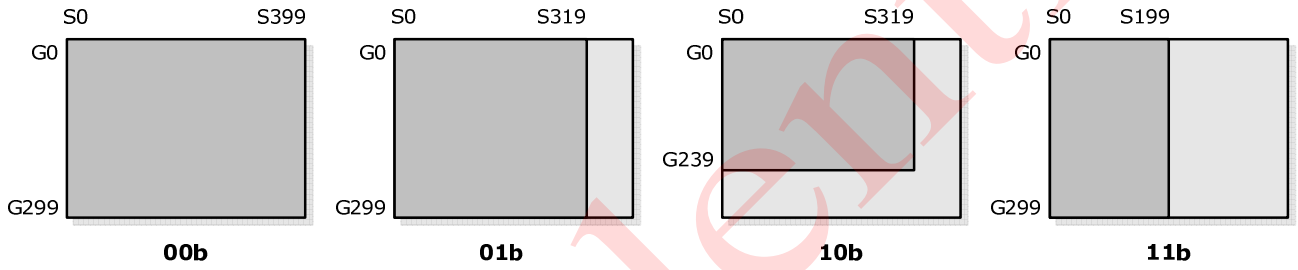
W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: –: Don't Care

(1) PANEL SETTING (PSR) (REGISTER: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting the panel	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	00H
	0	1	RES1	RES0	REG	KW/R	UD	SHL	SHD_N	RST_N	0FH
	0	1	-	-	-	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	0DH

RES[1:0]: Display Resolution setting (source x gate)

00b: 400x300 (Default) Active source channels: S0 ~ S399. Active gate channels: G0 ~ G299.
01b: 320x300 Active source channels: S0 ~ S319. Active gate channels: G0 ~ G299.
10b: 320x240 Active source channels: S0 ~ S319. Active gate channels: G0 ~ G239.
11b: 200x300 Active source channels: S0 ~ S199. Active gate channels: G0 ~ G299.



REG: LUT selection

0: LUT from OTP. (Default)
1: LUT from register.

KW/R: Black / White / Red

0: Pixel with Black/White/Red, KWR mode. (Default)
1: Pixel with Black/White, KW mode.

UD: Gate Scan Direction

0: Scan down. First line to Last line: Gn-1 → Gn-2 → Gn-3 → … → G0
1: Scan up. (Default) First line to Last line: G0 → G1 → G2 → … … . → Gn-1

SHL: Source Shift Direction

0: Shift left. First data to Last data: Sn-1 → Sn-2 → Sn-3 → … → S0
1: Shift right. (Default) First data to Last data: S0 → S1 → S2 → … … . → Sn-1

SHD_N: Booster Switch

0: Booster OFF
1: Booster ON (Default)

When SHD_N becomes LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF. And Source/Gate/Border/VCOM will be released to floating.

RST_N: Soft Reset

0: Reset. Booster OFF, Register data are set to their default values, all drivers will be reset, and all functions will be disabled. Source/Gate/Border/VCOM will be released to floating. After soft reset is transmitted, the internal operation needs at least 50uS to execute. During this period of time, the BUSY_N pin keeps low and any command will be ignored.

1: No effect (Default).

VCMZ: VCOM Hi-Z state function

0: No effect (Default)

1 : VCOM is always floating

TS_AUTO: Temperature sensor will be activated automatically one time.

0: No effect (Default)

1: Before enabling booster, Temperature Sensor will be activated automatically one time.

TIEG: VGL state function

0: No effect (Default)

1 : After power off booster, VGL will be tied to GND.

NORG: VCOM state during refreshing display

0: No effect (Default)

1: Expect refreshing display, VCOM is tied to GND.

VC_LUTZ: VCOM state during refreshing display

0: No effect (Default)

1: After refreshing display, the output of VCOM is set to floating automatically.

Note: Priority of Vcom setting: VCMZ > EOPT > NORG > VC_LUTZ

(2) POWER SETTING (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	01H
	0	1	-	-	-	BD_EN	-	-	VDS_EN	VDG_EN	03H
	0	1	-	-	-	VCOM_SLEW	VGHL_LV[3:0]				10H
	0	1	-	-	VSH[5:0]						3FH
	0	1	-	-	VSL[5:0]						3FH
	0	1	OPTEN	VDHR[6:0]							0DH

BD_EN: Border LDO enable control
0 : Border LDO disable (Default)
Border level selection: 00b: VCOM 01b: VSH 10b: VSL 11b: VDHR
1 : Border LDO enable
Border level selection: 00b: VCOM 01b: VBH(VCOM-VSL) 10b: VBL(VCOM-VSH) 11b: VDHR

VDS_EN: Source power selection
0 : External source power from VSH/VSL/VDHR pins
1 : Internal DC/DC function for generating VSH/VSL/VDHR. (Default)

VDG_EN: Gate power selection
0 : External gate power from VGH/VGL pins
1 : Internal DC/DC function for generating VGH/VGL. (Default)

VCOM_SLEW: VCOM slew rate selection for voltage transition. The value is fixed at **1.**

VGHL_LV[3:0]: VGH / VGL Voltage Level selection.

VGHL_LV	VGHL Voltage Level
0000 (Default)	VGH=20V, VGL= -20V
0001	VGH=19V, VGL= -19V
0010	VGH=18V, VGL= -18V
0011	VGH=17V, VGL= -17V
0100	VGH=16V, VGL= -16V
0101	VGH=15V, VGL= -15V
0110	VGH=14V, VGL= -14V
0111	VGH=13V, VGL= -13V
1000	VGH=12V, VGL= -12V
1001	VGH=11V, VGL= -11V
1010	VGH=10V, VGL= -10V

VSH[5:0]: Internal VSH power selection for B/W pixel.(**Default value: 111111b**)

VSH	Voltage	VSH	Voltage	VSH	Voltage	VSH	Voltage
00 0000	2.4 V	01 0000	5.6 V	10 0000	8.8 V	11 0000	12.0 V
00 0001	2.6 V	01 0001	5.8 V	10 0001	9.0 V	11 0001	12.2 V
00 0010	2.8 V	01 0010	6.0 V	10 0010	9.2 V	11 0010	12.4 V
00 0011	3.0 V	01 0011	6.2 V	10 0011	9.4 V	11 0011	12.6 V
00 0100	3.2 V	01 0100	6.4 V	10 0100	9.6 V	11 0100	12.8 V
00 0101	3.4 V	01 0101	6.6 V	10 0101	9.8 V	11 0101	13.0 V
00 0110	3.6 V	01 0110	6.8 V	10 0110	10.0V	11 0110	13.2 V
00 0111	3.8 V	01 0111	7.0 V	10 0111	10.2 V	11 0111	13.4 V
00 1000	4.0 V	01 1000	7.2 V	10 1000	10.4 V	11 1000	13.6 V
00 1001	4.2 V	01 1001	7.4 V	10 1001	10.6 V	11 1001	13.8 V
00 1010	4.4 V	01 1010	7.6 V	10 1010	10.8 V	11 1010	14.0 V
00 1011	4.6 V	01 1011	7.8 V	10 1011	11.0 V	11 1011	14.2 V
00 1100	4.8 V	01 1100	8.0 V	10 1100	11.2 V	11 1100	14.4 V
00 1101	5.0 V	01 1101	8.2V	10 1101	11.4 V	11 1101	14.6 V
00 1110	5.2 V	01 1110	8.4 V	10 1110	11.6 V	11 1110	14.8 V
00 1111	5.4 V	01 1111	8.6 V	10 1111	11.8 V	**11 1111**	**15.0 V**

VSL[5:0]: Internal VSL power selection for B/W pixel. (**Default value: 111111b**)

VSL	Voltage	VSL	Voltage	VSL	Voltage	VSL	Voltage
00 0000	-2.4 V	01 0000	-5.6 V	10 0000	-8.8 V	11 0000	-12.0 V
00 0001	-2.6 V	01 0001	-5.8 V	10 0001	-9.0 V	11 0001	-12.2 V
00 0010	-2.8 V	01 0010	-6.0 V	10 0010	-9.2 V	11 0010	-12.4 V
00 0011	-3.0 V	01 0011	-6.2 V	10 0011	-9.4 V	11 0011	-12.6 V
00 0100	-3.2 V	01 0100	-6.4 V	10 0100	-9.6 V	11 0100	-12.8 V
00 0101	-3.4 V	01 0101	-6.6 V	10 0101	-9.8 V	11 0101	-13.0 V
00 0110	-3.6 V	01 0110	-6.8 V	10 0110	-10.0V	11 0110	-13.2 V
00 0111	-3.8 V	01 0111	-7.0 V	10 0111	-10.2 V	11 0111	-13.4 V
00 1000	-4.0 V	01 1000	-7.2 V	10 1000	-10.4 V	11 1000	-13.6 V
00 1001	-4.2 V	01 1001	-7.4 V	10 1001	-10.6 V	11 1001	-13.8 V
00 1010	-4.4 V	01 1010	-7.6 V	10 1010	-10.8 V	11 1010	-14.0 V
00 1011	-4.6 V	01 1011	-7.8 V	10 1011	-11.0 V	11 1011	-14.2 V
00 1100	-4.8 V	01 1100	-8.0 V	10 1100	-11.2 V	11 1100	-14.4 V
00 1101	-5.0 V	01 1101	-8.2V	10 1101	-11.4 V	11 1101	-14.6 V
00 1110	-5.2 V	01 1110	-8.4 V	10 1110	-11.6 V	11 1110	-14.8 V
00 1111	-5.4 V	01 1111	-8.6 V	10 1111	-11.8 V	**11 1111**	**-15.0 V**

VDHR[5:0]: Internal VDHR power selection for Red pixel. (**Default value: 001101b**)

VDHR	Voltage	VDHR	Voltage	VDHR	Voltage	VDHR	Voltage
000000	2.4 V	010000	5.6 V	100000	8.8 V	110000	12.0 V
000001	2.6 V	010001	5.8 V	100001	9.0 V	110001	12.2 V
000010	2.8 V	010010	6.0 V	100010	9.2 V	110010	12.4 V
000011	3.0 V	010011	6.2 V	100011	9.4 V	110011	12.6 V
000100	3.2 V	010100	6.4 V	100100	9.6 V	110100	12.8 V
000101	3.4 V	010101	6.6 V	100101	9.8 V	110101	13.0 V
000110	3.6 V	010110	6.8 V	100110	10.0 V	110110	13.2 V
000111	3.8 V	010111	7.0 V	100111	10.2 V	110111	13.4 V
001000	4.0 V	011000	7.2 V	101000	10.4 V	111000	13.6 V
001001	4.2 V	011001	7.4 V	101001	10.6 V	111001	13.8 V
001010	4.4 V	011010	7.6 V	101010	10.8 V	111010	14.0 V
001011	4.6 V	011011	7.8 V	101011	11.0 V	111011	14.2 V
001100	4.8 V	011100	8.0 V	101100	11.2 V	111100	14.4 V
001101	**5.0 V**	011101	8.2 V	101101	11.4 V	111101	14.6 V
001110	5.2 V	011110	8.4 V	101110	11.6 V	111110	14.8 V
001111	5.4 V	011111	8.6 V	101111	11.8 V	111111	15.0 V

OPTEN: 1 enable step-0.1V voltage selection.

VDHR	Voltage	VDHR	Voltage	VDHR	Voltage	VDHR	Voltage
1000 0000	2.4 V	1010 0000	5.6 V	1100 0000	8.8 V	1110 0000	12 V
1000 0001	2.5 V	1010 0001	5.7 V	1100 0001	8.9 V	1110 0001	12.1 V
1000 0010	2.6 V	1010 0010	5.8 V	1100 0010	9.0 V	1110 0010	12.2 V
1000 0011	2.7 V	1010 0011	5.9 V	1100 0011	9.1 V	1110 0011	12.3 V
1000 0100	2.8 V	1010 0100	6.0 V	1100 0100	9.2 V	1110 0100	12.4 V
1000 0101	2.9 V	1010 0101	6.1 V	1100 0101	9.3 V	1110 0101	12.5 V
1000 0110	3.0 V	1010 0110	6.2 V	1100 0110	9.4 V	1110 0110	12.6 V
1000 0111	3.1 V	1010 0111	6.3 V	1100 0111	9.5 V	1110 0111	12.7 V
1000 1000	3.2 V	1010 1000	6.4 V	1100 1000	9.6 V	1110 1000	12.8 V
1000 1001	3.3 V	10101001	6.5 V	1100 1001	9.7 V	1110 1001	12.9 V
1000 1010	3.4 V	1010 1010	6.6 V	1100 1010	9.8 V	1110 1010	13.0 V
1000 1011	3.5 V	1010 1011	6.7 V	1100 1011	9.9 V	1110 1011	13.1 V
1000 1100	3.6 V	1010 1100	6.8 V	1100 1100	10.0 V	1110 1100	13.2 V
1000 1101	3.7 V	1010 1101	6.9 V	1100 1101	10.1 V	1110 1101	13.3 V
1000 1110	3.8 V	1010 1110	7.0 V	1100 1110	10.2 V	1110 1110	13.4 V
1000 1111	3.9 V	1010 1111	7.1 V	1100 1111	10.3 V	1110 1111	13.5 V
1001 0000	4.0 V	1011 0000	7.2 V	1101 0000	10.4 V	1111 0000	13.6 V
1001 0001	4.1 V	1011 0001	7.3 V	1101 0001	10.5 V	1111 0001	13.7 V
1001 0010	4.2 V	1011 0010	7.4 V	1101 0010	10.6 V	1111 0010	13.8 V
1001 0011	4.3 V	1011 0011	7.5 V	1101 0011	10.7 V	1111 0011	13.9 V
1001 0100	4.4 V	1011 0100	7.6 V	1101 0100	10.8 V	1111 0100	14.0 V
1001 0101	4.5 V	1011 0101	7.7 V	1101 0101	10.9 V	1111 0101	14.1 V
1001 0110	4.6 V	1011 0110	7.8 V	1101 0110	11.0 V	1111 0110	14.2 V
1001 0111	4.7 V	1011 0111	7.9 V	1101 0111	11.1 V	1111 0111	14.3 V
1001 1000	4.8 V	1011 1000	8.0 V	1101 1000	11.2 V	1111 1000	14.4 V
1001 1001	4.9 V	1011 1001	8.1 V	1101 1001	11.3 V	1111 1001	14.5 V
1001 1010	5.0 V	1011 1010	8.2 V	1101 1010	11.4 V	1111 1010	14.6 V
1001 1011	5.1 V	1011 1011	8.3 V	1101 1011	11.5 V	1111 1011	14.7 V
1001 1100	5.2 V	1011 1100	8.4 V	11011100	11.6 V	1111 1100	14.8 V
1001 1101	5.3 V	1011 1101	8.5 V	1101 1101	11.7 V	1111 1101	14.9 V
1001 1110	5.4 V	1011 1110	8.6 V	1101 1110	11.8 V	1111 1110	15.0 V
1001 1111	5.5 V	1011 1111	8.7 V	1101 1111	11.9 V		

(3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning OFF the power	0	0	0	0	0	0	0	0	1	0	02H

After the Power OFF command, the driver will be powered OFF. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode. Source/Gate/Border/VCOM will be released to floating.

(4) POWER OFF SEQUENCE SETTING (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1	03H
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-	00H

T_VDS_OFF[1:0]: Source to gate power off interval time.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

(5) POWER ON (PON) (REGISTER: R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning ON the power	0	0	0	0	0	0	0	1	0	0	04H

After the Power ON command, the driver will be powered ON. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUSY_N signal will return to high.

(6) POWER ON MEASURE (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	0	0	0	0	0	1	0	1	05H

This command enables the internal bandgap, which will be cleared by the next POF.

(7) BOOSTER SOFT START (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	0	0	1	1	0	06H
	0	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	17H
	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	17H
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	17H

BTPHA[7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA[5:3]: Driving strength of phase A

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHA[2:0]: Minimum OFF time setting of GDR in phase A

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHB[7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHB[5:3]: Driving strength of phase B

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHB[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHC[5:3]: Driving strength of phase C

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4
100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHC[2:0]: Minimum OFF time setting of GDR in phase C

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

(8) DEEP SLEEP (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Deep Sleep	0	0	0	0	0	0	0	1	1	1	07H
	0	1	1	0	1	0	0	1	0	1	A5H

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

(9) DATA START TRANSMISSION 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	0	0	10H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	-
	0	1	:	:	:	:	:	:	:	:	-
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	-

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes “OLD” data to SRAM.

In KWR mode, this command writes “B/W” data to SRAM.

In Program mode, this command writes “OTP” data to SRAM for programming.

(10) DATA STOP (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	0	0	0	1	0	0	0	1	11H
	1	1	data_flag	-	-	-	-	-	-	-	00H

Check the completeness of data. If data is complete, start to refresh display.

Data_flag: Data flag of receiving user data.

0: Driver didn’t receive all the data.
1: Driver has already received all the one-frame data (DTM1 and DTM2).

After “Data Start” (R10h) or “Data Stop” (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY_N signal will become “0”.

(11) DISPLAY REFRESH (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Refreshing the display	0	0	0	0	0	1	0	0	1	0	12H

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY_N signal will become “0” and the refreshing of panel starts.

The waiting interval form BUSY_N falling to the first FLG command must be larger than 200uS.

(12) DATA START TRANSMISSION 2 (DTM2) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	13H
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8	-
	0	1	:	:	:	:	:	:	:	:	-
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)	-

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes “NEW” data to SRAM.

In KWR mode, this command writes “RED” data to SRAM.

(13) AUTO SEQUENCE (AUTO) (R17H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Auto Sequence	0	0	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**1**	17H
	0	1	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	A5H

The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host’s control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.

AUTO (0x17) + Code(0xA5) = (PON → DRF → POF)

AUTO (0x17) + Code(0xA7) = (PON → DRF → POF → DSLP)

(14) VCOM LUT (LUTC) (R20H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-up Table for VCOM (57-byte command, structure of bytes 2~8 repeated 8 times)	0	0	0	0	1	0	0	0	0	0	20H
	0	1	Group Repeat Time [7:0]								00H
	0	1	Level Select 1-1[1:0]		Frame number 1-1 [5:0]						-
	0	1	Level Select 1-2[1:0]		Frame number 1-2 [5:0]						-
	0	1	Level Select 2-1[1:0]		Frame number 2-1 [5:0]						-
	0	1	Level Select 2-2[1:0]		Frame number 2-2 [5:0]						-
	0	1	State 1 repeat times [7:0]								-
	0	1	State 2 repeat times [7:0]								-

This command stores VCOM Look-Up Table with 8 groups of data. This LUT includes 8 kinds of groups; each group is of 7 bytes. Each group is divied to 2states and group repeat number. Each state made up 2 phases and each phase is combined with repeat time, level selection and frame number.

Bytes 2, 9, 16, 23 , 30,… :

Group repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

Bytes 3~6, 10~13, 17~20, 24~27, 31~34……:

[D7:D6] Level selection

00b: VCOM_DC

01b: VSH+VCOM_DC (VCOMH)

10b: VSL+VCOM_DC (VCOML)

11b: Floating

[D5:D0] Number of Frames (state1 & state2)

00 0000b: 0 time

: :

: :

11 1111b: 63 times

Bytes 7~8, 14~15, 21~22, 28~29, 35~36,..:

State 1 & State 2 repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: 1 ~ 255times

If KW/R=0 (KWR mode), all 8 groups are used.

If KW/R=1 (KW mode), only 6 groups are used.

(15) W2W LUT (LUTWW) (R21H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build White Look-up Table for W2W (43-byte command, structure of bytes 2~8 repeated 6 times)	0	0	0	0	1	0	0	0	0	1	21H
	0	1	Group Repeat Time [7:0]								-
	0	1	Level Select 1-1[1:0]		Frame number 1-1 [5:0]						-
	0	1	Level Select 1-2[1:0]		Frame number 1-2 [5:0]						-
	0	1	Level Select 2-1[1:0]		Frame number 2-1 [5:0]						-
	0	1	Level Select 2-2[1:0]		Frame number 2-2 [5:0]						-
	0	1	State 1 repeat times [7:0]								-
	0	1	State 2 repeat times [7:0]								-

This command stores LUTW2W Look-Up Table with 6 groups of data. This LUT includes 6 kinds of groups; each group is of 7 bytes. Each group is divied to 2states and group repeat number. Each state made up 2 phases and each phase is combined with repeat time, level selection and frame number.

Bytes 2, 9, 16, 23 , 30,… :

Group repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

Bytes 3~6, 10~13, 17~20, 24~27, 31~34……:

[D7:D6] Level selection

00b: 0V

01b: VSH

10b: VSL

11b: VDHR

[D5:D0] Number of Frames (state1 & state2)

00 0000b: 0 time

: :

: :

11 1111b: 63 times

Bytes 7~8, 14~15, 21~22, 28~29, 35~36,..:

State 1 & State 2 repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: 1 ~ 255times

If KW/R=0 (KWR mode), LUTWW is not used.

If KW/R=1 (KW mode), LUTWW is used.

(16) K2W LUT (LUTKW / LUTR) (R22H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Build Look-up Table for K2W or Red (57-byte command, structure of bytes 2~8 repeated 8 times)	0	0	0	0	1	0	0	0	0	0	22H
	0	1	Group Repeat Time [7:0]								-
	0	1	Level Select 1-1[1:0]		Frame number 1-1 [5:0]						-
	0	1	Level Select 1-2[1:0]		Frame number 1-2 [5:0]						-
	0	1	Level Select 2-1[1:0]		Frame number 2-1 [5:0]						-
	0	1	Level Select 2-2[1:0]		Frame number 2-2 [5:0]						-
	0	1	State 1 repeat times [7:0]								-
	0	1	State 2 repeat times [7:0]								-

This command stores LUTKW / LUTR Look-Up Table with 8 groups of data. This LUT includes 8 kinds of groups; each group is of 7 bytes. Each group is divied to 2states and group repeat number. Each state made up 2 phases and each phase is combined with repeat time, level selection and frame number.

Bytes 2, 9, 16, 23 , 30,… :

Group repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: Repeat 1 ~ 255times

Bytes 3~6, 10~13, 17~20, 24~27, 31~34……:

[D7:D6] Level selection

00b: 0V

01b: VSH

10b: VSL

11b: VDHR

[D5:D0] Number of Frames (state1 & state2)

00 0000b: 0 time

: :

11 1111b: 63 times

Bytes 7~8, 14~15, 21~22, 28~29, 35~36,..:

State 1 & State 2 repeat times

0000 0000b: No repeat

0000 0001b ~ 1111 1111b: 1 ~ 255times

If KW/R=0 (KWR mode), all 8 groups are used.

If KW/R=1 (KW mode), only 6 groups are used.

(17) W2K LUT (LUTWK / LUTW) (R23H)

This command builds Look-up Table for White-to-Black. Please refer to W2W LUT (LUTWW) for similar definition details.

Regardless of KW/R=0 or KW/R=1, LUTWK/LUTW is used.

(18) K2K LUT (LUTKK / LUTK) (R24H)

This command builds Look-up Table for Black-to-Black. Please refer to W2W LUT (LUTWW) for similar definition details.

Regardless of KW/R=0 or KW/R=1, LUTKK/LUTK is used.

Note: All LUTs are independent of each other and could be deal with separately.If waveform time is different for each LUT , IC would elect longest LUT as refresh time and fill 0 (GND) to remaining refresh time for other LUT.

(19) LUT OPTION (LUTOPT) (R2AH)

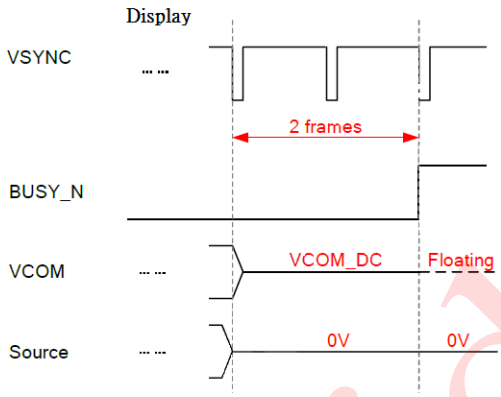
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
LUT Option	0	0	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	2AH
	0	1	EOPT	ESO	-	-	-	-	-	-	00H
	0	1	STATE_XON[7:0]								00H
	0	1	STATE_XON[15:8]								00H
	0	1	GROUP_KWE[7:0]								FFH
	0	1	-	-	-	-	-	-	ATRED	NORED	00H

This command sets XON and the several options of KWR mode's LUT. .

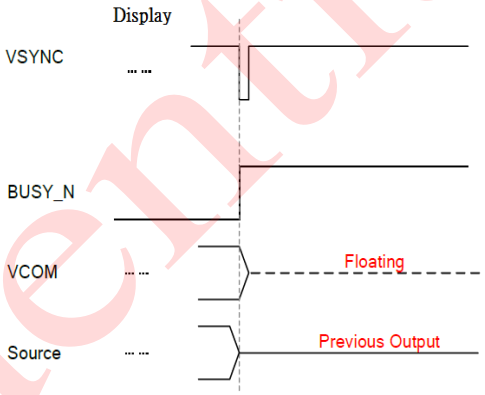
EOPT: LUT sequence option 1

0: Disable 1: Enable

EOPT=0



EOPT=1



ESO: LUT sequence option 2

STATE_XON[15:0]:

All Gate ON (Each bit controls one state, STATE_XON [0] for state-1, STATE_XON [1] for State-2 .....)

0000 0000 0000 0000b: no All-Gate-ON

0000 0000 0000 0001b: Group-1/State-1 All-Gate-ON

0000 0000 0000 0010b: Group-1/State-1 and Group-1/State2 All-Gate-ON

GROUP_KWE[7:0]:

The control bits are only available when KW/R=0 (KWR mode) and (ATRED | NORED)=1

There are only 8 groups in the K/W LUT. Each bit controls one group.

1111 1111b: all groups are executed sequentially.

1111 1110b: only Group-1 is bypassed.

1111 1100b: Group-1 and Group-2 are bypassed.

: :

ATRED: Automatic mode. The option is only available when KW/R=0

NORED: No Red data. The option is only available when KW/R=0

(20) PLL CONTROL (PLL) (R30H)

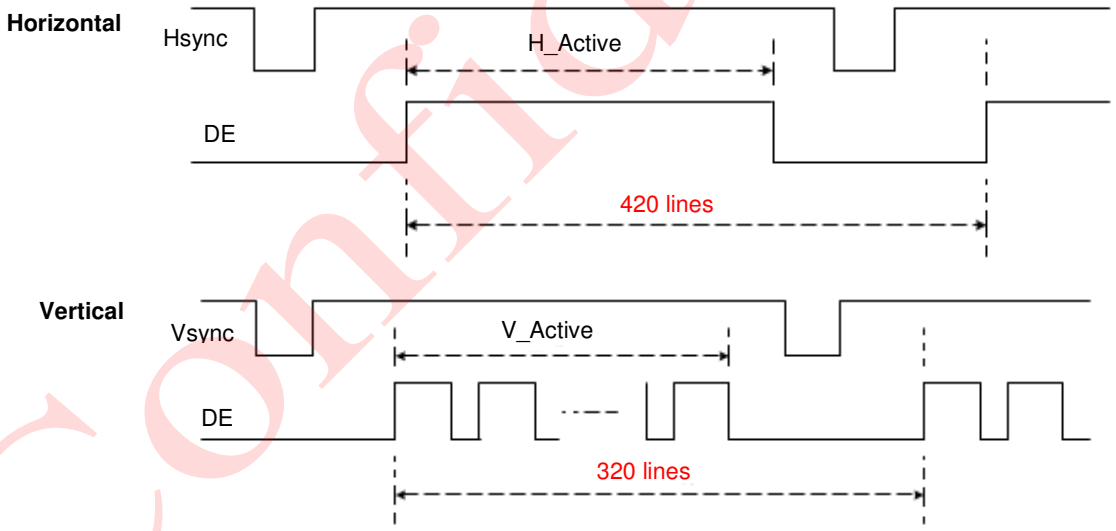
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Controlling PLL	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	30H
	0	1	-	-	-	FRS[4:0]					09H

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

FMR[4:0]: Frame rate setting

FRS	Frame rate
00000	5Hz
00001	10Hz
00010	15Hz
00011	20Hz
00100	25Hz
00101	30Hz
00110	35Hz
00111	40Hz
01000	45Hz
01001	**50Hz**
01010	55Hz
01011	60Hz
01100	65Hz
01101	70Hz
01110	75Hz
01111	80Hz

FRS	Frame rate
10000	85Hz
10001	90Hz
10010	95Hz
10011	100Hz
10100	105Hz
10101	110Hz
10110	115Hz
10111	120Hz
11000	130Hz
11001	140Hz
11010	150Hz
11011	160Hz
11100	170Hz
11101	180Hz
11110	190Hz
11111	200Hz



(21) TEMPERATURE SENSOR CALIBRATION (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	40H
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0	00H
	1	1	D2	D1	D0	-	-	-	-	-	00H

This command enables internal or external temperature sensor, and reads the result.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temperature (°C)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
1110_1110	-18
1110_1111	-17
1111_0000	-16
1111_0001	-15
1111_0010	-14
1111_0011	-13
1111_0100	-12
1111_0101	-11
1111_0110	-10
1111_0111	-9
1111_1000	-8
1111_1001	-7
1111_1010	-6
1111_1011	-5
1111_1100	-4
1111_1101	-3
1111_1110	-2
1111_1111	-1

TS[7:0]/D[10:3]	Temperature(°C)
0000_0000	**0**
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
0000_0111	7
0000_1000	8
0000_1001	9
0000_1010	10
0000_1011	11
0000_1100	12
0000_1101	13
0000_1110	14
0000_1111	15
0001_0000	16
0001_0001	17
0001_0010	18
0001_0011	19
0001_0100	20
0001_0101	21
0001_0110	22
0001_0111	23
0001_1000	24

TS[7:0]/D[10:3]	Temperature(°C)
0001_1001	25
0001_1010	26
0001_1011	27
0001_1100	28
0001_1101	29
0001_1110	30
0001_1111	31
0010_0000	32
0010_0001	33
0010_0010	34
0010_0011	35
0010_0100	36
0010_0101	37
0010_0110	38
0010_0111	39
0010_1000	40
0010_1001	41
0010_1010	42
0010_1011	43
0010_1100	44
0010_1101	45
0010_1110	46
0010_1111	47
0011_0000	48
0011_0001	49

(22) TEMPERATURE SENSOR ENABLE (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enable Temperature Sensor /Offset	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	41H
	0	1	TSE	-	-	-	TO[3:0]				00H

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (default) 1: Disable; using external sensor.

TO[3:0]: Temperature offset.

TO[3:0]	Calculation
0000 b	**+0 (Default)**
0001	+1
0010	+2
0011	+3
0100	+4
0101	+5
0110	+6
0111	+7

TO[3:0]	Calculation
1000	-8
1001	-7
1010	-6
1011	-5
1100	-4
1101	-3
1110	-2
1111	-1

(23) TEMPERATURE SENSOR WRITE (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Write External Temperature Sensor	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	42H
	0	1	WATTR[7:0]								00H
	0	1	WMSB[7:0]								00H
	0	1	WLSB[7:0]								00H

This command writes the temperature sensed by the temperature sensor.

WATTR[7:6]: I²C Write Byte Number

00b : 1 byte (head byte only)
01b : 2 bytes (head byte + pointer)
10b : 3 bytes (head byte + pointer + 1st parameter)
11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

WATTR[5:3]: User-defined address bits (A2, A1, A0)

WATTR[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor

WLSB[7:0]: LSByte of write-data to external temperature sensor

(24) TEMPERATURE SENSOR READ (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read External Temperature Sensor	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	43H
	1	1	RMSB[7:0]								00H
	1	1	RLSB[7:0]								00H

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor

RLSB[7:0]: LSByte read data from external temperature sensor

(25) PANEL GLASS CHECK (PBC)

Action	R/W	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Check Panel Glass	W	0	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**	44H
	R	1	-	-	-	-	-	-	-	PSTA	00H

This command is used to enable panel check, and to disable after reading result.

PSTA: 0: Panel check fail (panel broken) 1: Panel check pass

(26) VCOM AND DATA INTERVAL SETTING (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Interval between VCOM and Data	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	50h
	0	1	VBD[1:0]		DDX[1:0]		CDI[3:0]				D7h

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

VBD[1:0]: Border data selection

KWR mode (KW/R=0)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTK
1 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	Floating

KW mode (KW/R=1)

DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	Floating
1 (Default)	00	Floating
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	Floating

DDX[1:0]: Data polality.

Under KWR mode (KW/R=0):

DDX[1] is for RED data.
DDX[0] is for B/W data,

DDX[1:0]	Data {Red, B/W}	LUT
00	00	LUTW
	01	LUTK
	10	LUTR
	11	LUTR
01 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTR

DDX[1:0]	Data {Red, B/W}	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTK
11	00	LUTR
	01	LUTR
	10	LUTK
	11	LUTW

Under KW mode (KW/R=1):

DDX[1]=0 is for KW mode with NEW/OLD,
DDX[1]=1 is for KW mode without NEW/OLD.

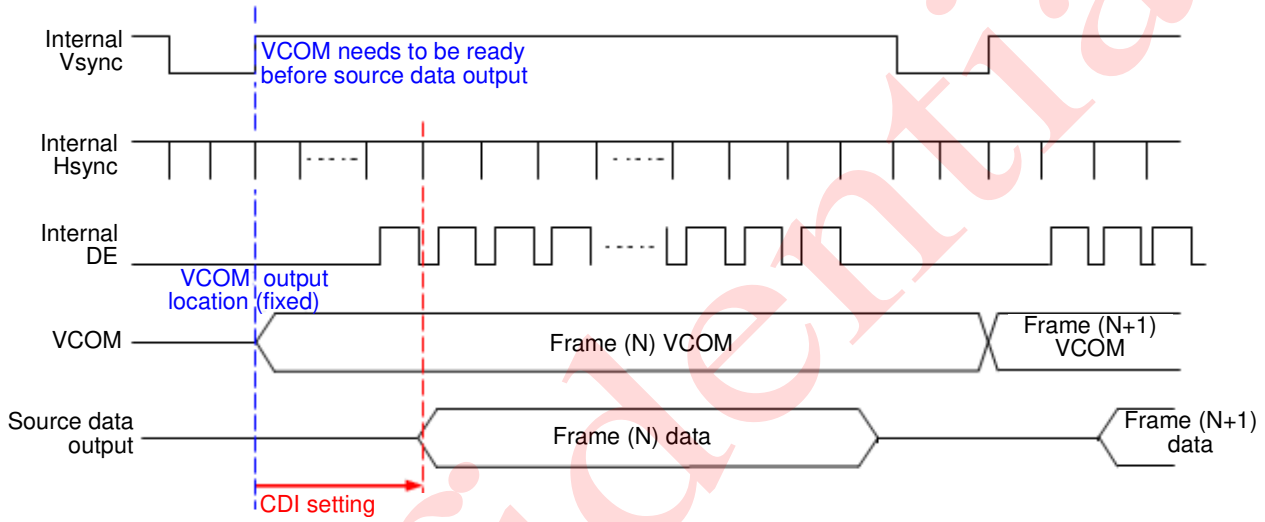
DDX[1:0]	Data {NEW, OLD}	LUT
00	00	LUTWW (0 → 0)
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (1 → 1)
01 (Default)	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTWW (1 → 1)

DDX[1:0]	Data {NEW}	LUT
10	0	LUTKW (1 → 0)
	1	LUTWK (0 → 1)
11	0	LUTWK (1 → 0)
	1	LUTKW (0 → 1)

CDI[3:0]: VCOM and data interval

CDI[3:0]	VCOM and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	**10 (Default)**

CDI[3:0]	VCOM and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



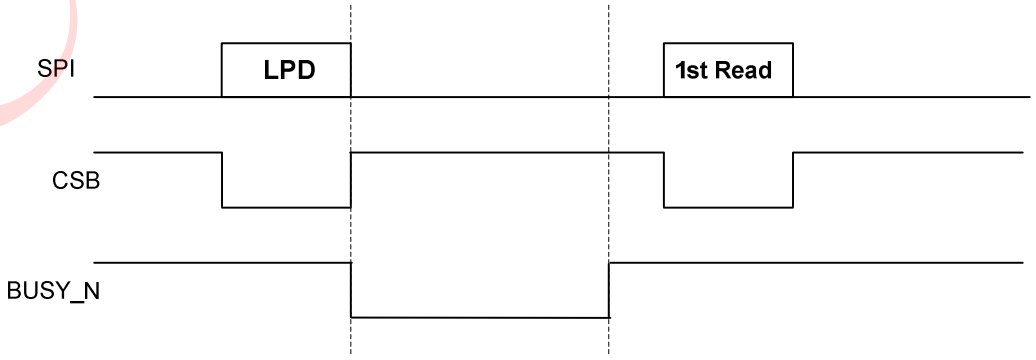
(27) LOW POWER DETECTION (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Detect Low Power	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	51h
	1	1	-	-	-	-	-	-	-	LPD	01h

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal Low Power Detection Flag

0: Low power input (V_{DD}<2.5V, selected by LVD_SEL[1:0] in command LVSEL)
1: Normal status (default)



(28) TCON SETTING (TCON) (R60H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Non-overlap Period	0	0	0	1	1	0	0	0	0	0	60h
	0	1	S2G[3:0]				G2S[3:0]				22h

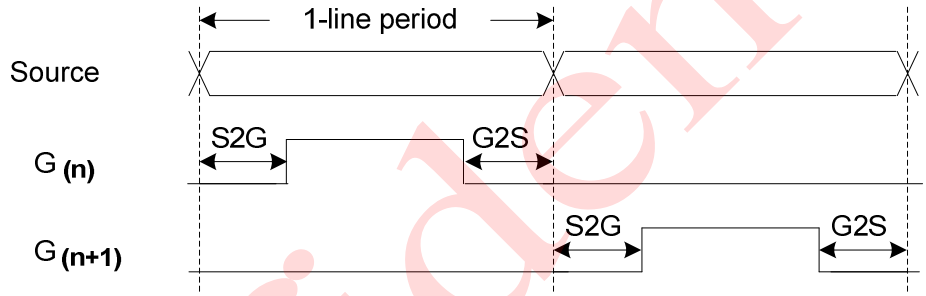
This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000 b	4
0001	8
0010	**12 (Default)**
0011	16
0100	20
0101	24
0110	28
0111	32

S2G[3:0] or G2S[3:0]	Period
1000 b	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	60
1111	64

Period Unit = 650 nS.



(29) RESOLUTION SETTING (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	61h
	0	1	-	-	-	-	-	-	-	HRES[8]	00h
	0	1	HRES[7:3]					**0**	**0**	**0**	00h
	0	1	-	-	-	-	-	-	-	VRES[8]	00h
	0	1	VRES[7:0]								00h

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[8:3]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Active channel calculation, assuming HRES[8:3]=0, VRES[8:0]=0:

Gate: First active gate = G0;
Last active gate = VRES[8:0] – 1

Source: First active source = S0;
Last active source = HRES[8:3]*8 - 1

Example: 128 (source) x 272 (gate), assuming HRES[8:3]=0, VRES[8:0]=0

Gate: First active gate = G0,
Last active gate = G271; (VRES[8:0] = 272, 272 - 1= 271)

Source: First active source = S0,
Last active source = S127; (HRES[8:3]=16, 16*8 – 1 = 127)

(30) GATE/SOURCE START SETTING (GSST) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Start	0	0	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**1**	65h
	0	1	-	-	-	-	-	-	-	HST[8]	00h
	0	1	HST[7:3]					**0**	**0**	**0**	00h
	0	1	-	-	-	-	-	-	-	VST[8]	00h
	0	1	VST[7:0]								00h

This command defines resolution start gate/source position.

HST[8:3]: Horizontal Display Start Position (Source)

VST[8:0]: Vertical Display Start Position (Gate)

Example : For 128(Source) x 240(Gate)
HST[8:3] = 4 (HST[8:0] = 4*8 = 32),
VST[8:0] = 32

Gate: First active gate = G32 (VST[8:0] = 32),
Last active gate = G271 (VST[8:0] = 32, VRES[8:0] = 240, 32+240-1=271)

Source: First active source = S32 (HST[8:0] = 32),
Last active source = S159 (HST[8:0] = 32, HRES[8:0] = 128, 32+128-1=159)

(31) REVISION (REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Chip Revision	0	0	0	1	1	1	0	0	0	0	70h
	1	1	RESERVED								FFh
	1	1	CHIP_REV[7:0]								07h
	1	1	LUT_REV[7:0]								FFh
	1	1	LUT_REV[15:8]								FFh
	1	1	LUT_REV[23:16]								FFh

The LUT_REV is read from OTP address =0x001A~0x001C / 0x0C1A~0x0C1C .

CHIP_REV[7:0]: Chip Revision, fixed at 0x07h.

(32) GET STATUS (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read Flags	0	0	0	1	1	1	0	0	0	1	71h
	1	1	-	PTL_ flag	I²C_ERR	I²C_ BUSYN	data_ flag	PON	POF	BUSY_N	13h

This command reads the IC status.

PTL_FLAG Partial display status (high: partial mode)

I²C_ERR: I²C master error status

I²C_BUSYN: I²C master busy status (low active)

data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY_N: Driver busy status (low active)

(33) CYCLIC REDUNDANCY CHECK (CRC) (R72H)

Action	R/W	A0	D7	D6	D5	D4	D3	D2	D1	D0	
Cyclic redundancy check	R	0	0	1	1	1	0	0	1	0	72H
	R	1	CRC_MSB[7:0]								FFH
	R	1	CRC_LSB[7:0]								FFH

This command reads Cyclic redundancy check(CRC) result.

The calculation only includes 0x0000~0x1FEF OTP data..

Polynomial = $x^{16} + x^{12} + x^5 + 1$, initial vaulte: 16'hFFFF

The result will be reset after this command.

CRC_MSB[7:0]: Most significant bits of CRC result

CRC_LSB[7:0]: Most significant bits of CRC result

(34) AUTO MEASURE VCOM (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	80h
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE	10h

This command controls automatic VCOM measurement mechanism.

AMVT[1:0]: Auto Measure VCOM Time

00b: 3s
01b: 5s (default)
10b: 8s
11b: 10s

XON: All Gate ON of AMV

0: Gate normally scan during Auto Measure VCOM period. (default)
1: All Gate ON during Auto Measure VCOM period.

AMVS: Source output of AMV

0: Source output 0V during Auto Measure VCOM period. (default)
1: Source output VDHR during Auto Measure VCOM period.

AMV: Analog signal

0: Get VCOM value with the VV command (R81h) (default)
1: Get VCOM value in analog signal. (External analog to digital converter)

AMVE: Auto Measure VCOM Enable (/Disable)

0: No effect (default)
1: Trigger auto VCOM sensing.

(35) VCOM VALUE (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure VCOM	0	0	1	0	0	0	0	0	0	1	81h
	1	1	-	-	VV[6:0]						00h

This command gets the VCOM value.

VV[6:0]: VCOM Value Output

VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)	VV [6:0]	VCOM Voltage (V)
0000000b	-0.1	0101011b	-4.4	1010110b	-8.7
0000001b	-0.2	0101100b	-4.5	1010111b	-8.8
0000010b	-0.3	0101101b	-4.6	1011000b	-8.9
0000011b	-0.4	0101110b	-4.7	1011001b	-9
0000100b	-0.5	0101111b	-4.8	1011010b	-9.1
0000101b	-0.6	0110000b	-4.9	1011011b	-9.2
0000110b	-0.7	0110001b	-5	1011100b	-9.3
0000111b	-0.8	0110010b	-5.1	1011101b	-9.4
0001000b	-0.9	0110011b	-5.2	1011110b	-9.5
0001001b	-1	0110100b	-5.3	1011111b	-9.6
0001010b	-1.1	0110101b	-5.4	1100000b	-9.7
0001011b	-1.2	0110110b	-5.5	1100001b	-9.8
0001100b	-1.3	0110111b	-5.6	1100010b	-9.9
0001101b	-1.4	0111000b	-5.7	1100011b	-10
0001110b	-1.5	0111001b	-5.8	1100100b	-10.1
0001111b	-1.6	0111010b	-5.9	1100101b	-10.2
0010000b	-1.7	0111011b	-6	1100110b	-10.3
0010001b	-1.8	0111100b	-6.1	1100111b	-10.4
0010010b	-1.9	0111101b	-6.2	1101000b	-10.5
0010011b	-2	0111110b	-6.3	1101001b	-10.6
0010100b	-2.1	0111111b	-6.4	1101010b	-10.7
0010101b	-2.2	1000000b	-6.5	1101011b	-10.8
0010110b	-2.3	1000001b	-6.6	1101100b	-10.9
0010111b	-2.4	1000010b	-6.7	1101101b	-11
0011000b	-2.5	1000011b	-6.8	1101110b	-11.1
0011001b	-2.6	1000100b	-6.9	1101111b	-11.2
0011010b	-2.7	1000101b	-7	1110000b	-11.3
0011011b	-2.8	1000110b	-7.1	1110001b	-11.4
0011100b	-2.9	1000111b	-7.2	1110010b	-11.5
0011101b	-3	1001000b	-7.3	1110011b	-11.6
0011110b	-3.1	1001001b	-7.4	1110100b	-11.7
0011111b	-3.2	1001010b	-7.5	1110101b	-11.8
0100000b	-3.3	1001011b	-7.6	1110110b	-11.9
0100001b	-3.4	1001100b	-7.7	1110111b	-12
0100010b	-3.5	1001101b	-7.8	1111000b	-12.1
0100011b	-3.6	1001110b	-7.9	1111001b	-12.2
0100100b	-3.7	1001111b	-8	1111010b	-12.3
0100101b	-3.8	1010000b	-8.1	1111011b	-12.4
0100110b	-3.9	1010001b	-8.2	1111100b	-12.5
0100111b	-4	1010010b	-8.3	1111101b	-12.6
0101000b	-4.1	1010011b	-8.4	1111110b	-12.7
0101001b	-4.2	1010100b	-8.5		
0101010b	-4.3	1010101b	-8.6		

(36) VCOM_DC SETTING (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set VCOM_DC	0	0	1	0	0	0	0	0	1	0	82h
	0	1	-	VDCS[6:0]							00h

This command sets VCOM_DC value

VDCS[6:0]: VCOM_DC Setting

VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)
0000000b	-0.1	0101011b	-4.4	1010110b	-8.7
0000001b	-0.2	0101100b	-4.5	1010111b	-8.8
0000010b	-0.3	0101101b	-4.6	1011000b	-8.9
0000011b	-0.4	0101110b	-4.7	1011001b	-9
0000100b	-0.5	0101111b	-4.8	1011010b	-9.1
0000101b	-0.6	0110000b	-4.9	1011011b	-9.2
0000110b	-0.7	0110001b	-5	1011100b	-9.3
0000111b	-0.8	0110010b	-5.1	1011101b	-9.4
0001000b	-0.9	0110011b	-5.2	1011110b	-9.5
0001001b	-1	0110100b	-5.3	1011111b	-9.6
0001010b	-1.1	0110101b	-5.4	1100000b	-9.7
0001011b	-1.2	0110110b	-5.5	1100001b	-9.8
0001100b	-1.3	0110111b	-5.6	1100010b	-9.9
0001101b	-1.4	0111000b	-5.7	1100011b	-10
0001110b	-1.5	0111001b	-5.8	1100100b	-10.1
0001111b	-1.6	0111010b	-5.9	1100101b	-10.2
0010000b	-1.7	0111011b	-6	1100110b	-10.3
0010001b	-1.8	0111100b	-6.1	1100111b	-10.4
0010010b	-1.9	0111101b	-6.2	1101000b	-10.5
0010011b	-2	0111110b	-6.3	1101001b	-10.6
0010100b	-2.1	0111111b	-6.4	1101010b	-10.7
0010101b	-2.2	1000000b	-6.5	1101011b	-10.8
0010110b	-2.3	1000001b	-6.6	1101100b	-10.9
0010111b	-2.4	1000010b	-6.7	1101101b	-11
0011000b	-2.5	1000011b	-6.8	1101110b	-11.1
0011001b	-2.6	1000100b	-6.9	1101111b	-11.2
0011010b	-2.7	1000101b	-7	1110000b	-11.3
0011011b	-2.8	1000110b	-7.1	1110001b	-11.4
0011100b	-2.9	1000111b	-7.2	1110010b	-11.5
0011101b	-3	1001000b	-7.3	1110011b	-11.6
0011110b	-3.1	1001001b	-7.4	1110100b	-11.7
0011111b	-3.2	1001010b	-7.5	1110101b	-11.8
0100000b	-3.3	1001011b	-7.6	1110110b	-11.9
0100001b	-3.4	1001100b	-7.7	1110111b	-12
0100010b	-3.5	1001101b	-7.8	1111000b	-12.1
0100011b	-3.6	1001110b	-7.9	1111001b	-12.2
0100100b	-3.7	1001111b	-8	1111010b	-12.3
0100101b	-3.8	1010000b	-8.1	1111011b	-12.4
0100110b	-3.9	1010001b	-8.2	1111100b	-12.5
0100111b	-4	1010010b	-8.3	1111101b	-12.6
0101000b	-4.1	1010011b	-8.4	1111110b	-12.7
0101001b	-4.2	1010100b	-8.5		
0101010b	-4.3	1010101b	-8.6		

(37) PARTIAL WINDOW (PTL) (R90H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Partial Window	0	0	1	0	0	0	0	0	1	0	90h
	0	1	-	-	-	-	-	-	-	HRST[8]	00h
	0	1	HRST[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	-	HRED[8]	00h
	0	1	HRED[7:3]					1	1	1	07h
	0	1	-	-	-	-	-	-	-	VRST[8]	00h
	0	1	VRST[7:0]								00h
	0	1	-	-	-	-	-	-	-	VRED[8]	00h
	0	1	VRED[7:0]								00h
	0	1	-	-	-	-	-	-	-	PT_SCAN	01h

This command sets partial window.

HRST[8:3]: Horizontal start channel bank. (value 00h~31h)

HRED[8:3]: Horizontal end channel bank. (value 00h~31h). HRED must be greater than HRST.

VRST[8:0]: Vertical start line. (value 000h~12Bh)

VRED[8:0]: Vertical end line. (value 000h~12Bh). VRED must be greater than VRST.

PT_SCAN: 0: Gates scan only inside of the partial window.
1: Gates scan both inside and outside of the partial window. (default)

(38) PARTIAL IN (PTIN) (R91H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial In	0	0	1	0	0	1	0	0	0	1	91h

This command makes the display enter partial mode.

(39) PARTIAL OUT (PTOUT) (R92H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial Out	0	0	1	0	0	1	0	0	1	0	92h

This command makes the display exit partial mode and enter normal mode.

(40) PROGRAM MODE (PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enter Program Mode	0	0	1	0	1	0	0	0	0	0	A0h

After this command is issued, the chip would enter the program mode.

After the programming procedure completed, a hardware reset is necessary for leaving program mode.

(41) ACTIVE PROGRAM (APG) (RA1H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Active Program OTP	0	0	1	0	1	0	0	0	0	1	A1h

After this command is transmitted, the programming state machine would be activated.

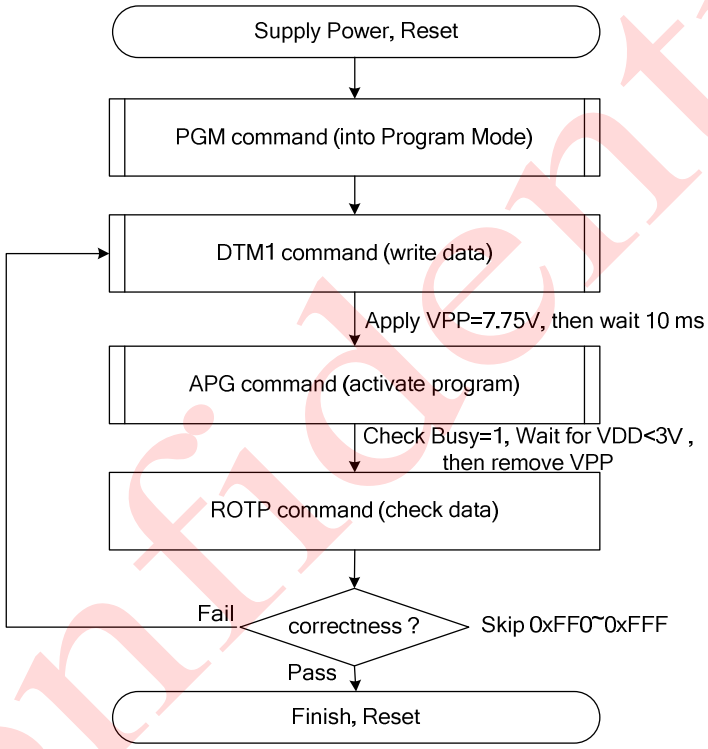
The BUSY_N flag would fall to 0 until the programming is completed.

(42) READ OTP DATA (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read OTP data for check	0	0	1	0	1	0	0	0	1	0	A2h
	1	1	Dummy								--
	1	1	The data of address 0x000 in the OTP								--
	1	1	The data of address 0x001 in the OTP								--
	1	1	:								--
	1	1	The data of address (n-1) in the OTP								--
	1	1	The data of address (n) in the OTP								--

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0xFFF.



The sequence of programming OTP.

(43) CASCADE SETTING (CCSET) (RE0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Cascade Option	0	0	1	1	1	0	0	0	0	0	E0h
	0	1	-	-	-	-	-	-	TSFIX	CCEN	00h

This command is used for cascade.

CCEN: Output clock enable/disable.

0: Output 0V at CL pin. (default)

1: Output clock at CL pin for slave chip.

TSFIX: Let the value of slave's temperature is same as the master's.

0: Temperature value is defined by internal temperature sensor / external LM75. (default)

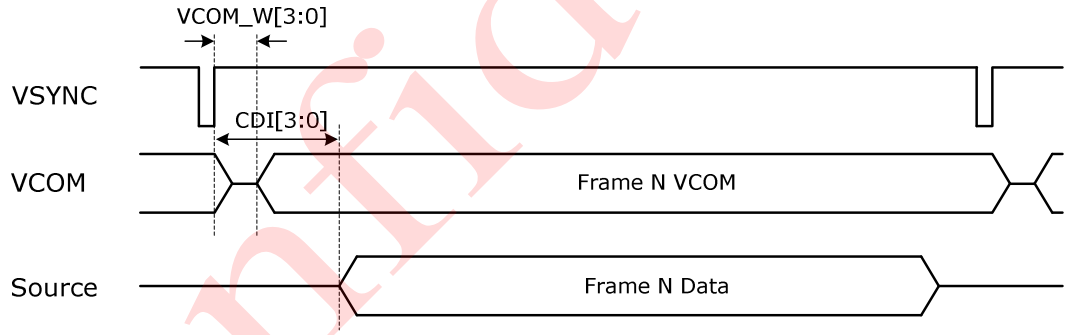
1: Temperature value is defined by TS_SET[7:0] registers.

(44) POWER SAVING (PWS) (RE3H)

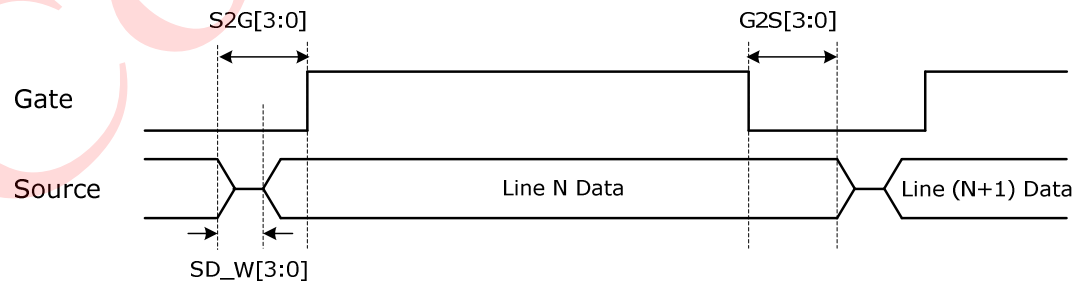
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power Saving for VCOM & Source	0	0	1	1	1	0	0	0	1	1	E3h
	0	1	VCOM_W[3:0]				SD_W[3:0]				00h

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 650nS)



(45) LVD VOLTAGE SELECT (LVSEL) (RE4H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Select LVD Voltage	0	0	1	1	1	0	0	1	0	0	E4h
	0	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h

LVD_SEL[1:0]: Low Power Voltage selection

LVD_SEL[1:0]	LVD value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V (default)

(46) FORCE TEMPERATURE (TSSET) (RE5H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Force Temperature Value for Cascade	0	0	1	1	1	0	0	1	0	1	E5h
	0	1	TS_SET[7:0]								00h

This command is used for cascade to fix the temperature value of master and slave chip.

HOST INTERFACES

UC8276 provides 3-wire/4-wire serial interface for command and display data transferred from the MCU. The serial interface supports 8-bit mode. Data can be input/output by clocks while the chip is active (CSB =LOW). While input, data are written in order from MSB at the clock rising edge. When too many parameters are input, the chip accepts only defined parameters, and ignores undefined ones.

BS	Interface	CSB	DC	SCL	SDA
High	3-wire SPI	Available	Fix to GND	Available	Available
Low	4-wire SPI	Available	Available	Available	Available

3 wire SPI format

Data / Command is recognized with the first bit transferred. Data are transferred in the unit of 9 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 9 bits. (The serial counter is reset at the rising edge of the CSB signal.)

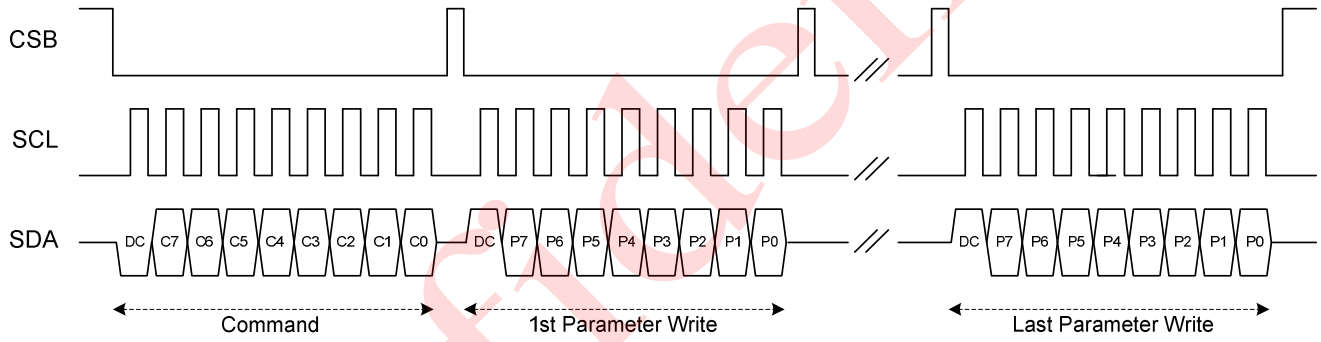


Figure: 3-wire SPI write operation

The MSB bit of data will be output at SDA pin after the 1st SCL falling edge, if the 1st input data at SDA is high. Only in the case of OTP data read, the 1st packet of output data are dummy data.

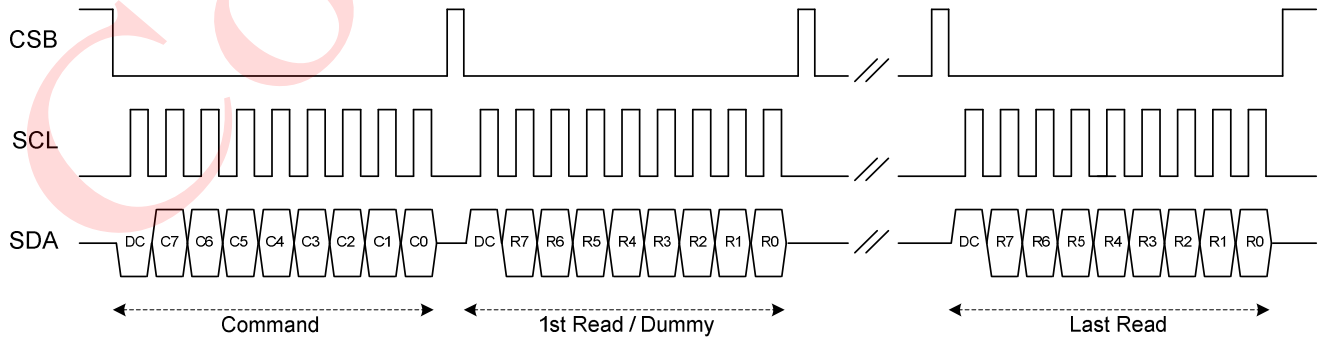


Figure: 3-wire SPI read operation

4 wire SPI format

Data / Command is recognized with DC pin. Data are transferred in the unit of 8 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 8 bits. (The serial counter is reset at the rising edge of the CSB signal.)

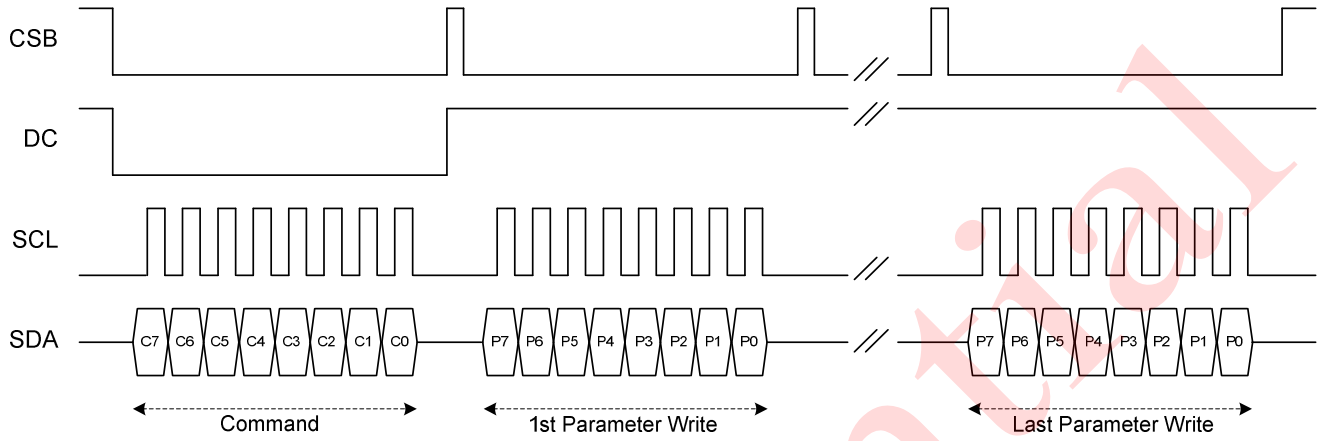


Figure: 4-wire SPI write operation

The MSB bit of data will be output at SDA pin after the CSB falling edge, if DC pin is High. Only in the case of OTP data read, the 1st packet of output data are dummy data.

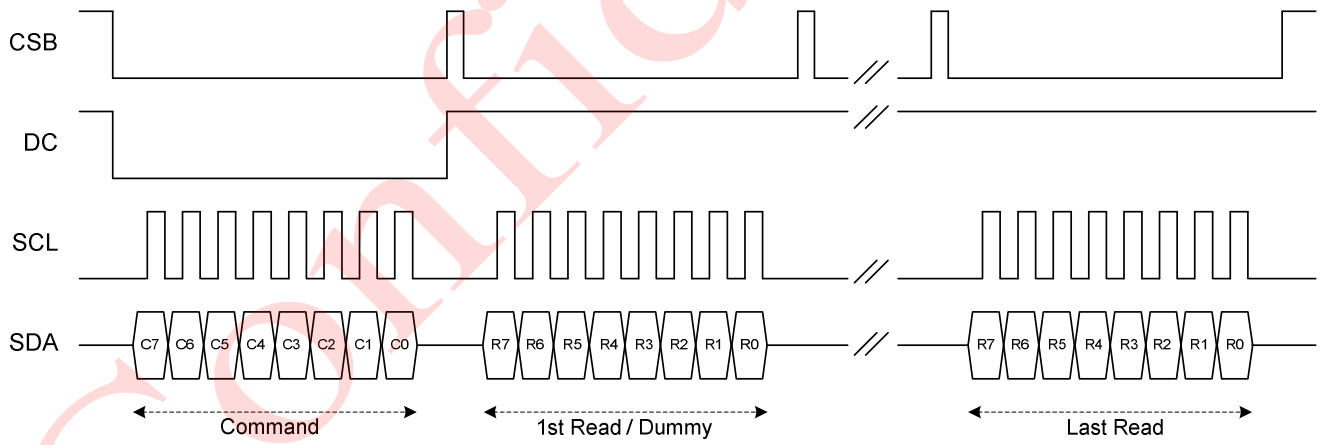
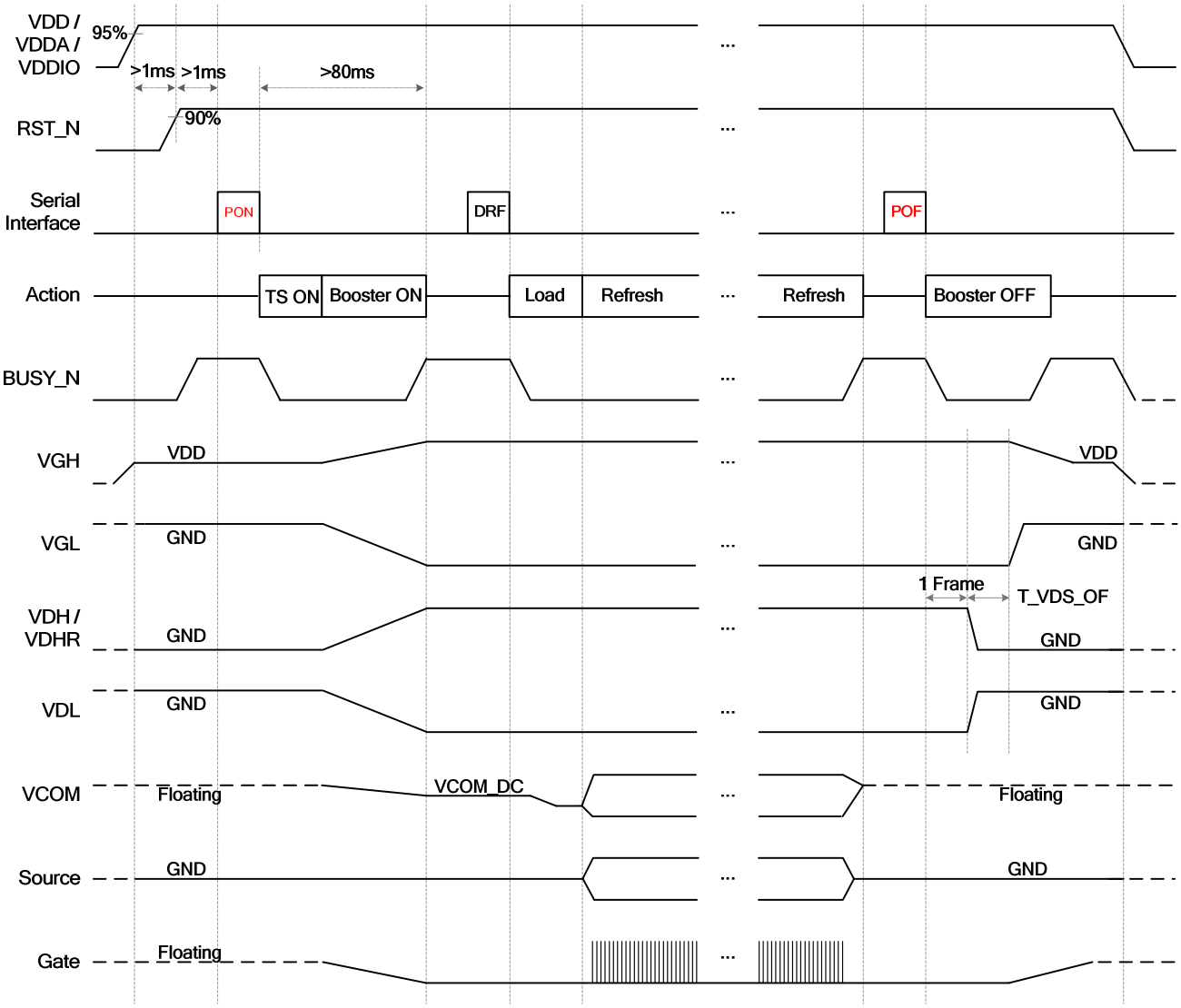


Figure: 4-wire SPI read operation

POWER MANAGEMENT

Power ON/OFF Sequence

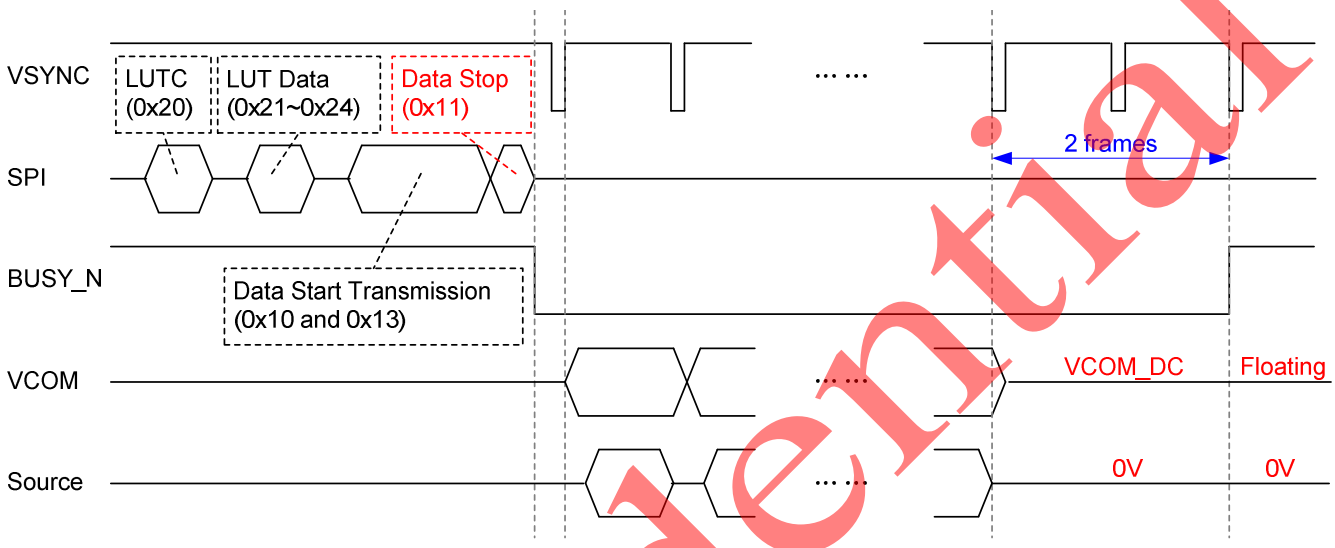
1. Temperature sensor will be activated automatically for one-time sensing before enabling booster.
2. After refreshing display, VCOM will be set to floating automatically.
3. In OTP mode (REG=0), the LUT in OTP will be copied to register automatically after the DSP/DRF command.
4. After RST_N rising, the waiting time for internal initial processing, greater than 1mS, is necessary. Any commands transmitted to chip during this time will be ignored.



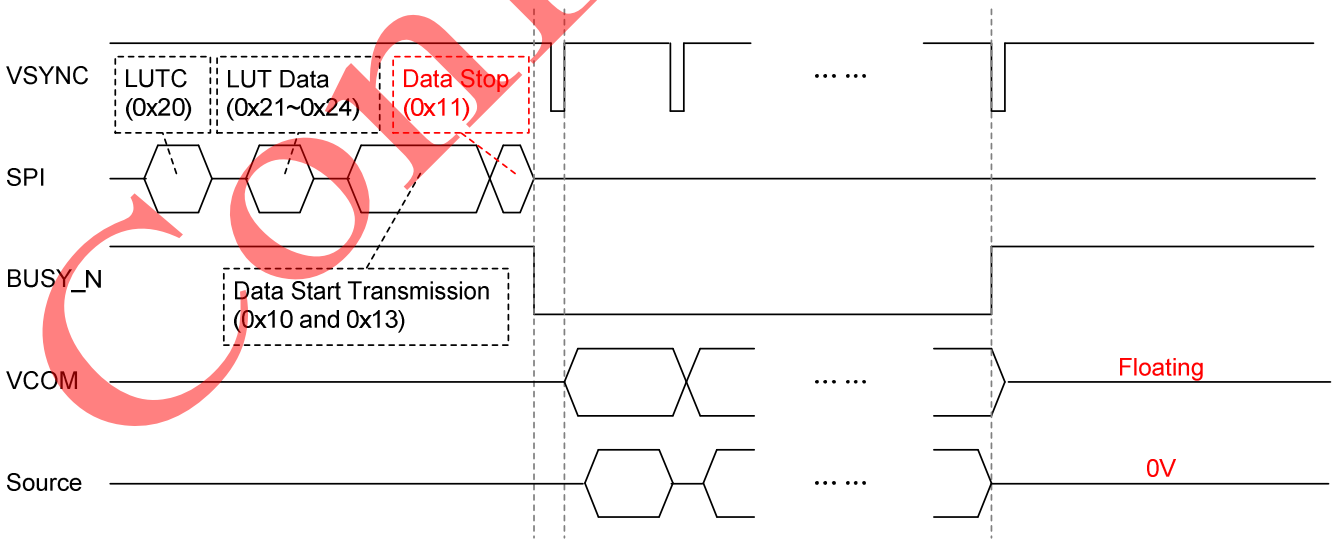
Data Transmission Waveform

Example 1: After 3 cases, the driver will send 2 frame VCOM and data to 0 V.

1. All 6 LUT groups (KW mode) or 8 LUT groups (KWR mode) complete .
2. meet the group whose Times to Repeat =0
3. meet the group whose all Number of Frames =0



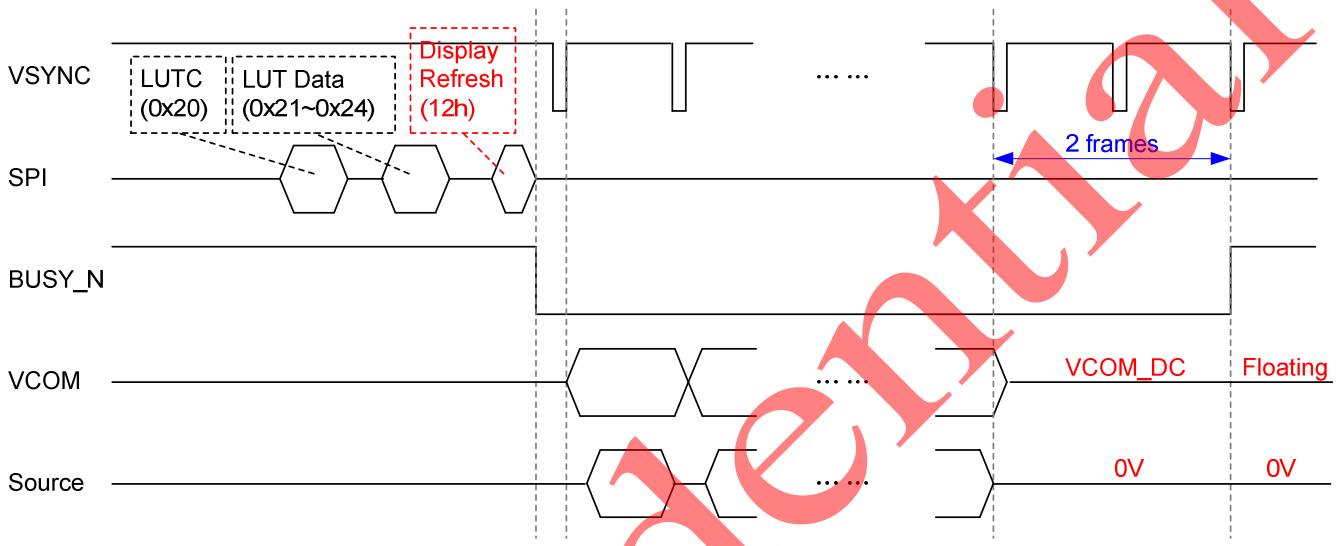
Example2: While level selection in LUT (LUTC only) is "1111_1111b", the driver will float VCOM.



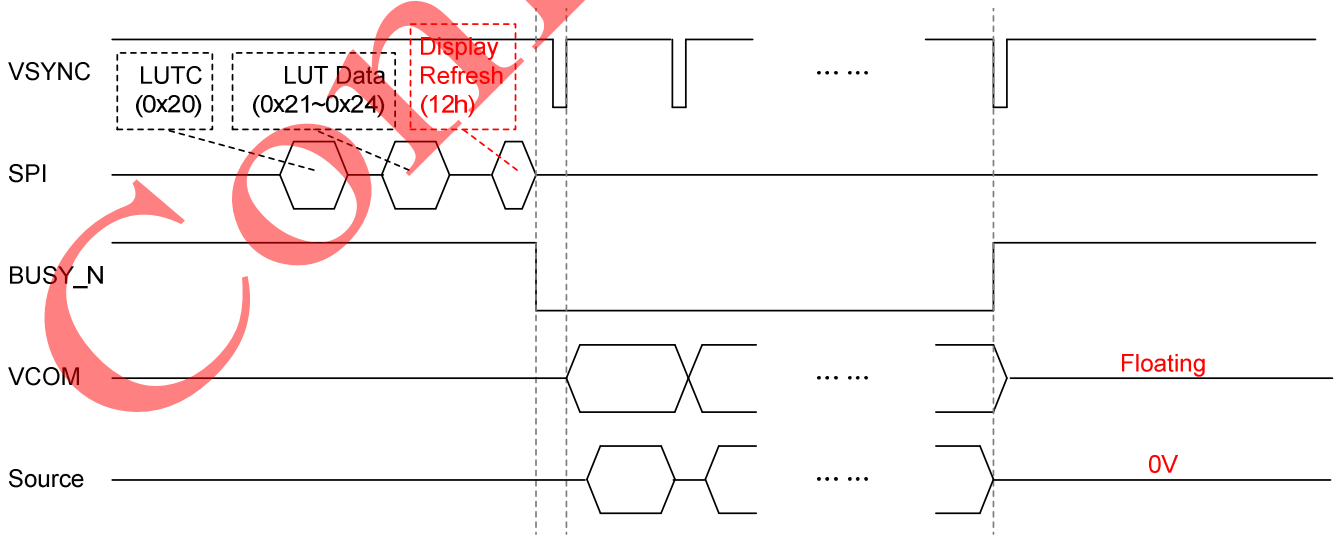
Display Refresh Waveform

Example 1: After three cases, the driver will send 2 frames VCOM and data to 0 V.

1. All 6 LUT states (KW mode) or 8 LUT states (KWR mode) complete
2. meet the state whose Times to Repeat = 0
3. meet the state whose all Number of Frames = 0



Example2: While level selection in LUT (LUTC only) is "1111_1111b", the driver will float VCOM.



BUSY_N Signal

Commands, except reading command, are restricted by refreshing display (DRF / DSP) as listed in the following table.

BUSY_N is used to represent the status of internal action. Commands activating internal operation or calculation will cause BUSY_N falling to LOW. After actions completed, BUSY_N will return to HIGH.

Command	Refresh Restriction	BUSY_N flag
PSR	X	No action
PWR	X	No action
POF	X	Flag
PFS	X	No action
PON	X	Flag
PMES	X	Flag
BTST	X	No action
DSLP	X	Flag
AUTO	X	Flag
DTM1	X	No action
DSP	X	Flag
DRF	X	Flag
DTM2	X	No action
LUTC	X	No action
LUTWW	X	No action
LUTWK/LUTW	X	No action
LUTKW/LUTR	X	No action
LUTKK/LUTK	X	No action
LUTOPT	X	No action
PLL	X	No action
TSC	X	Flag
TSE	X	No action
TSW	X	No action
TSR	X	No action
PBC	X	No action
CDI	X	No action
LPD	X	Flag
TCON	X	No action
TRES	X	No action
GSST	X	No action
REV	V	No action
FLG	V	No action
AMV	X	Flag
VV	V	No action
VDCS	X	No action
PTL	X	No action
PTIN	X	No action
PTOUT	X	No action
PGM	X	No action
APG	X	Flag
ROTP	X	No action
CCSET	X	No action
PWS	X	No action
LVSEL	X	No action
TSSET	X	No action

V: Accepted, X: Ignored

OTP ADDRESS MAPPING

The size of the internal One Time Programmable (OTP) memory is 6K bytes, and the address is from 0x000 to 0x17FF. The unprogrammed bit is logic 1. Only the bit at logic 1 can be programmed to logic 0, but the bit at logic 0 can not be converted to logic 1.

There is one area (0x17E0~0x17FF) is reserved for UltraChip only, and write all 0xFF of data to skip the 2 areas. The recommended voltage of VPP during programming is 7.75V. In the other condition except for programming, let VPP floating or be connected to GND. The maximum current of VPP during programming is 5mA.

There are 2 banks in the internal OTP, and each bank has 3K bytes storage memory. The formats of each bank are the same, and the selection of bank is controlled by Check Code (0x0000 and 0x0C00). The 2 banks are used for two times programming.

Table 1: OTP Address Map

Bank0		Bank1	
Address	Content	Address	Content
0x0000	Check Code (0xA5)	0x0C00	Check Code (0xA5)
0x0001~0x0016	Command Default Setting *(1)	0x0C01~0x0C16	Command Default Setting *(1)
0x0017~0x0019	Chip ID [23:0]	0x0C17~0x0C19	Chip ID [23:0]
0x001A~0x001C	LUT Version [23:0]	0x0C1A~0x0C1C	LUT Version [23:0]
0x001D~0x0027	Temperature Boundary 0~10 (TB0~TB10)	0x0C1D~0x0C27	Temperature Boundary 0~10 (TB0~TB10)
0x0028~0x0110	Temperature Range 0 *(2)	0x0C28~0x0D10	Temperature Range 0 *(2)
0x0111~0x01F9	Temperature Range 1 *(2)	0x0D11~0x0DF9	Temperature Range 1 *(2)
0x01FA~0x02E2	Temperature Range 2 *(2)	0x0DFA~0x0EE2	Temperature Range 2 *(2)
0x02E3~0x03CB	Temperature Range 3 *(2)	0x0EE3~0x0FCB	Temperature Range 3 *(2)
0x03CC~0x04B4	Temperature Range 4 *(2)	0x0FCC~0x10B4	Temperature Range 4 *(2)
0x04B5~0x059D	Temperature Range 5 *(2)	0x10B5~0x119D	Temperature Range 5 *(2)
0x059E~0x0686	Temperature Range 6 *(2)	0x119E~0x1286	Temperature Range 6 *(2)
0x0687~0x076F	Temperature Range 7 *(2)	0x1287~0x136F	Temperature Range 7 *(2)
0x0770~0x0858	Temperature Range 8 *(2)	0x1370~0x1458	Temperature Range 8 *(2)
0x0859~0x0941	Temperature Range 9 *(2)	0x1459~0x1541	Temperature Range 9 *(2)
0x0942~0x0A2A	Temperature Range 10 *(2)	0x1542~0x162A	Temperature Range 10 *(2)
0x0A2B~0x0B13	Temperature Range 11 *(2)	0x162B~0x1713	Temperature Range 11 *(2)
0x0B14~0x0BF0	Reserved for user-defined	0x1714~0x17DF	Reserved for user-defined
0x0BF1~0x0BFF	Reserved for user-defined	0x17E0~0x17FF	Reserved for UltraChip

Note:

(1) See section “COMMAND DEFAULT SETTING” for more detail.

(2) See section “LUT FORMAT IN OTP” for more detail.

TEMPERATURE RANGE

The temperature selection mechanism consists of a less-than-or-equal-to operator and 11 temperature boundary settings (TBx) to determine 12 temperature ranges. The sequence of mechanism is from TB0 to TB8, as shown below. If less than 10 tempeature ranges are used, the last TBx must be set to 0x7F to end the mechanism.

Procedure Order	Comparison Condition	Action & Segment Selection
1-0. Read 0x000	Content = 0xA5 ?	Yes: Jump to Procedure 2 (Bank0), No: Jump to Procedure 1-1
1-1, Read 0xC00	Content = 0xA5 ?	Yes: Jump to Procedure 2 (Bank1), No: Stop Refresh
2. Read 0x001D / 0x0C1D	Real Temperature ≦ TB0	Use TR0's table & setting, exit
3. Read 0x001E / 0x0C1E	Real Temperature ≦ TB1	Use TR1's table & setting, exit
4. Read 0x001F / 0x0C1F	Real Temperature ≦ TB2	Use TR2's table & setting, exit
5. Read 0x0020 / 0x0C20	Real Temperature ≦ TB3	Use TR3's table & setting, exit
6. Read 0x0021 / 0x0C21	Real Temperature ≦ TB4	Use TR4's table & setting, exit
7. Read 0x0022 / 0x0C22	Real Temperature ≦ TB5	Use TR5's table & setting, exit
8. Read 0x0023 / 0x0C23	Real Temperature ≦ TB6	Use TR6's table & setting, exit
9. Read 0x0024 / 0x0C24	Real Temperature ≦ TB7	Use TR7's table & setting, exit
10. Read 0x0025 / 0x0C25	Real Temperature ≦ TB8	Use TR8's table & setting, exit
11. Read 0x0026 / 0x0C26	Real Temperature ≦ TB9	Use TR9's table & setting, exit
12. Read 0x0027 / 0x0C27	Real Temperature ≦ TB10	Use TR10's table & setting, exit
13. Other	Real Temperature > TB10	Use TR11's table & setting, finish

***Note:**

(1) TRx's content is defined in "LUT FORMAT IN OTP" section.

Example:

If temperature = -20 °C, TR0 is selected.

If temperature = -10 °C, TR1 is selected.

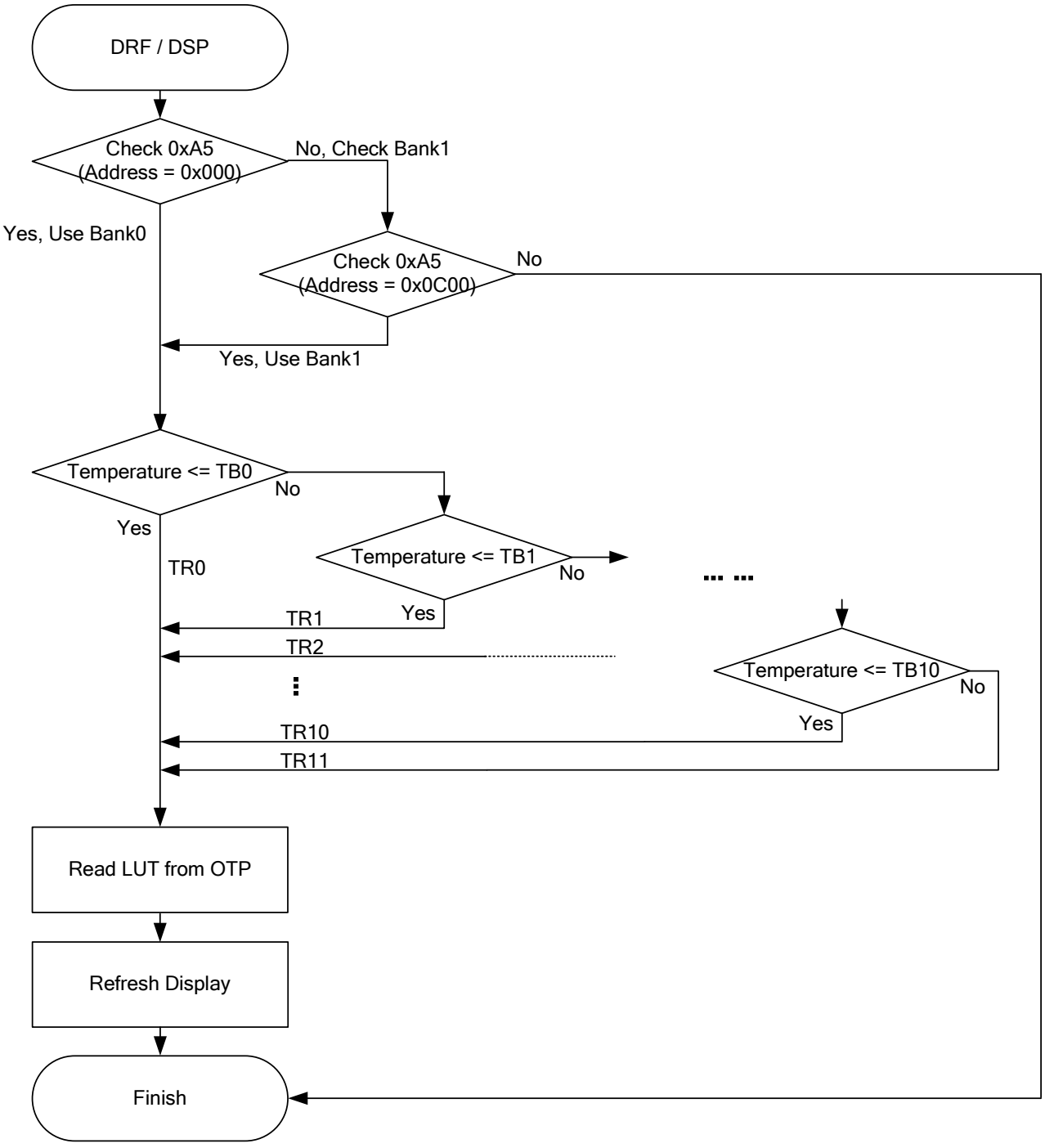
If temperature = 0 °C, TR2 is selected.

If temperature = 20 °C, TR4 is selected.

If temperature = 40 °C, TR5 is selected.

If temperature > 40 °C, TR5 is selected.

OTP Address	Content	
002h	0xF1	(-15 °C)
003h	0xFB	(-5 °C)
004h	0x00	(0 °C)
005h	0x0A	(10 °C)
006h	0x1E	(30 °C)
007h	0x7F	-



Temperature Selection Mechanism

COMMAND DEFAULT SETTING

This function can modify the default value of command registers by the OTP content between address 0x0001~0x0015 (or 0x0C01~0x0C15). The data of address 0x0001 (or 0x0C01) is the enable key of the function. Changing default value function is used to reduce the initial code length executed by the microcontroller.

Address (Hex)	D7	D6	D5	D4	D3	D2	D1	D0	Command	Registers	Original
0x0001	#	#	#	#	#	#	#	#	Check Code	0xA5 (Enable Key)	--
0x0002	#	#	#	#	#	#	--	--	PSR	RES[1:0], REG, KW/R, UD, SHL	0x0F
0x0003	--	--	--	#-	#	#	#	#		VCMZ,TS_AUTO,TIEG ,NORG, VC_LUTZ	0x0D
0x0004	--	--	#	#	--	--	--	--	PFS	T_VDS_OF[1:0]	0x00
0x0005	#	#	#	#	#	#	#	#	BTST	BT_PHA[7:0]	0x17
0x0006	#	#	#	#	#	#	#	#		BT_PHB[7:0]	0x17
0x0007	--	--	#	#	#	#	#	#		BT_PHC[5:0]	0x17
0x0008	#	--	--	--	#	#	#	#	TSE	TSE, TO[3:0]	0x00
0x0009	#	#	#	#	#	#	#	#	CDI	VBD[1:0], DDX[1:0], CDI[3:0]	0xD7
0x000A	#	#	#	#	#	#	#	#	TCON	S2G[3:0], G2S[3:0]	0x22
0x000B	--	--	--	--	--	--	--	#	TRES	HRES[8:3]	0x00
0x000C	#	#	#	#	#	0	0	0			0x00
0x000D	--	--	--	--	--	--	--	#		VRES[8:0]	0x00
0x000E	#	#	#	#	#	#	#	#			0x00
0x000F	--	--	--	--	--	--	--	#	GSST	HST[8:3]	0x00
0x0010	#	#	#	#	#	0	0	0			0x00
0x0011	--	--	--	--	--	--	--	#		VST[8:0]	0x00
0x0012	#	#	#	#	#	#	#	#			0x00
0x0013	--	--	--	--	--	--	#	#	CCSET	TSFIX,CCEN	0x00
0x0014	#	#	#	#	#	#	#	#	PWS	VCOM_W[3:0], SD_W[3:0]	0x00
0x0015	--	--	--	--	--	--	#	#	LVSEL	LVD_SEL[1:0]	0x03
0x0016	#	#	#	#	#	#	#	#	TSSET	TS_SET[7:0]	0x00

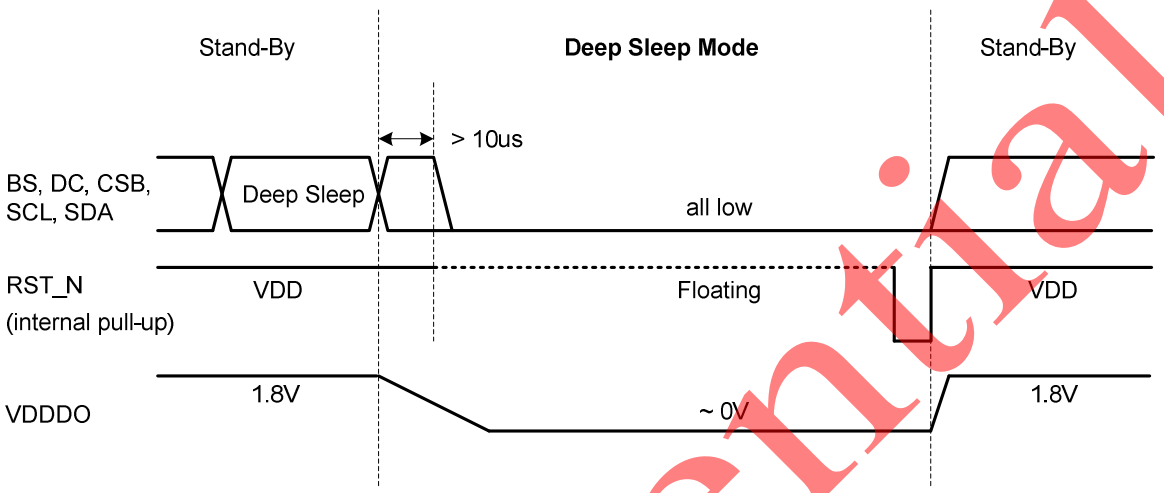
LUT FORMAT IN OTP

There are 12 TRs (temperature range) in a bank. Each TR has independant frame rate, voltage, XON settings and LUTs. The fomat of LUT is different in different mode. In KWR mode, there are only 4 LUTs including LUTC, LUTR, LUTW and LUTK in TRs. In KW mode, there are 5 LUTs including LUT, LUTWW, LUTKW, LUTWK and LUTKK in TRs. All LUTs have same number of state.

	KWR Mode (KW/R=0)		KW Mode (KW/R=1)	
	Address	Content	Address	Content
TR0	0x0028	3'b0,Frame Rate[5:0]	0x0028	3'b0,Frame Rate[5:0]
	0x0029	3'b0, VCOM_SLEW,VG Voltage[3:0]	0x0029	3'b0, VCOM_SLEW,VG Voltage [2:0]
	0x002A	2'b0, VSH Voltage[5:0]	0x002A	2'b0, VSH Voltage [5:0]
	0x002B	2'b0,VSL Voltage[5:0]	0x002B	2'b0,VSL Voltage [5:0]
	0x002C	2'b0,VDHR Voltage[5:0]	0x002C	2'b0,VDHR Voltage [5:0]
	0x002D	1'b0, VCOM_DC Voltage[6:0]	0x002D	1'b0, VCOM_DC Voltage [6:0]
	0x002E	EOPT, ESO, 6'b0	0x002E	EOPT, ESO, 6'b0
	0x002F	STATE XON[7:0]	0x002F	STATE XON[7:0]
	0x0030	STATE XON[15:8]	0x0030	STATE XON[15:8]
	0x0031~0x068	LUTC (8 states)	0x0031~0x0C5A	LUTC (6 states)
			0x005B~0x0084	LUTWW (6 states)
	0x0069~0x00A0	LUTR (8 states)	0x0085~0x00AE	LUTKW (6 states)
			0x00AF~0x00D8	LUTWK (6 states)
	0x0A1~0x0D8	LUTW (8 states)	0x00D9~0x0102	LUTKK (6 states)
	0x00D9~0x0110	LUTK (8 states)	0x0103~0x0110	Reserved

DEEP SLEEP MODE

After deep sleep command (R07H) is transmitted, UC8276 enter “Deep Sleep Mode”, and leaves by RST_N falling. In “Deep Sleep Mode”, the control signals are recommended tied to 0v to avoid IO leakage current. And the die must be keep away from light which causes photoelectric effect to make internal nodes unstable.



PANEL BREAK CHECK

The panel break check (PBC) function is accomplished by testing the connection of the ITO along panel edge. If the panel is broken, the loop ITO may be cut off. The connection check is judged by signal transmission from CHKGO to CHKGI.

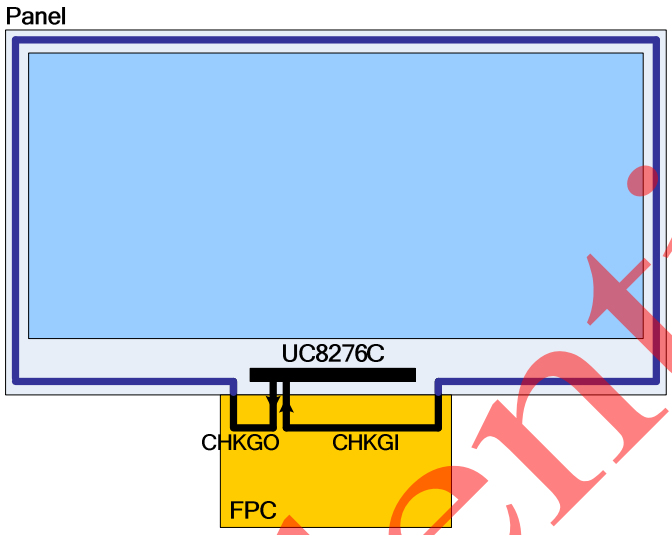


Figure: Panel break check layout example

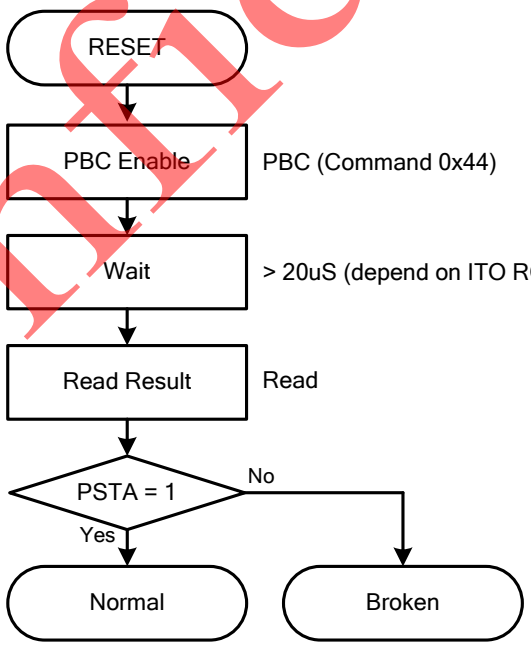
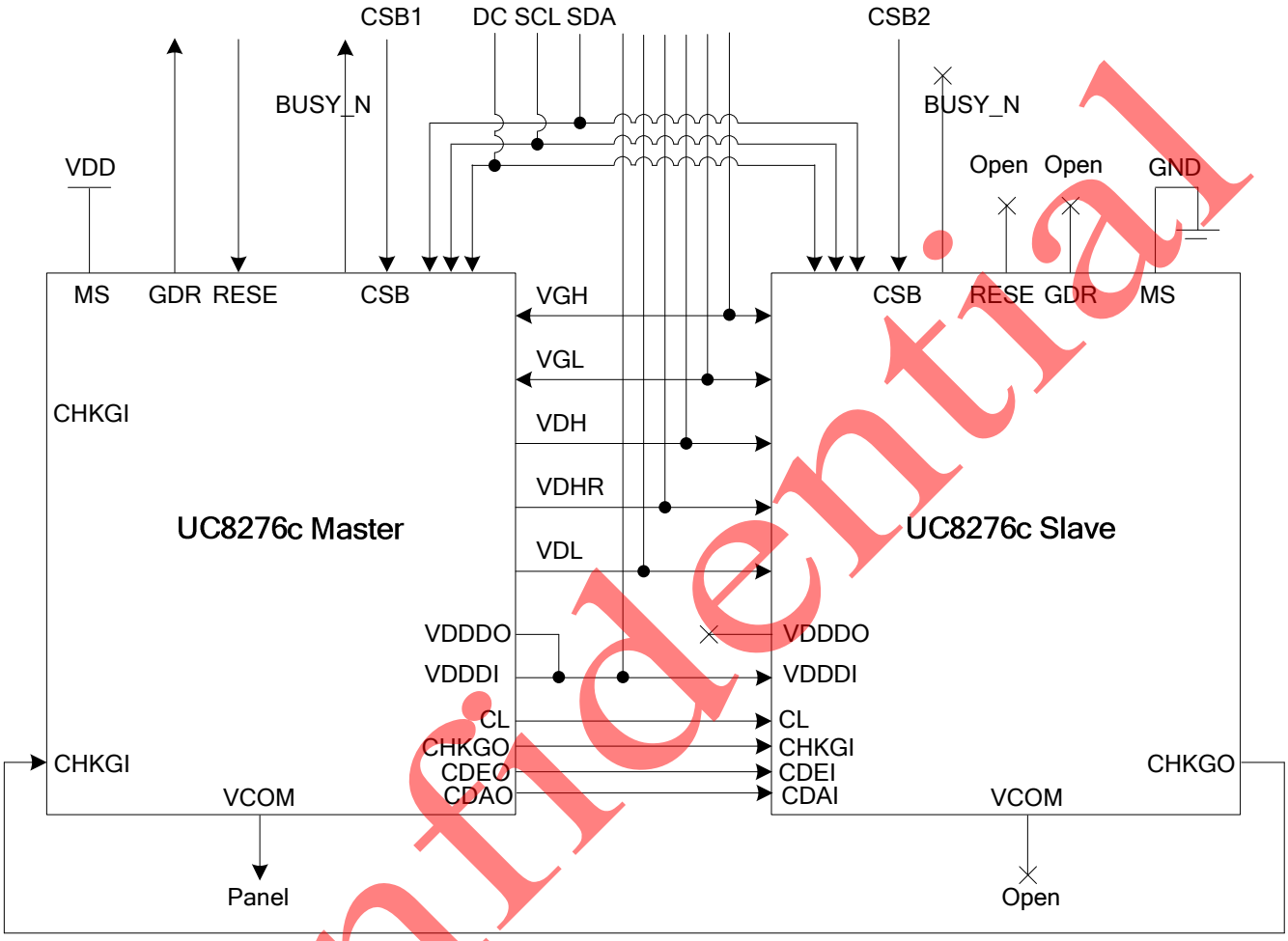


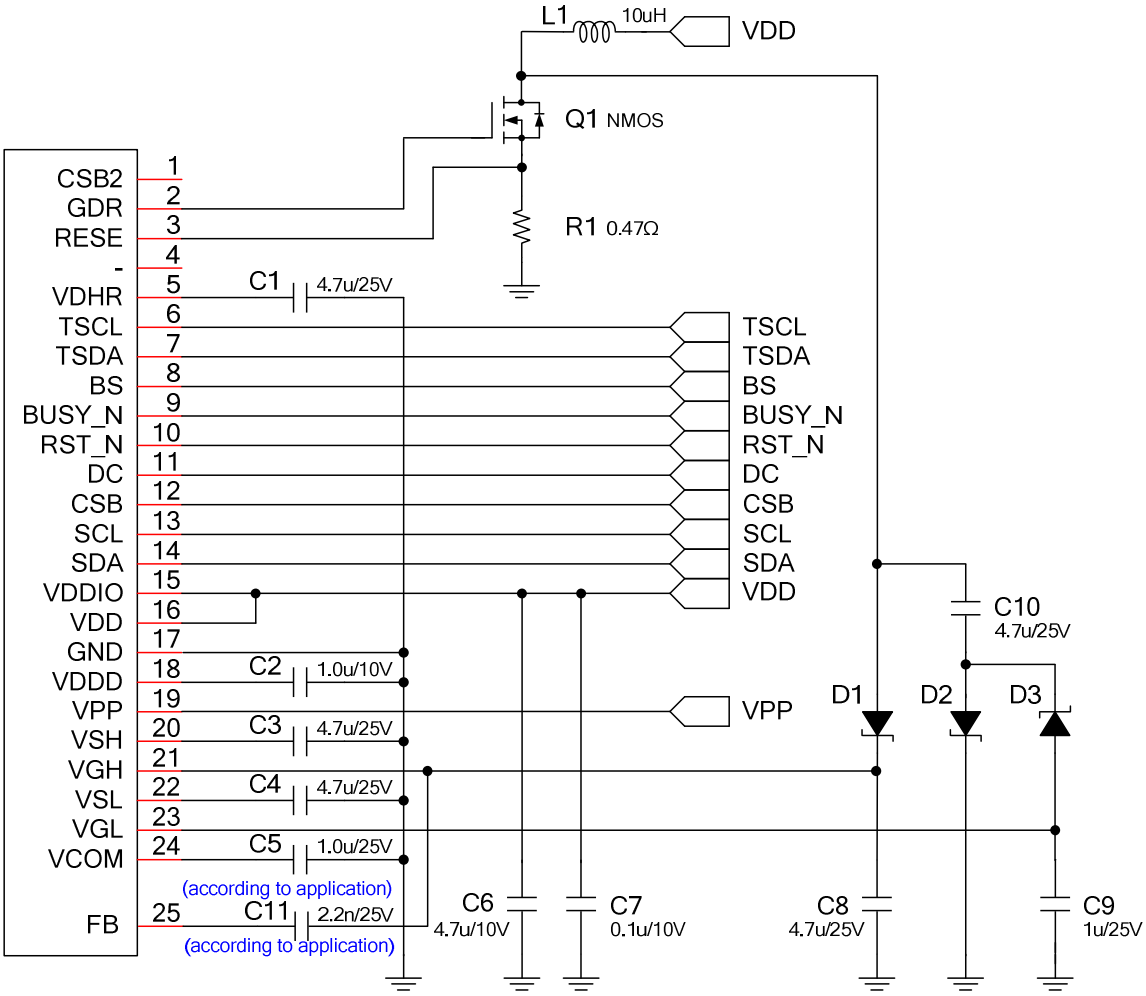
Figure: Panel Break Check (PBC) Sequence

CASCADE APPLICATION CIRCUIT



All commands sent to **Master** must be also sent to **Slave** except for data writing (DTM1 and DTM2). The display data must be separated to two parts, one is for **Master** and another is for **Slave**. They are transmitted to **Master** and **Slave** individually by using CSB1 and CSB2.

BOOSTER APPLICATION CIRCUIT



Note:

The capacitor value of VGH/VGL must be equal or more than the one of VSH/VSL/VDHR.

Recommended Device

1. Switch MOS NMOS: Vishay Si1308EDL (V_{DS} > 25V, I_D > 500mA, V_{GS}(th) < 1.5V, C_{iss} < 200pF, R_{DS}(on) < 400mΩ)
2. Schottky Diode: OnSemi MBR0530 (V_R > 25V, I_F > 500mA, I_R < 1mA @ V_R=15V, T_a=100°C)

Recommended Resister

Item	Pins	Resistance
Powers	VDD, VDDA, VDDIO, GND, GNDA, VDM	< 5 Ω
Boosters	VGL, VGH, GDR, RESE	< 10 Ω
Regulators	VDH, VDL, VDHR, VCOM, VDDD, VDDDO	< 10 Ω
Logics	MS, BS, CSB, SCL, SDA, GDR, etc.	< 50 Ω
OTP	VPP	< 10 Ω

ABSOLUTE MAXIMUM RATINGS

Signal	Item	Min	Max.	Unit
VDD, VDDIO, VDDA	Logic Supply voltage	-0.3	+6.0	V
VPP	OTP programming voltage	-0.3	+8.0	V
VI	Digital input range	-0.3	VDDIO+0.3	V
VGH-VGL	Supply range	-	+44.0	V
Source				
VSH	Analog supply voltage – positive	+16		V
VSL	Analog supply voltage -- negative	-16		V
VDHR	Analog supply voltage – positive	+16		V
Gate				
VGH	Analog supply voltage – positive	-0.3	+22	V
VGL	Analog supply voltage -- negative	-22	0.3	V
TSTG	Storage temperature range	-55	+125	°C

Warning:

If ICs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
VDDIO	IO supply voltage		2.3	3.3	3.6	V
VDD	Supply voltage		2.3	3.3	3.6	V
VDDA	DCDC driver supply voltage		2.3	3.3	3.6	V
VIL	LOW Level input voltage	Digital input pins	0	--	0.3xVDD	V
VIH	HIGH Level input voltage	Digital input pins	0.7xVDDIO	--	VDDIO	V
VOH	HIGH Level output voltage	Digital input pins, IOH=400uA	VDDIO-0.4	--	--	V
VOL	LOW Level Output voltage	Digital input pins, IOL=-400uA	0	--	0.4	V
IIN	Input leakage current	Digital input pins except pull-up, pull-down pin	-1	--	1	uA
RIN	Pull-up/down impedance			200		KΩ
Top	Operating temperature		-30		85	°C
dVGH	VGH Supply voltage dev		-400	0	+400	mV
VGH-VGL	Voltage Range of VGH - VGL		--		40	V
dVSH	Supply voltage dev		-200	0	+200	mV
dVSL	Supply voltage dev		-200	0	+200	mV
dVDHR	Supply voltage dev		-200	0	+200	mV
dVCOM	Supply voltage dev		-200	0	+200	mV
RON	Driver Output Resistance	For source driver, TOP=25°C, VOUT = ±15V		18.6	38.4	KΩ
		For gate driver, TOP=25°C, VOUT = ±20V		4	8	

VDD=VDDA=VDDIO=3.0V, TOP=25.0 °C

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
IVDD	Digital deep sleep current	VDDD OFF	--	0.3	0.5	uA
	Digital stand-by current	All stopped	--	8.2	10.0	uA
	Digital operating current		--	--	0.1	mA
IVDDIO	IO deep sleep current	VDDD OFF	--	0.1	0.3	uA
	IO stand-by current	Booster OFF	--	2.5	4.0	uA
	IO operating current	No load	--	--	0.1	mA
IVDDA	DCDC deep sleep current	VDDD OFF	--	0.1	0.3	uA
	DCDC stand-by current	Booster OFF	--	15.5	20.0	uA
	DCDC operating current	Source output VDH/VDL, Duty=0.5, Period =125uS VCOM DC No load	--	--	5.0	mA
		Source output VDH/VDL, Duty=0.5, Period =125uS, VCOM DC External cap: 415pF, NMOS=340pF	--	--	25.0	

AC CHARACTERISTICS

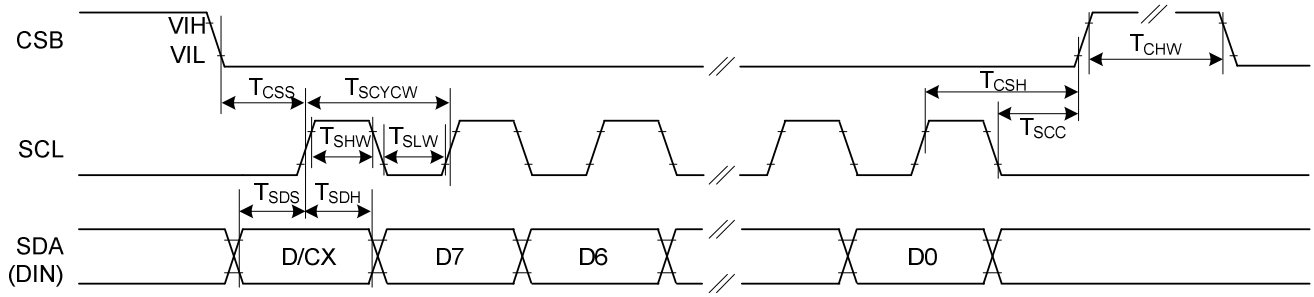


Figure: 3-wire Serial Interface Characteristics (Write mode)

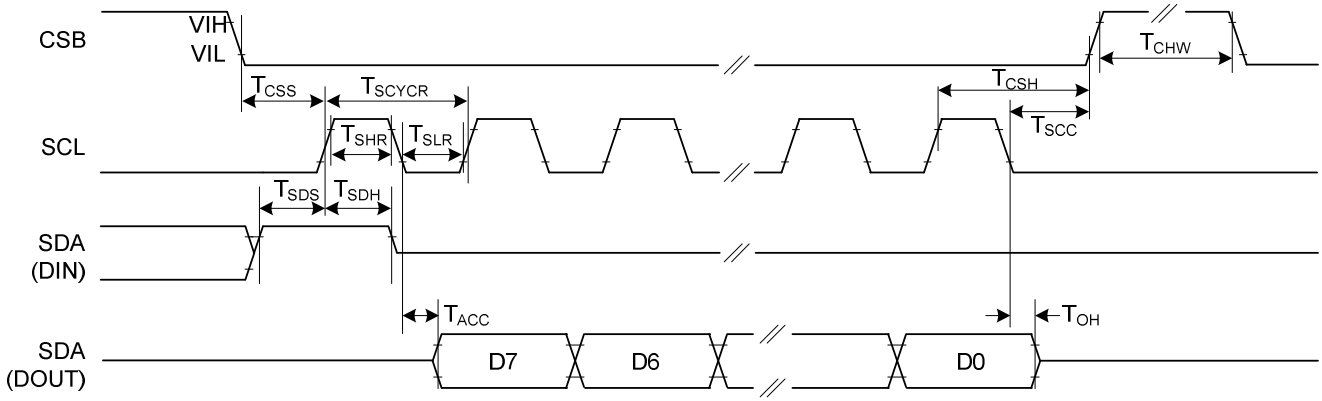


Figure: 3-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL “H” pulse width (Write)	35			ns
T_{SLW}		SCL “L” pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	350			ns
T_{SHR}		SCL “H” pulse width (Read)	175			ns
T_{SLR}		SCL “L” pulse width (Read)	175			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			250	ns
T_{OH}		Output disable time	15			ns

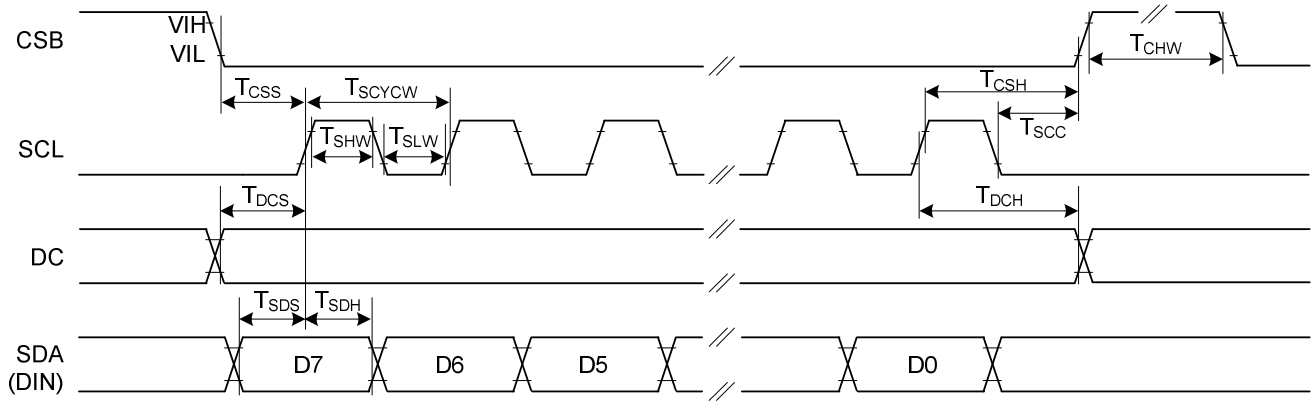


Figure: 4-wire Serial Interface Characteristics (Write mode)

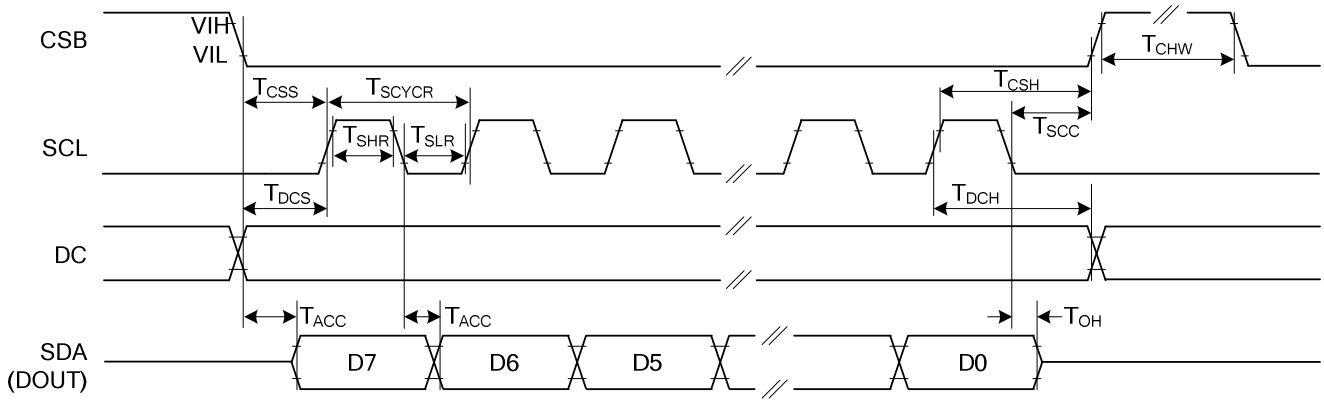
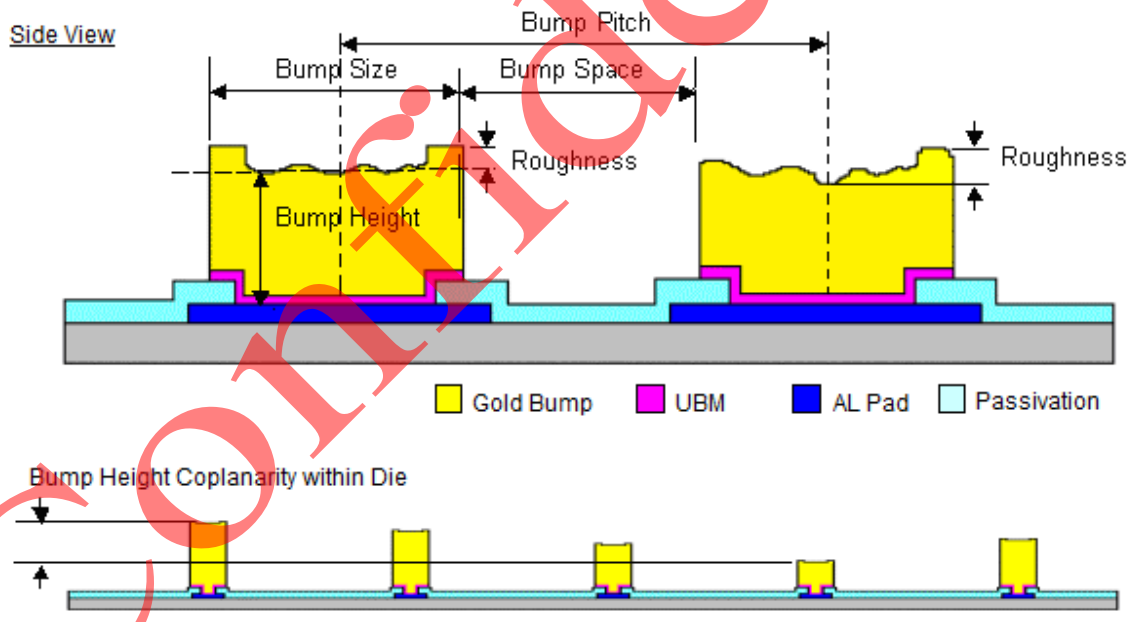


Figure: 4-wire Serial Interface Characteristics (Read mode)

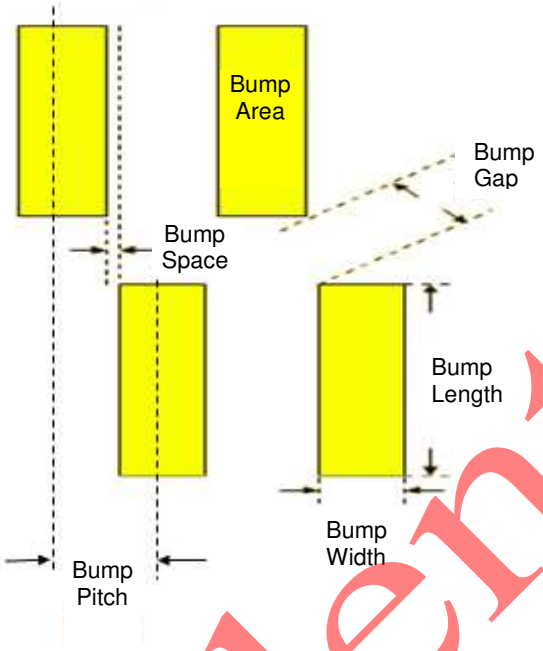
Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL “H” pulse width (Write)	35			ns
T_{SLW}		SCL “L” pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	350			ns
T_{SHR}		SCL “H” pulse width (Read)	175			ns
T_{SLR}		SCL “L” pulse width (Read)	175			ns
T_{DCS}	DC	DC setup time	30			ns
T_{DCH}		DC hold time	30			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			250	ns
T_{OH}		Output disable time	15			ns

PHYSICAL DIMENSIONS

Die Size:	(13130 μM ± 40μM) x (1030 μM ± 40μM)
Die Thickness:	300 μM ± 20μM
Die TTV:	(D_{MAX} – D_{MIN}) within die ≤ 2μM
Bump Height:	12 μM ± 3μM
	(H_{MAX} – H_{MIN}) within die ≤ 2μM
Bump Size:	16 μM x 75 μM ± 3μM
Bump Area:	1200 μM^2
Bump Pitch:	14 μM
Bump Gap:	-2 μM ± 3μM
Hardness:	65 Hv ± 15Hv
Shear:	5g/Mil^2
Coordinate origin:	Chip center
Pad reference:	Pad center

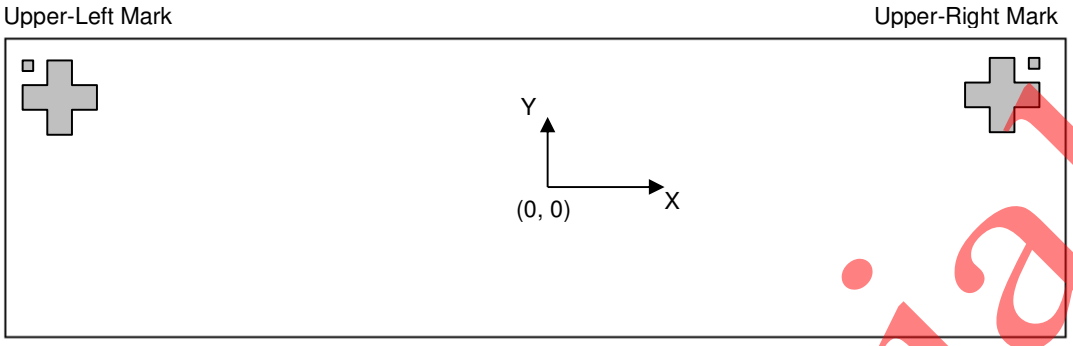


For Stagger Layout

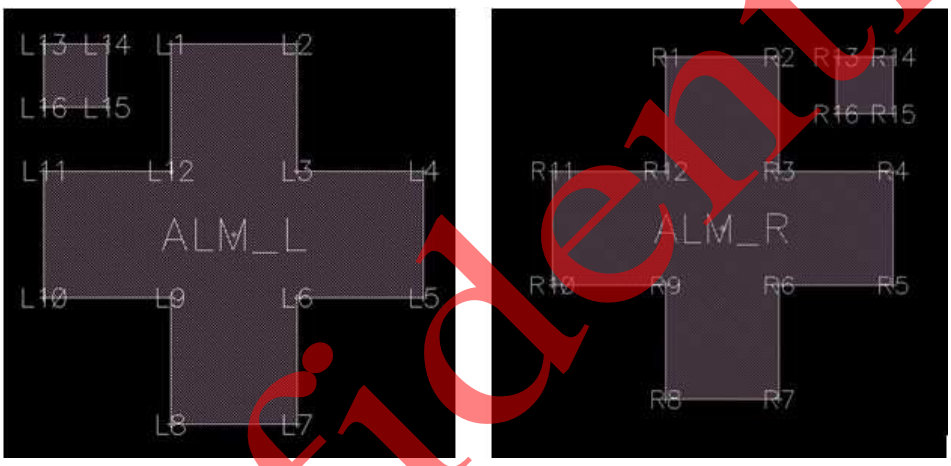


ALIGNMENT MARK INFORMATION

Location:



Shapes and Points:



Point Coordinates:

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
Center	-6465	415	6465	415
1	-6475	445	6455	445
2	-6455	445	6475	445
3	-6455	425	6475	425
4	-6435	425	6495	425
5	-6435	405	6495	405
6	-6455	405	6475	405
7	-6455	385	6475	385
8	-6475	385	6455	385
9	-6475	405	6455	405
10	-6495	405	6435	405
11	-6495	425	6435	425
12	-6475	425	6455	425
13	-6495	445	6485	445
14	-6485	445	6495	445
15	-6485	435	6495	435
16	-6495	435	6485	435

PAD COORDINATES

#	Pad	X	Y	W	H
1	NC	-6440	-423	28	70
2	VCOM	-6394	-423	28	70
3	VCOM	-6348	-423	28	70
4	VCOM	-6302	-423	28	70
5	VCOM	-6256	-423	28	70
6	VCOM	-6210	-423	28	70
7	VCOM	-6164	-423	28	70
8	VCOM	-6118	-423	28	70
9	VCOM	-6072	-423	28	70
10	VDM	-6026	-423	28	70
11	VGL	-5980	-423	28	70
12	VGL	-5934	-423	28	70
13	VGL	-5888	-423	28	70
14	VGL	-5842	-423	28	70
15	VGL	-5796	-423	28	70
16	VGL	-5750	-423	28	70
17	VGL	-5704	-423	28	70
18	VGL	-5658	-423	28	70
19	VGL	-5612	-423	28	70
20	VGL	-5566	-423	28	70
21	VGL	-5520	-423	28	70
22	VGL	-5474	-423	28	70
23	VGL	-5428	-423	28	70
24	VGL	-5382	-423	28	70
25	VGL	-5336	-423	28	70
26	VGL	-5290	-423	28	70
27	GND	-5244	-423	28	70
28	VSL	-5198	-423	28	70
29	VSL	-5152	-423	28	70
30	VSL	-5106	-423	28	70
31	VSL	-5060	-423	28	70
32	VSL	-5014	-423	28	70
33	VSL	-4968	-423	28	70
34	VSL	-4922	-423	28	70
35	VSL	-4876	-423	28	70
36	VSL	-4830	-423	28	70
37	VSL	-4784	-423	28	70
38	GND	-4738	-423	28	70
39	VGH	-4692	-423	28	70
40	VGH	-4646	-423	28	70
41	VGH	-4600	-423	28	70
42	VGH	-4554	-423	28	70
43	VGH	-4508	-423	28	70
44	VGH	-4462	-423	28	70
45	VGH	-4416	-423	28	70
46	VGH	-4370	-423	28	70
47	VGH	-4324	-423	28	70
48	VGH	-4278	-423	28	70
49	VGH	-4232	-423	28	70
50	VGH	-4186	-423	28	70
51	VGH	-4140	-423	28	70
52	VGH	-4094	-423	28	70
53	GND	-4048	-423	28	70
54	VSH	-4002	-423	28	70
55	VSH	-3956	-423	28	70
56	VSH	-3910	-423	28	70

#	Pad	X	Y	W	H
57	VSH	-3864	-423	28	70
58	VSH	-3818	-423	28	70
59	VSH	-3772	-423	28	70
60	VSH	-3726	-423	28	70
61	VSH	-3680	-423	28	70
62	VSH	-3634	-423	28	70
63	VSH	-3588	-423	28	70
64	GND	-3542	-423	28	70
65	VPP	-3496	-423	28	70
66	VPP	-3450	-423	28	70
67	VPP	-3404	-423	28	70
68	VPP	-3358	-423	28	70
69	VPP	-3312	-423	28	70
70	VPP	-3266	-423	28	70
71	VPP	-3220	-423	28	70
72	VDDDI	-3174	-423	28	70
73	VDDDI	-3128	-423	28	70
74	VDDDI	-3082	-423	28	70
75	VDDDI	-3036	-423	28	70
76	VDDDI	-2990	-423	28	70
77	VDDDO	-2944	-423	28	70
78	VDDDO	-2898	-423	28	70
79	VDDDO	-2852	-423	28	70
80	VDDDO	-2806	-423	28	70
81	VDDDO	-2760	-423	28	70
82	VDM	-2714	-423	28	70
83	VDM	-2668	-423	28	70
84	GNDA	-2622	-423	28	70
85	GNDA	-2576	-423	28	70
86	GNDA	-2530	-423	28	70
87	GNDA	-2484	-423	28	70
88	GNDA	-2438	-423	28	70
89	GNDA	-2392	-423	28	70
90	GNDA	-2346	-423	28	70
91	GNDA	-2300	-423	28	70
92	GNDA	-2254	-423	28	70
93	GNDA	-2208	-423	28	70
94	GND	-2162	-423	28	70
95	GND	-2116	-423	28	70
96	GND	-2070	-423	28	70
97	GND	-2024	-423	28	70
98	GND	-1978	-423	28	70
99	GND	-1932	-423	28	70
100	GND	-1886	-423	28	70
101	GND	-1840	-423	28	70
102	GND	-1794	-423	28	70
103	GND	-1748	-423	28	70
104	GND	-1702	-423	28	70
105	GND	-1656	-423	28	70
106	VDDA	-1610	-423	28	70
107	VDDA	-1564	-423	28	70
108	VDDA	-1518	-423	28	70
109	VDDA	-1472	-423	28	70
110	VDDA	-1426	-423	28	70
111	VDDA	-1380	-423	28	70
112	VDDA	-1334	-423	28	70

#	Pad	X	Y	W	H
113	VDDA	-1288	-423	28	70
114	VDDA	-1242	-423	28	70
115	VDDA	-1196	-423	28	70
116	VDD	-1150	-423	28	70
117	VDD	-1104	-423	28	70
118	VDD	-1058	-423	28	70
119	VDD	-1012	-423	28	70
120	VDD	-966	-423	28	70
121	VDD	-920	-423	28	70
122	VDD	-874	-423	28	70
123	DUMMY	-828	-423	28	70
124	DUMMY	-782	-423	28	70
125	DUMMY	-736	-423	28	70
126	DUMMY	-690	-423	28	70
127	DUMMY	-644	-423	28	70
128	DUMMY	-598	-423	28	70
129	DUMMY	-552	-423	28	70
130	DUMMY	-506	-423	28	70
131	DUMMY	-460	-423	28	70
132	DUMMY	-414	-423	28	70
133	DUMMY	-368	-423	28	70
134	DUMMY	-322	-423	28	70
135	DUMMY	-276	-423	28	70
136	DUMMY	-230	-423	28	70
137	DUMMY	-184	-423	28	70
138	DUMMY	-138	-423	28	70
139	DUMMY	-92	-423	28	70
140	DUMMY	-46	-423	28	70
141	DUMMY	0	-423	28	70
142	DUMMY	46	-423	28	70
143	DUMMY	92	-423	28	70
144	DUMMY	138	-423	28	70
145	DUMMY	184	-423	28	70
146	DUMMY	230	-423	28	70
147	DUMMY	276	-423	28	70
148	DUMMY	322	-423	28	70
149	DUMMY	368	-423	28	70
150	DUMMY	414	-423	28	70
151	DUMMY	460	-423	28	70
152	DUMMY	506	-423	28	70
153	DUMMY	552	-423	28	70
154	DUMMY	598	-423	28	70
155	DUMMY	644	-423	28	70
156	DUMMY	690	-423	28	70
157	DUMMY	736	-423	28	70
158	DUMMY	782	-423	28	70
159	DUMMY	828	-423	28	70
160	TEST1	874	-423	28	70
161	GND	920	-423	28	70
162	TEST2	966	-423	28	70
163	DUMMY	1012	-423	28	70
164	DUMMY	1058	-423	28	70
165	VDDIO	1104	-423	28	70
166	VDDIO	1150	-423	28	70
167	VDDIO	1196	-423	28	70
168	VDDIO	1242	-423	28	70
169	DUMMY	1288	-423	28	70
170	TEST3	1334	-423	28	70
171	DUMMY	1380	-423	28	70

#	Pad	X	Y	W	H
172	DUMMY	1426	-423	28	70
173	DUMMY	1472	-423	28	70
174	DUMMY	1518	-423	28	70
175	DUMMY	1564	-423	28	70
176	SDA	1610	-423	28	70
177	SCL	1656	-423	28	70
178	GND	1702	-423	28	70
179	CSB	1748	-423	28	70
180	VDDIO	1794	-423	28	70
181	DUMMY	1840	-423	28	70
182	DUMMY	1886	-423	28	70
183	GND	1932	-423	28	70
184	DC	1978	-423	28	70
185	VDDIO	2024	-423	28	70
186	DUMMY	2070	-423	28	70
187	DUMMY	2116	-423	28	70
188	DUMMY	2162	-423	28	70
189	DUMMY	2208	-423	28	70
190	RST_N	2254	-423	28	70
191	BUSY_N	2300	-423	28	70
192	GND	2346	-423	28	70
193	DUMMY	2392	-423	28	70
194	DUMMY	2438	-423	28	70
195	DUMMY	2484	-423	28	70
196	CDAO	2530	-423	28	70
197	CDEO	2576	-423	28	70
198	CL	2622	-423	28	70
199	CDEI	2668	-423	28	70
200	CDAI	2714	-423	28	70
201	DUMMY	2760	-423	28	70
202	VDDIO	2806	-423	28	70
203	VSYNC	2852	-423	28	70
204	GND	2898	-423	28	70
205	DUMMY	2944	-423	28	70
206	VDDIO	2990	-423	28	70
207	BS	3036	-423	28	70
208	GND	3082	-423	28	70
209	DUMMY	3128	-423	28	70
210	VDDIO	3174	-423	28	70
211	CHKGI	3220	-423	28	70
212	GND	3266	-423	28	70
213	MS	3312	-423	28	70
214	VDDIO	3358	-423	28	70
215	GND	3404	-423	28	70
216	TSDA	3450	-423	28	70
217	TSDA	3496	-423	28	70
218	TSCL	3542	-423	28	70
219	TSCL	3588	-423	28	70
220	GND	3634	-423	28	70
221	CHKGO	3680	-423	28	70
222	TEST5	3726	-423	28	70
223	GND	3772	-423	28	70
224	TEST6	3818	-423	28	70
225	TEST7	3864	-423	28	70
226	GND	3910	-423	28	70
227	TEST8	3956	-423	28	70
228	TEST9	4002	-423	28	70
229	GND	4048	-423	28	70
230	TEST10	4094	-423	28	70

#	Pad	X	Y	W	H
231	TEST11	4140	-423	28	70
232	GND	4186	-423	28	70
233	TEST12	4232	-423	28	70
234	TEST13	4278	-423	28	70
235	DUMMY	4324	-423	28	70
236	DUMMY	4370	-423	28	70
237	DUMMY	4416	-423	28	70
238	DUMMY	4462	-423	28	70
239	DUMMY	4508	-423	28	70
240	DUMMY	4554	-423	28	70
241	DUMMY	4600	-423	28	70
242	DUMMY	4646	-423	28	70
243	VDHR	4692	-423	28	70
244	VDHR	4738	-423	28	70
245	VDHR	4784	-423	28	70
246	VDHR	4830	-423	28	70
247	VDHR	4876	-423	28	70
248	VDHR	4922	-423	28	70
249	VDHR	4968	-423	28	70
250	VDHR	5014	-423	28	70
251	DUMMY	5060	-423	28	70
252	DUMMY	5106	-423	28	70
253	DUMMY	5152	-423	28	70
254	DUMMY	5198	-423	28	70
255	DUMMY	5244	-423	28	70
256	DUMMY	5290	-423	28	70
257	GND	5336	-423	28	70
258	FB	5382	-423	28	70
259	FB	5428	-423	28	70
260	GND	5474	-423	28	70
261	RESE	5520	-423	28	70
262	RESE	5566	-423	28	70
263	GND	5612	-423	28	70
264	GDR	5658	-423	28	70
265	GDR	5704	-423	28	70
266	GDR	5750	-423	28	70
267	GDR	5796	-423	28	70
268	GDR	5842	-423	28	70
269	GDR	5888	-423	28	70
270	GDR	5934	-423	28	70
271	GDR	5980	-423	28	70
272	NC	6026	-423	28	70
273	VCOM	6072	-423	28	70
274	VCOM	6118	-423	28	70
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276	VCOM	6210	-423	28	70
277	VCOM	6256	-423	28	70
278	VCOM	6302	-423	28	70
279	VCOM	6348	-423	28	70
280	VCOM	6394	-423	28	70
281	NC	6440	-423	28	70
282	NC	6345	338.5	17	75
283	NC	6324	438.5	17	75
284	NC	6303	338.5	17	75
285	NC	6282	438.5	17	75
286	NC	6261	338.5	17	75
287	GD<0>	6240	438.5	17	75
288	G<0>	6219	338.5	17	75
289	G<2>	6198	438.5	17	75

#	Pad	X	Y	W	H
290	G<4>	6177	338.5	17	75
291	G<6>	6156	438.5	17	75
292	G<8>	6135	338.5	17	75
293	G<10>	6114	438.5	17	75
294	G<12>	6093	338.5	17	75
295	G<14>	6072	438.5	17	75
296	G<16>	6051	338.5	17	75
297	G<18>	6030	438.5	17	75
298	G<20>	6009	338.5	17	75
299	G<22>	5988	438.5	17	75
300	G<24>	5967	338.5	17	75
301	G<26>	5946	438.5	17	75
302	G<28>	5925	338.5	17	75
303	G<30>	5904	438.5	17	75
304	G<32>	5883	338.5	17	75
305	G<34>	5862	438.5	17	75
306	G<36>	5841	338.5	17	75
307	G<38>	5820	438.5	17	75
308	G<40>	5799	338.5	17	75
309	G<42>	5778	438.5	17	75
310	G<44>	5757	338.5	17	75
311	G<46>	5736	438.5	17	75
312	G<48>	5715	338.5	17	75
313	G<50>	5694	438.5	17	75
314	G<52>	5673	338.5	17	75
315	G<54>	5652	438.5	17	75
316	G<56>	5631	338.5	17	75
317	G<58>	5610	438.5	17	75
318	G<60>	5589	338.5	17	75
319	G<62>	5568	438.5	17	75
320	G<64>	5547	338.5	17	75
321	G<66>	5526	438.5	17	75
322	G<68>	5505	338.5	17	75
323	G<70>	5484	438.5	17	75
324	G<72>	5463	338.5	17	75
325	G<74>	5442	438.5	17	75
326	G<76>	5421	338.5	17	75
327	G<78>	5400	438.5	17	75
328	G<80>	5379	338.5	17	75
329	G<82>	5358	438.5	17	75
330	G<84>	5337	338.5	17	75
331	G<86>	5316	438.5	17	75
332	G<88>	5295	338.5	17	75
333	G<90>	5274	438.5	17	75
334	G<92>	5253	338.5	17	75
335	G<94>	5232	438.5	17	75
336	G<96>	5211	338.5	17	75
337	G<98>	5190	438.5	17	75
338	G<100>	5169	338.5	17	75
339	G<102>	5148	438.5	17	75
340	G<104>	5127	338.5	17	75
341	G<106>	5106	438.5	17	75
342	G<108>	5085	338.5	17	75
343	G<110>	5064	438.5	17	75
344	G<112>	5043	338.5	17	75
345	G<114>	5022	438.5	17	75
346	G<116>	5001	338.5	17	75
347	G<118>	4980	438.5	17	75
348	G<120>	4959	338.5	17	75

#	Pad	X	Y	W	H
349	G<122>	4938	438.5	17	75
350	G<124>	4917	338.5	17	75
351	G<126>	4896	438.5	17	75
352	G<128>	4875	338.5	17	75
353	G<130>	4854	438.5	17	75
354	G<132>	4833	338.5	17	75
355	G<134>	4812	438.5	17	75
356	G<136>	4791	338.5	17	75
357	G<138>	4770	438.5	17	75
358	G<140>	4749	338.5	17	75
359	G<142>	4728	438.5	17	75
360	G<144>	4707	338.5	17	75
361	G<146>	4686	438.5	17	75
362	G<148>	4665	338.5	17	75
363	G<150>	4644	438.5	17	75
364	G<152>	4623	338.5	17	75
365	G<154>	4602	438.5	17	75
366	G<156>	4581	338.5	17	75
367	G<158>	4560	438.5	17	75
368	G<160>	4539	338.5	17	75
369	G<162>	4518	438.5	17	75
370	G<164>	4497	338.5	17	75
371	G<166>	4476	438.5	17	75
372	G<168>	4455	338.5	17	75
373	G<170>	4434	438.5	17	75
374	G<172>	4413	338.5	17	75
375	G<174>	4392	438.5	17	75
376	G<176>	4371	338.5	17	75
377	G<178>	4350	438.5	17	75
378	G<180>	4329	338.5	17	75
379	G<182>	4308	438.5	17	75
380	G<184>	4287	338.5	17	75
381	G<186>	4266	438.5	17	75
382	G<188>	4245	338.5	17	75
383	G<190>	4224	438.5	17	75
384	G<192>	4203	338.5	17	75
385	G<194>	4182	438.5	17	75
386	G<196>	4161	338.5	17	75
387	G<198>	4140	438.5	17	75
388	G<200>	4119	338.5	17	75
389	G<202>	4098	438.5	17	75
390	G<204>	4077	338.5	17	75
391	G<206>	4056	438.5	17	75
392	G<208>	4035	338.5	17	75
393	G<210>	4014	438.5	17	75
394	G<212>	3993	338.5	17	75
395	G<214>	3972	438.5	17	75
396	G<216>	3951	338.5	17	75
397	G<218>	3930	438.5	17	75
398	G<220>	3909	338.5	17	75
399	G<222>	3888	438.5	17	75
400	G<224>	3867	338.5	17	75
401	G<226>	3846	438.5	17	75
402	G<228>	3825	338.5	17	75
403	G<230>	3804	438.5	17	75
404	G<232>	3783	338.5	17	75
405	G<234>	3762	438.5	17	75
406	G<236>	3741	338.5	17	75
407	G<238>	3720	438.5	17	75

#	Pad	X	Y	W	H
408	G<240>	3699	338.5	17	75
409	G<242>	3678	438.5	17	75
410	G<244>	3657	338.5	17	75
411	G<246>	3636	438.5	17	75
412	G<248>	3615	338.5	17	75
413	G<250>	3594	438.5	17	75
414	G<252>	3573	338.5	17	75
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417	G<258>	3510	438.5	17	75
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420	G<264>	3447	338.5	17	75
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423	G<270>	3384	438.5	17	75
424	G<272>	3363	338.5	17	75
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427	G<278>	3300	438.5	17	75
428	G<280>	3279	338.5	17	75
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431	G<286>	3216	438.5	17	75
432	G<288>	3195	338.5	17	75
433	G<290>	3174	438.5	17	75
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435	G<294>	3132	438.5	17	75
436	G<296>	3111	338.5	17	75
437	G<298>	3090	438.5	17	75
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441	NC	3006	438.5	17	75
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443	NC	2964	438.5	17	75
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445	NC	2835	438.5	16	75
446	NC	2821	338.5	16	75
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454	S<6>	2709	338.5	16	75
455	S<7>	2695	438.5	16	75
456	S<8>	2681	338.5	16	75
457	S<9>	2667	438.5	16	75
458	S<10>	2653	338.5	16	75
459	S<11>	2639	438.5	16	75
460	S<12>	2625	338.5	16	75
461	S<13>	2611	438.5	16	75
462	S<14>	2597	338.5	16	75
463	S<15>	2583	438.5	16	75
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466	S<18>	2541	338.5	16	75

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471	S<23>	2471	438.5	16	75
472	S<24>	2457	338.5	16	75
473	S<25>	2443	438.5	16	75
474	S<26>	2429	338.5	16	75
475	S<27>	2415	438.5	16	75
476	S<28>	2401	338.5	16	75
477	S<29>	2387	438.5	16	75
478	S<30>	2373	338.5	16	75
479	S<31>	2359	438.5	16	75
480	S<32>	2345	338.5	16	75
481	S<33>	2331	438.5	16	75
482	S<34>	2317	338.5	16	75
483	S<35>	2303	438.5	16	75
484	S<36>	2289	338.5	16	75
485	S<37>	2275	438.5	16	75
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487	S<39>	2247	438.5	16	75
488	S<40>	2233	338.5	16	75
489	S<41>	2219	438.5	16	75
490	S<42>	2205	338.5	16	75
491	S<43>	2191	438.5	16	75
492	S<44>	2177	338.5	16	75
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494	S<46>	2149	338.5	16	75
495	S<47>	2135	438.5	16	75
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497	S<49>	2107	438.5	16	75
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502	S<54>	2037	338.5	16	75
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517	S<69>	1827	438.5	16	75
518	S<70>	1813	338.5	16	75
519	S<71>	1799	438.5	16	75
520	S<72>	1785	338.5	16	75
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524	S<76>	1729	338.5	16	75
525	S<77>	1715	438.5	16	75

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531	S<83>	1631	438.5	16	75
532	S<84>	1617	338.5	16	75
533	S<85>	1603	438.5	16	75
534	S<86>	1589	338.5	16	75
535	S<87>	1575	438.5	16	75
536	S<88>	1561	338.5	16	75
537	S<89>	1547	438.5	16	75
538	S<90>	1533	338.5	16	75
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541	S<93>	1491	438.5	16	75
542	S<94>	1477	338.5	16	75
543	S<95>	1463	438.5	16	75
544	S<96>	1449	338.5	16	75
545	S<97>	1435	438.5	16	75
546	S<98>	1421	338.5	16	75
547	S<99>	1407	438.5	16	75
548	S<100>	1393	338.5	16	75
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550	S<102>	1365	338.5	16	75
551	S<103>	1351	438.5	16	75
552	S<104>	1337	338.5	16	75
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562	S<114>	1197	338.5	16	75
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574	S<126>	1029	338.5	16	75
575	S<127>	1015	438.5	16	75
576	S<128>	1001	338.5	16	75
577	S<129>	987	438.5	16	75
578	S<130>	973	338.5	16	75
579	S<131>	959	438.5	16	75
580	S<132>	945	338.5	16	75
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589	S<141>	819	438.5	16	75
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591	S<143>	791	438.5	16	75
592	S<144>	777	338.5	16	75
593	S<145>	763	438.5	16	75
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595	S<147>	735	438.5	16	75
596	S<148>	721	338.5	16	75
597	S<149>	707	438.5	16	75
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599	S<151>	679	438.5	16	75
600	S<152>	665	338.5	16	75
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606	S<158>	581	338.5	16	75
607	S<159>	567	438.5	16	75
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617	S<169>	427	438.5	16	75
618	S<170>	413	338.5	16	75
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620	S<172>	385	338.5	16	75
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622	S<174>	357	338.5	16	75
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631	S<183>	231	438.5	16	75
632	S<184>	217	338.5	16	75
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636	S<188>	161	338.5	16	75
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638	S<190>	133	338.5	16	75
639	S<191>	119	438.5	16	75
640	S<192>	105	338.5	16	75
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642	S<194>	77	338.5	16	75
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649	S<201>	-21	438.5	16	75
650	S<202>	-35	338.5	16	75
651	S<203>	-49	438.5	16	75
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653	S<205>	-77	438.5	16	75
654	S<206>	-91	338.5	16	75
655	S<207>	-105	438.5	16	75
656	S<208>	-119	338.5	16	75
657	S<209>	-133	438.5	16	75
658	S<210>	-147	338.5	16	75
659	S<211>	-161	438.5	16	75
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661	S<213>	-189	438.5	16	75
662	S<214>	-203	338.5	16	75
663	S<215>	-217	438.5	16	75
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665	S<217>	-245	438.5	16	75
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667	S<219>	-273	438.5	16	75
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669	S<221>	-301	438.5	16	75
670	S<222>	-315	338.5	16	75
671	S<223>	-329	438.5	16	75
672	S<224>	-343	338.5	16	75
673	S<225>	-357	438.5	16	75
674	S<226>	-371	338.5	16	75
675	S<227>	-385	438.5	16	75
676	S<228>	-399	338.5	16	75
677	S<229>	-413	438.5	16	75
678	S<230>	-427	338.5	16	75
679	S<231>	-441	438.5	16	75
680	S<232>	-455	338.5	16	75
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682	S<234>	-483	338.5	16	75
683	S<235>	-497	438.5	16	75
684	S<236>	-511	338.5	16	75
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686	S<238>	-539	338.5	16	75
687	S<239>	-553	438.5	16	75
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690	S<242>	-595	338.5	16	75
691	S<243>	-609	438.5	16	75
692	S<244>	-623	338.5	16	75
693	S<245>	-637	438.5	16	75
694	S<246>	-651	338.5	16	75
695	S<247>	-665	438.5	16	75
696	S<248>	-679	338.5	16	75
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698	S<250>	-707	338.5	16	75
699	S<251>	-721	438.5	16	75
700	S<252>	-735	338.5	16	75
701	S<253>	-749	438.5	16	75
702	S<254>	-763	338.5	16	75

#	Pad	X	Y	W	H
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705	S<257>	-805	438.5	16	75
706	S<258>	-819	338.5	16	75
707	S<259>	-833	438.5	16	75
708	S<260>	-847	338.5	16	75
709	S<261>	-861	438.5	16	75
710	S<262>	-875	338.5	16	75
711	S<263>	-889	438.5	16	75
712	S<264>	-903	338.5	16	75
713	S<265>	-917	438.5	16	75
714	S<266>	-931	338.5	16	75
715	S<267>	-945	438.5	16	75
716	S<268>	-959	338.5	16	75
717	S<269>	-973	438.5	16	75
718	S<270>	-987	338.5	16	75
719	S<271>	-1001	438.5	16	75
720	S<272>	-1015	338.5	16	75
721	S<273>	-1029	438.5	16	75
722	S<274>	-1043	338.5	16	75
723	S<275>	-1057	438.5	16	75
724	S<276>	-1071	338.5	16	75
725	S<277>	-1085	438.5	16	75
726	S<278>	-1099	338.5	16	75
727	S<279>	-1113	438.5	16	75
728	S<280>	-1127	338.5	16	75
729	S<281>	-1141	438.5	16	75
730	S<282>	-1155	338.5	16	75
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732	S<284>	-1183	338.5	16	75
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735	S<287>	-1225	438.5	16	75
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737	S<289>	-1253	438.5	16	75
738	S<290>	-1267	338.5	16	75
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740	S<292>	-1295	338.5	16	75
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751	S<303>	-1449	438.5	16	75
752	S<304>	-1463	338.5	16	75
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754	S<306>	-1491	338.5	16	75
755	S<307>	-1505	438.5	16	75
756	S<308>	-1519	338.5	16	75
757	S<309>	-1533	438.5	16	75
758	S<310>	-1547	338.5	16	75
759	S<311>	-1561	438.5	16	75
760	S<312>	-1575	338.5	16	75
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#	Pad	X	Y	W	H
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765	S<317>	-1645	438.5	16	75
766	S<318>	-1659	338.5	16	75
767	S<319>	-1673	438.5	16	75
768	S<320>	-1687	338.5	16	75
769	S<321>	-1701	438.5	16	75
770	S<322>	-1715	338.5	16	75
771	S<323>	-1729	438.5	16	75
772	S<324>	-1743	338.5	16	75
773	S<325>	-1757	438.5	16	75
774	S<326>	-1771	338.5	16	75
775	S<327>	-1785	438.5	16	75
776	S<328>	-1799	338.5	16	75
777	S<329>	-1813	438.5	16	75
778	S<330>	-1827	338.5	16	75
779	S<331>	-1841	438.5	16	75
780	S<332>	-1855	338.5	16	75
781	S<333>	-1869	438.5	16	75
782	S<334>	-1883	338.5	16	75
783	S<335>	-1897	438.5	16	75
784	S<336>	-1911	338.5	16	75
785	S<337>	-1925	438.5	16	75
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790	S<342>	-1995	338.5	16	75
791	S<343>	-2009	438.5	16	75
792	S<344>	-2023	338.5	16	75
793	S<345>	-2037	438.5	16	75
794	S<346>	-2051	338.5	16	75
795	S<347>	-2065	438.5	16	75
796	S<348>	-2079	338.5	16	75
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800	S<352>	-2135	338.5	16	75
801	S<353>	-2149	438.5	16	75
802	S<354>	-2163	338.5	16	75
803	S<355>	-2177	438.5	16	75
804	S<356>	-2191	338.5	16	75
805	S<357>	-2205	438.5	16	75
806	S<358>	-2219	338.5	16	75
807	S<359>	-2233	438.5	16	75
808	S<360>	-2247	338.5	16	75
809	S<361>	-2261	438.5	16	75
810	S<362>	-2275	338.5	16	75
811	S<363>	-2289	438.5	16	75
812	S<364>	-2303	338.5	16	75
813	S<365>	-2317	438.5	16	75
814	S<366>	-2331	338.5	16	75
815	S<367>	-2345	438.5	16	75
816	S<368>	-2359	338.5	16	75
817	S<369>	-2373	438.5	16	75
818	S<370>	-2387	338.5	16	75
819	S<371>	-2401	438.5	16	75
820	S<372>	-2415	338.5	16	75

#	Pad	X	Y	W	H
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823	S<375>	-2457	438.5	16	75
824	S<376>	-2471	338.5	16	75
825	S<377>	-2485	438.5	16	75
826	S<378>	-2499	338.5	16	75
827	S<379>	-2513	438.5	16	75
828	S<380>	-2527	338.5	16	75
829	S<381>	-2541	438.5	16	75
830	S<382>	-2555	338.5	16	75
831	S<383>	-2569	438.5	16	75
832	S<384>	-2583	338.5	16	75
833	S<385>	-2597	438.5	16	75
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875	G<265>	-3447	438.5	17	75
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878	G<259>	-3510	338.5	17	75
879	G<257>	-3531	438.5	17	75

#	Pad	X	Y	W	H
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900	G<215>	-3972	338.5	17	75
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937	G<141>	-4749	438.5	17	75
938	G<139>	-4770	338.5	17	75

#	Pad	X	Y	W	H
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941	G<133>	-4833	438.5	17	75
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943	G<129>	-4875	438.5	17	75
944	G<127>	-4896	338.5	17	75
945	G<125>	-4917	438.5	17	75
946	G<123>	-4938	338.5	17	75
947	G<121>	-4959	438.5	17	75
948	G<119>	-4980	338.5	17	75
949	G<117>	-5001	438.5	17	75
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976	G<63>	-5568	338.5	17	75
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#	Pad	X	Y	W	H
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982	G<51>	-5694	338.5	17	75
983	G<49>	-5715	438.5	17	75
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985	G<45>	-5757	438.5	17	75
986	G<43>	-5778	338.5	17	75
987	G<41>	-5799	438.5	17	75
988	G<39>	-5820	338.5	17	75
989	G<37>	-5841	438.5	17	75
990	G<35>	-5862	338.5	17	75
991	G<33>	-5883	438.5	17	75
992	G<31>	-5904	338.5	17	75
993	G<29>	-5925	438.5	17	75
994	G<27>	-5946	338.5	17	75
995	G<25>	-5967	438.5	17	75
996	G<23>	-5988	338.5	17	75
997	G<21>	-6009	438.5	17	75
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999	G<17>	-6051	438.5	17	75
1000	G<15>	-6072	338.5	17	75
1001	G<13>	-6093	438.5	17	75
1002	G<11>	-6114	338.5	17	75
1003	G<9>	-6135	438.5	17	75
1004	G<7>	-6156	338.5	17	75
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1006	G<3>	-6198	338.5	17	75
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1008	GD<1>	-6240	338.5	17	75
1009	NC	-6261	438.5	17	75
1010	NC	-6282	338.5	17	75
1011	NC	-6303	438.5	17	75
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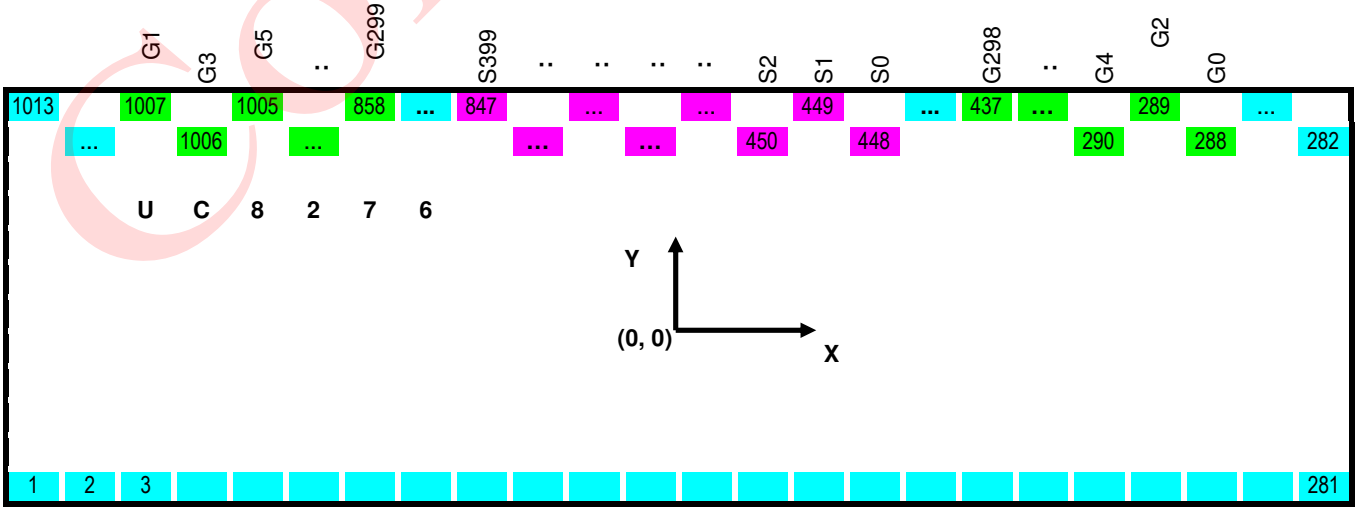
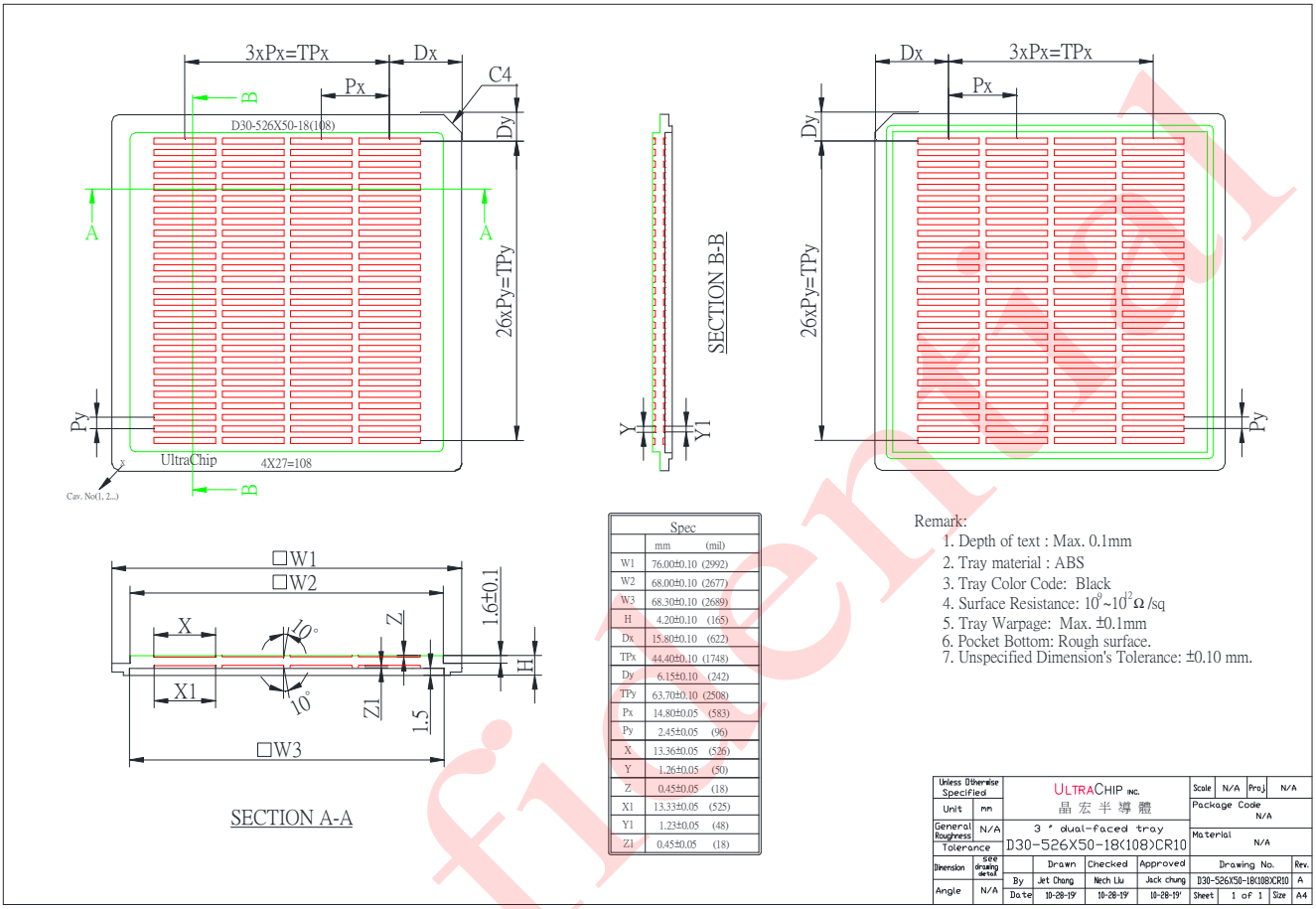
1013	NC	-6345	438.5	17	75

Output Pad Location



TRAY INFORMATION

3 Inch Tray



Spec		
	mm	(mil)
W1	76.00±0.10	(2992)
W2	68.00±0.10	(2677)
W3	68.30±0.10	(2689)
H	4.20±0.10	(165)
Dx	15.80±0.10	(622)
TPx	44.40±0.10	(1748)
Dy	6.15±0.10	(242)
TPy	63.70±0.10	(2508)
Px	14.80±0.05	(583)
Py	2.45±0.05	(96)
X	13.36±0.05	(526)
Y	1.26±0.05	(50)
Z	0.45±0.05	(18)
X1	13.33±0.05	(525)
Y1	1.23±0.05	(48)
Z1	0.45±0.05	(18)

Remark:
1. Depth of text : Max. 0.1mm
2. Tray material : ABS
3. Tray Color Code: Black
4. Surface Resistance: 10^{9}~10^{12}Ω /sq
5. Tray Warpage: Max. ±0.1mm
6. Pocket Bottom: Rough surface.
7. Unspecified Dimension's Tolerance: ±0.10 mm.

Unless Otherwise Specified		ULTRACHIP INC. 晶宏半導體			Scale	N/A	Proj	N/A
Unit	mm				Package Code	N/A		
General Roughness	N/A	3 " dual-faced tray D30-526X50-18(108)CR10			Material	N/A		
Tolerance								
Dimension	see drawing detail		Drawn	Checked	Approved	Drawing No.		Rev.
Angle	N/A	By	Jet Chang	Nech Liu	Jack chung	D30-526X50-18(108)CR10		A
		Date	10-28-19'	10-28-19'	10-28-19'	Sheet	1 of 1	Size	A4

REVISION HISTORY

Revision	Contents	Date
0.1	NA	Feb.21,2019
0.6	1. page 16 , POWER SETTING (PWR) : VCOM_SLEW & explanation 2. page 22, VSL-VCOM_DC → VSL+VCOM_DC 3. page 32 , RESOLUTION SETTING (TRES) : modify example 4. page 33, REVISION (REV) : correct typo 5. page 72, Modify tray drawing	Nov, 19, 2019