HIGH-VOLTAGE MIXED-SIGNAL IC

UC8175

All-in-one driver w/ Timing Controller

PP Specifications
Datasheet Revision: 0.8 (for TFT Module Use only)

IC Version: c_B
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ULTRACHIP

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UC8175

All-in-one driver IC with Timing Controller

INTRODUCTION

The UC8175 is an all-in-one driver with timing controller. Its output is of 1-bit white/black resolution per pixel. The timing controller provides control signals for source driver and gate driver.

The DC-DC controller allows it to generate the source output voltage VDH/VDL (±2.4V~±11.0V). The chip also includes an output buffer for the supply of the COM electrode (DC-VCOM). The system is configurable through a 3-wire/4-wire (SPI) serial interface.

MAIN APPLICATIONS

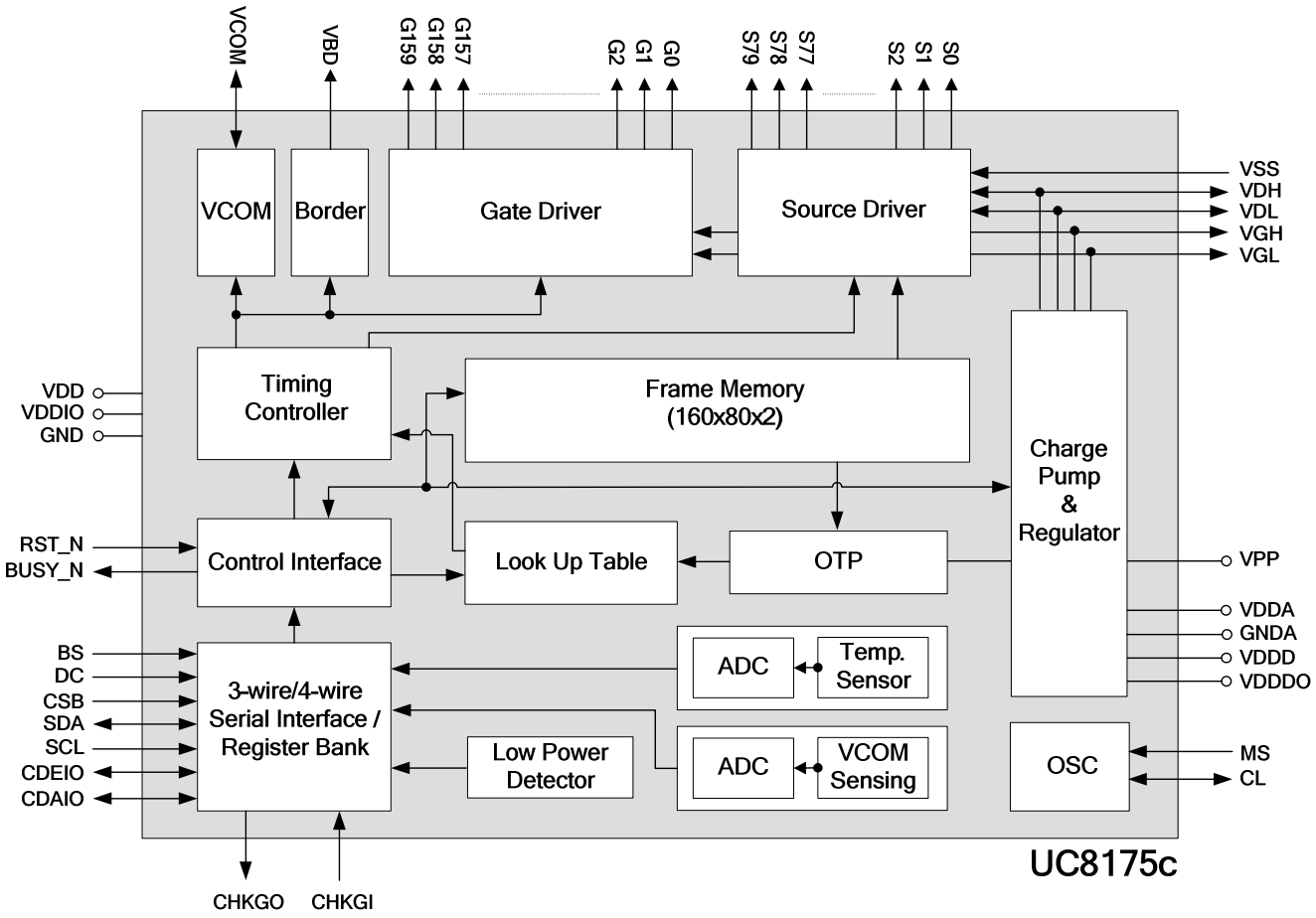
- Cards

FEATURE HIGHLIGHTS

- System-on-chip (SOC)
- Resolution
  - Up to 80(source)x160(gate) resolution + 1 border + 1 VCOM
  - 2-bit white/black
- Memory: 80 x 160 x 2 bits SRAM
- Cascade: 2 or more chips cascade mode
- MCU I/F: 3-wire/4-wire SPI
- On-Chip Thermal Sensor range: -25°C ~ 50°C
  Deviation: ± 2°C / 8-bit status
- LPD: Low power detection (VDD<2.5V)
- OSC / PLL: On-chip RC oscillator
- VCOM: DC-VCOM, -0.1V ~ -3.0V (step 0.05V)
- Charge Pump and Regulator:
  (1) VGH: +11V ~ +16V (programmable, step 1V)
  (2) VGL: -11V ~ -16V (programmable, step 1V)
  (3) VDH: +2.4V ~ +11.0V (programmable, step 0.2V)
  (4) VDL: -2.4V ~ -11.0V (programmable, step 0.2V)
- OTP for LUTs and settings
- Power Supply: 2.3V ~ 3.6V
- Die size: 3500uM x 2700uM
- Pad Pitch: 30uM
- Package: COG

Remark: The inspection standard of the product appearance is based on Ultrachip's inspection document.

BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Description
UC8175cHAA-U0X2-3	IC Thickness: 230uM, with double-faced 3" tray

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

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PIN DESCRIPTION

Type: I: Input, O: Output, I/O: Input/Output, PWR: Power, C: Capacitor pin

Pin (Pad) Name	Pin Count	Type	Description
POWER SUPPLY PINS			
VDD	5	PWR	Digital power
VDDA	2	PWR	Analog power
VDDIO	2	PWR	IO power
VPP	2	PWR	OTP program power
GND	5	PWR	Digital Ground
GNDA	2	PWR	Analog Ground
VDM	8	PWR	Analog Ground.
LDO PINS			
VDDD	1	PWR	Digital power input (1.8V)
VDDDO	1	PWR	Digital power output (1.8V)
VDH	2	I/O	Positive source driver Voltage (+2.4V ~ +11V)
VDL	2	I/O	Negative source driver voltage (-2.4V ~ -11V)
CONTROL INTERFACE PINS			
BS	1	I	Bus Selection. Select 3-wire / 4-wire SPI interface L: 4-wire interface. H: 3-wire interface.
RST_N	1	I (Pull-up)	Global reset pin. Low: active. When RST_N becomes low, driver will reset. All registers will reset to default value. All driver functions will be disabled. Source/Gate/Border/VCOM will be released to floating. The minimal width of RST_N=low is 100uS.
MS	1	I	Cascade setting pin. L: Slave chip. H: Master chip.
CL	1	I/O	Clock input/output pin. Leave it open if not used. Master: Clock output. Slave: Clock input.
CDEIO	1	I/O	Cascade pin. Leave it open if not used.
CDAIO	1	I/O	Cascade pin. Leave it open if not used.
BUSY_N	1	O	Driver busy flag. L: Driver is Busy. H: Host side can send command/data to driver.
MCU INTERFACE (SPI) PINS			
CSB	1	I	Serial communication chip select.
SDA	1	I/O	Serial communication data input/output
SCL	1	I	Serial communication clock input.
DC	1	I	Command/Data input. L: command H: data Connect to GND if BS=High.

Pin (Pad) Name	Pin Count	Type	Description
CHARGE PUMP PINS			
C1P, C1N C2P, C2N C3P, C3N C4P, C4N C5P, C5N C6P, C6N	2, 2 2, 2 2, 2 2, 2 2, 2 2, 2	PWR	Capacitor connecting pins on the positive/negative side
VCOMH	2	PWR	Positive pumping voltage for internal use
VCOML	2	PWR	Negative pumping voltage for internal use
VGH	4	PWR	Positive gate driver voltage (+11V ~ +16V)
VGL	4	PWR	Negative gate driver voltage (-11V ~ -16V)
OUTPUT PINS			
S0~S79 (S<0>~S<79>)	80	O	Source driver output signals.
G0~G159 (G<0>~G<159>)	160	O	Gate driver output signals.
VCOM	4	O	VCOM output.
VBD (Border<1>, Border<2>)	 1, 1	O	Border output pins.
CHECK PANEL PINS			
CHKGI	1	I (Pull-down)	Check panel break input. Leave open if it is not used.
CHKGO	1	O	Check panel break output. Leave open if it is not used.
RESERVED PINS			
TEST2	1	O	Leave open.
TEST3~TEST5	1x3	I	Leave open.
DUMMY	12	-	Leave open.

COMMAND TABLE

W/R: 0: Write Cycle 1: Read Cycle C/D: 0: Command / 1: Data D7~D0: –: Don't Care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0		Default
1.	PSR	W	0	0	0	0	0	0	0	0	0		00H
		W	1	#	#	#	#	#	#	#	#	RES[1:0], REG[1:0], UD, SHL, SHD_N, RST_N	0FH
2.	PWR	W	0	0	0	0	0	0	0	0	1		01H
		W	1	-	-	-	-	-	-	#	#	VDS_EN, VDG_EN	03H
		W	1	-	-	-	-	-	#	#	#	VDG_LVL[2:0]	00H
		W	1	-	-	#	#	#	#	#	#	VDH_LVL[5:0]	26H
		W	1	-	-	#	#	#	#	#	#	VDL_LVL[5:0]	26H
3.	POF	W	0	0	0	0	0	0	0	1	0		02H
4.	PFS	W	0	0	0	0	0	0	0	1	1		03H
		W	1	-	-	#	#	-	-	-	-	T_OFF[1:0]	00H
5.	PON	W	0	0	0	0	0	0	1	0	0		04H
6.	PMES	W	0	0	0	0	0	0	1	0	1		05H
7.	CPSET	W	0	0	0	0	0	0	1	1	0		06H
		W	1	-	-	#	#	#	#	#	#	CPINT[1:0], CPS[1:0], CPFRQ[1:0]	0FH
8.	DSLP	W	0	0	0	0	0	0	1	1	1		07H
		W	1	#	#	#	#	#	#	#	#	Check code = A5H	A5H
9.	DTM1	W	0	0	0	0	1	0	0	0	0		10H
		W	1	#	#	#	#	#	#	#	#	Pixel(1)..Pixel(8)	00H
		W	1	…	…	…	…	…	…	…	…	~	00H
		W	1	#	#	#	#	#	#	#	#	Pixel(N-7)..Pixel(N)	00H
10.	DSP	W	0	0	0	0	1	0	0	0	1		11H
		R	1	#	-	-	-	-	-	-	-	Data_flag	00H
11.	DRF	W	0	0	0	0	1	0	0	1	0		12H
12.	DTM2	W	0	0	0	0	1	0	0	1	1		13H
		W	1	#	#	#	#	#	#	#	#	Pixel(1)..Pixel(8)	00H
		W	1	…	…	…	…	…	…	…	…	~	00H
		W	1	#	#	#	#	#	#	#	#	Pixel(N-7)..Pixel(N)	00H
13.	AUTO	W	0	0	0	0	1	0	1	1	1		17H
		W	1	#	#	#	#	#	#	#	#	Check code = A5H / A7H	00H
14.	LUTW (43-byte command, structure of bytes 2~7 repeated 7 times)	W	0	0	0	1	0	0	0	1	1		23H
		W	1	#	#	#	#	#	#	#	#	Phase 0 [1:0] ~ Phase 3 [1:0]	00H
		W	1	#	#	#	#	#	#	#	#	Number of Frame 0 [7:0]	00H
		W	1	#	#	#	#	#	#	#	#	Number of Frame 1 [7:0]	00H
		W	1	#	#	#	#	#	#	#	#	Number of Frame 2 [7:0]	00H
		W	1	#	#	#	#	#	#	#	#	Number of Frame 3 [7:0]	00H
		W	1	#	#	#	#	#	#	#	#	Times to Repeat [7:0]	00H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0		Default
15.	LUTB (43-byte command, structure of bytes 2~7 repeated 7 times)	W	0	0	0	1	0	0	1	0	0		24H
		W	1	#	#	#	#	#	#	#	#	Phase 0 [1:0] ~ Phase 3 [1:0]	00H
		W	1	#	#	#	#	#	#	#	#	Number of Frame 0 [7:0]	00H
		W	1	#	#	#	#	#	#	#	#	Number of Frame 1 [7:0]	00H
		W	1	#	#	#	#	#	#	#	#	Number of Frame 2 [7:0]	00H
		W	1	#	#	#	#	#	#	#	#	Number of Frame 3 [7:0]	00H
		W	1	#	#	#	#	#	#	#	#	Times to Repeat [7:0]	00H
16.	LUTOPT	W	0	0	0	1	0	1	0	1	0		2AH
		W	1	#	#	#	#	#	#	#	#	EOPT, STAGE_XON[6:0]	00H
17.	PLL	W	0	0	0	1	1	0	0	0	0		30H
		W	1	-	-	#	#	#	#	#	#	FR[5:0]	13H
18.	TSC	W	0	0	1	0	0	0	0	0	0		40H
		R	1	#	#	#	#	#	#	#	#	TS[7:0]	00H
19.	TSE	W	0	0	1	0	0	0	0	0	1		41H
		W	1	0	-	-	-	#	#	#	#	TO[3:0]	00H
20.	PBC	W	0	0	1	0	0	0	1	0	0		44H
		R	1	#	#	#	#	#	#	#	#	PSTA	00H
21.	CDI	W	0	0	1	0	1	0	0	0	0		50H
		W	1	#	#	#	#	-	#	#	#	VBD[1:0], DDX[1:0], CDI[2:0]	D2H
22.	LPD	W	0	0	1	0	1	0	0	0	1		51H
		R	1	-	-	-	-	-	-	-	#	LPD	01H
23.	TCON	W	0	0	1	1	0	0	0	0	0		60H
		W	1	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	22H
24.	TRES	W	0	0	1	1	0	0	0	0	1		61H
		W	1	-	#	#	#	#	0	0	0	HRES[6:3]	00H
		W	1	#	#	#	#	#	#	#	#	VRES[7:0]	00H
25.	GSST	W	0	0	1	1	0	0	1	0	1		65H
		W	1	-	#	#	#	#	0	0	0	HST[6:3]	00H
		W	1	#	#	#	#	#	#	#	#	VST[7:0]	00H
26.	REV	W	0	0	1	1	1	0	0	0	0		70H
		R	1	#	#	#	#	#	#	#	#	LUT_REV0[7:0]	FFH
		R	1	#	#	#	#	#	#	#	#	LUT_REV1[7:0]	FFH
27.	FLG	W	0	0	1	1	1	0	0	0	1		71H
		R	1	#	#	-	-	#	#	#	#	CPOK, PTL_flag, data_flag, PON, POF, BUSY_N	02H
28.	CRC	W	0	0	1	1	1	0	0	1	0		72H
		R	1	#	#	#	#	#	#	#	#	CRC_MSB[7:0]	FFH
		R	1	#	#	#	#	#	#	#	#	CRC_LSB[7:0]	FFH
29.	AMV	W	0	1	0	0	0	0	0	0	0		80H
		W	1	-	-	#	#	#	#	#	#	AMVT[1:0], XON, AMVS, AMV, AMVE	10H
30.	VV	W	0	1	0	0	0	0	0	0	1		81H
		R	1	-	-	#	#	#	#	#	#	VV[5:0]	00H
31.	VDCS	W	0	1	0	0	0	0	0	1	0		82H
		W	1	-	-	#	#	#	#	#	#	VDCS[5:0]	00H

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0		Default
32.	PTL	W	0	1	0	0	1	0	0	0	0		90H
		W	1	-	#	#	#	#	0	0	0	HRST[6:3]	00H
		W	1	-	#	#	#	#	1	1	1	HRED[6:3]	07H
		W	1	#	#	#	#	#	#	#	#	VRST[7:0]	00H
		W	1	#	#	#	#	#	#	#	#	VRED[7:0]	00H
		W	1	-	-	-	-	-	-	-	#	PTL_SCAN	01H
33.	PIN	W	0	1	0	0	1	0	0	0	1		91H
34.	POUT	W	0	1	0	0	1	0	0	1	0		92H
35.	PGM	W	0	1	0	1	0	0	0	0	0		A0H
		W	1	-	-	-	-	-	#	#	#	RGSET[2:0]	04H
36.	APG	W	0	1	0	1	0	0	0	0	1		A1H
37.	ROTP	W	0	1	0	1	0	0	0	1	0		A2H
		R	1	#	#	#	#	#	#	#	#	Dummy	--
		R	1	#	#	#	#	#	#	#	#	Data of Address = 0	--
		R	1	:	:	:	:	:	:	:	:	:	--
		R	1	#	#	#	#	#	#	#	#	Data of Address = n	--
38.	CCSET	W	0	1	1	1	0	0	0	0	0		E0H
		W	1	-	-	-	-	-	-	#	#	TSFIX, CCEN	00H
39.	PWS	W	0	1	1	1	0	0	0	1	1		E3H
		W	1	#	#	#	#	#	#	#	#	BD_W[3:0], SD_W[3:0]	33H
40.	LVSEL	W	0	1	1	1	0	0	1	0	0		E4H
		W	1	-	-	-	-	-	-	#	#	LVD_SEL[1:0]	03H
41.	TSSET	W	0	1	1	1	0	0	1	0	1		E5H
		W	1	#	#	#	#	#	#	#	#	TS_SET[7:0]	00H

Note: (1) All other register addresses are invalid or reserved by UltraChip, and should NOT be used.

(2) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.

(3) Commands are processed on the 'stop' condition of the interface.

(4) Registers marked 'W/R' can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.

COMMAND DESCRIPTION

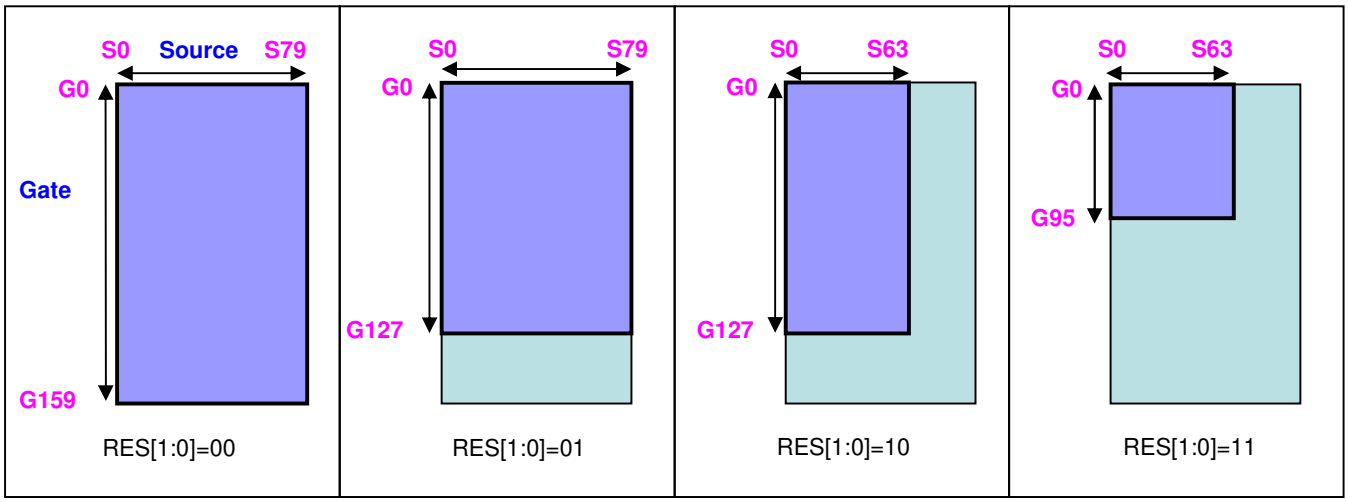
W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: –: Don't Care

(1) PSR (R00H)

Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Panel Setting Registers	W	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	00H
	W	1	RES[1:0]		REG[1:0]		UD	SHL	SHD_N	RST_N	0FH

RES[1:0]: Resolution Setting

00b: 80 x 160 (source x gate) **(Default)**
01b: 80 x 128 (source x gate)
10b: 64 x 128 (source x gate)
11b: 64 x 96 (source x gate)



Minimum active GD is always G0 regardless of <UD> (R00H).

Minimum active SD is always S0 regardless of <SHL> (R00H).

REG[1:0]: LUT select

00b: Reserved **(Default)** 01b: LUT from OTP.
10b: LUT from registers. 11b: LUT from registers.

UD: Gate Scan Direction

0: Scan down. First line = Gn-1 → Gn-2 → ⋯ → G1 → G0.
1: Scan up. First line = G0 → G1 → ⋯ → Gn-2 → Gn-1. **(Default)**

SHL: Source Shift Direction

0: Shift left. First data = Sn-1 → Sn-2 → ⋯ → S1 → S0.
1: Shift right. **(Default)** First data = S0 → S1 → ⋯ → Sn-2 → Sn-1

SHD_N: Charge pump Switch

0: Charge pump OFF
1: Charge pump ON **(Default)**

When SHD_N becomes LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF. And Source/Gate/Border/VCOM will be released to floating.

RST_N: Soft Reset

0: Reset. Charge pump OFF, Register data are set to their default values, all drivers will be reset, and all functions will be disabled. Source/Gate/Border/VCOM will be released to floating. After soft reset is transmitted, the internal operation needs at least 50us to execute. During this period of time, the BUSY_N pin keeps low and any command will be ignored.

1: No effect. **(Default)**

(2) PWR (R01H)

Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power Setting	W	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	01H
	W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03H
	W	1	-	-	-	-	-	VDG_LVL[2:0]			00H
	W	1	-	-	VDH_LVL[5:0]						26H
	W	1	-	-	VDL_LVL[5:0]						26H

VDS_EN: Source Power Selection

0: External source power from VDH/VDL pins
1 Internal voltage generation circuit for both VDH/VDL (Default)

VDG_EN: Gate Power Selection

0: External gate power from VGH/VGL pins
1: Internal voltage generation circuit for both VGH/VGL (Default)

VDG_LVL[2:0]: VGH / VGL Voltage Level selection

VGHL_LV	VGHL Voltage Level
000 (Default)	VGH=16V, VGL= -16V
001	VGH=15V, VGL= -15V
010	VGH=14V, VGL= -14V
011	VGH=13V, VGL= -13V
100	VGH=12V, VGL= -12V
101	VGH=11V, VGL= -11V
others	VGH=11V, VGL= -11V

VDH_LVL[5:0]: Internal VDH power selection.(**Default value: 100110b**)

VDH	Voltage	VDH	Voltage	VDH	Voltage	VDH	Voltage
000000	2.4 V	001100	4.8 V	011000	7.2 V	100100	9.6 V
000001	2.6 V	001101	5.0 V	011001	7.4 V	100101	9.8 V
000010	2.8 V	001110	5.2 V	011010	7.6 V	100110	10.0V
000011	**3.0 V**	001111	5.4 V	011011	7.8 V	100111	10.2 V
000100	3.2 V	010000	5.6 V	011100	8.0 V	101000	10.4 V
000101	3.4 V	010001	5.8 V	011101	8.2V	101001	10.6 V
000110	3.6 V	010010	6.0 V	011110	8.4 V	101010	10.8 V
000111	3.8 V	010011	6.2 V	011111	8.6 V	101011	11.0 V
001000	4.0 V	010100	6.4 V	100000	8.8 V	(others)	11.0 V
001001	4.2 V	010101	6.6 V	100001	9.0 V		
001010	4.4 V	010110	6.8 V	100010	9.2 V		
001011	4.6 V	010111	7.0 V	100011	9.4 V		

VDL_LVL[5:0]: Internal VDL power selection.(**Default value: 100110b**)

VDL	Voltage	VDL	Voltage	VDL	Voltage	VDL	Voltage
000000	-2.4 V	001100	-4.8 V	011000	-7.2 V	100100	-9.6 V
000001	-2.6 V	001101	-5.0 V	011001	-7.4 V	100101	-9.8 V
000010	-2.8 V	001110	-5.2 V	011010	-7.6 V	100110	-10.0 V
000011	-3.0 V	001111	-5.4 V	011011	-7.8 V	100111	-10.2 V
000100	-3.2 V	010000	-5.6 V	011100	-8.0 V	101000	-10.4 V
000101	-3.4 V	010001	-5.8 V	011101	-8.2 V	101001	-10.6 V
000110	-3.6 V	010010	-6.0 V	011110	-8.4 V	101010	-10.8 V
000111	-3.8 V	010011	-6.2 V	011111	-8.6 V	101011	-11.0 V
001000	-4.0 V	010100	-6.4 V	100000	-8.8 V	(others)	-11.0 V
001001	-4.2 V	010101	-6.6 V	100001	-9.0 V		
001010	-4.4 V	010110	-6.8 V	100010	-9.2 V		
001011	-4.6 V	010111	-7.0 V	100011	-9.4 V		

(3) POF (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power Off	W	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	02H

After the Power OFF command, the driver will be powered OFF. Refer to the POWER MANAGEMENT section for the sequence.

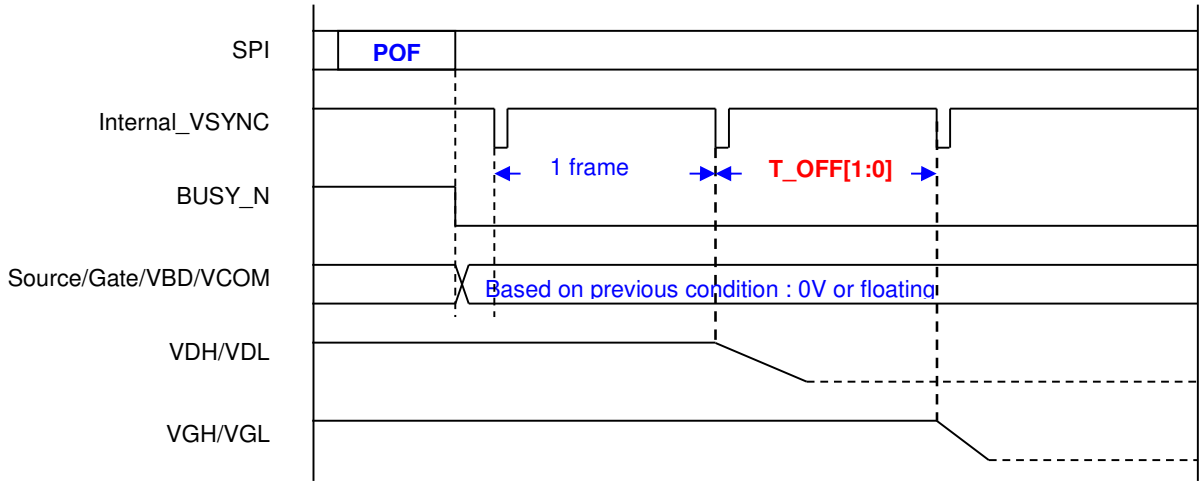
This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode. Source/Gate/Border/VCOM will be released to floating.

(4) PFS (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power OFF Sequence	W	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	03H
	W	1	**-**	**-**	T_OFF[1:0]		**-**	**-**	**-**	**-**	00H

T_VDS_OFF[1:0]: Source to gate power off interval time.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame



(5) PON (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power ON	W	0	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	04H

After the Power ON command, the driver will be powered ON. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUSY_N signal will return to high.

(6) PMES (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power ON Measure	W	0	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	05H

This command enables the internal bandgap, which will be cleared by the next POF.

(7) CPSET (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Charge Pump Setting	W	0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	06H
	W	1	**-**	**-**	CPINT[1:0]		CPS[1:0]		CPFRQ[1:0]		0FH

CPINT[1:0]: Charge pump time interval

00b: 20mS (Default) 01b: 30mS 10b: 40mS 11b: 50mS

CPS[1:0]: Charge pump driving strength

00b: Strength 1 01b: Strength 2 10b: Strength 3 **11b: Strength 4 (Default)**

CPFRQ[1:0]: Charge pump frequency setting

00b: 1 KHz 01b: 2 KHz 10b: 4 KHz **11b: 8 KHz (Default)**

(8) DSLP (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Deep Sleep	W	0	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	07H
	W	1	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	A5H

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

(9) DTM1 (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Data Transmission 1	W	0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	10H
	W	1	Pixel(1)	Pixel(2)	Pixel(3)	Pixel(4)	Pixel(5)	Pixel(6)	Pixel(7)	Pixel(8)	00H
	W	1	**…**	**…**	**…**	**…**	**…**	**…**	**…**	**…**	00H
	W	1	**…**	**…**	**…**	**…**	**…**	**…**	Pixel(N-1)	Pixel(N)	00H

This command starts transmitting “OLD” data and write them into SRAM.

In Program mode, this command writes “OTP” data to SRAM for programming.

(10) DSP (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Data Stop	W	0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**1**	11H
	R	1	Data_flag	**-**	**-**	**-**	**-**	**-**	**-**	**-**	00H

Check the completeness of data. If data is complete, start to refresh display.

Data_flag: Data flag of receiving user data.

0: Driver didn’t receive all the data. **(Default)**
1: Driver has already received all the one-frame data (DTM1 and DTM2).

After “Data Start” (R10h) or “Data Stop” (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY_N signal will become “0”.

(11) DRF (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Data Refresh	W	0	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	12H

While user sends this command, the driver will refresh display according to SRAM data and LUT.

After the Display Refresh command, BUSY_N signal will become “0” and the refreshing of panel starts.

The waiting interval form BUSY_N falling to the first FLG command must be longer than 200uS.

(12) DTM2 (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Data Transmission 2	W	0	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	13H
	W	1	Pixel(1)	Pixel(2)	Pixel(3)	Pixel(4)	Pixel(5)	Pixel(6)	Pixel(7)	Pixel(8)	00H
	W	1	…	…	…	…	…	…	…	…	00H
	W	1	…	…	…	…	…	…	Pixel(N-1)	Pixel(N)	00H

This command starts transmitting “NEW” data and write them into SRAM.

(13) AUTO (R17H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Auto Sequence	W	0	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**1**	17H
	W	1	Check code = A5h / A7h								--

The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to aviod unnecessary power consumption and reduce the complexity of the host's control procedure.The sequence contains several operations, including PON, DRF, POF, and DSLP.

AUTO(0x17) + Code(0xA5) = (PON → DRF → POF)

AUTO(0x17) + Code(0xA7) = (PON → DRF → POF → DSLP)

(14) LUTW (R23H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Look-up Table for White (43-byte command) The data of bytes 2~7 describes one stage, and there are 7 stages in the LUT.	W	0	**0**	**0**	**1**	**0**	**0**	**0**	**1**	**1**	23H
	W	1	Phase 0		Phase 1		Phase 2		Phase 3		00H
	W	1	Number of frame 0								00H
	W	1	Number of frame 1								00H
	W	1	Number of frame 2								00H
	W	1	Number of frame 3								00H
	W	1	Times to Repeat								00H

This command stores White Look-Up Table with 7 groups of data. Each group contains information for one stage and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.

Bytes 2, 8, 14, 20, 26, 32, 38:

Phase

00b: GND
01b: VDH
10b: VDL
11b: Floating

Bytes 3~6, 9~12, 15~18, 21~24, 27~30, 33~36, 39~42:

Number of Frame

0000 0000b: 0 frame

: :

: :

1111 1111b: 255 frames

Bytes 7, 13, 19, 25, 31, 37, 43:

Times to Repeat

0000 0000b: 0 time

: :

: :

1111 1111b: 255 times

(15) LUTB (R24H)

This command builds Look-up Table for Black. Please refer to White LUT (LUTW) for similar definition details.

(16) LUTOPT (R2AH)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
LUT Option	W	0	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**0**	2AH
	W	1	EOPT	STAGE_XON[6:0]							00H

This command sets XON and the options of LUT.

EOPT: LUT sequence option

STAGE_XON[6:0]:

All Gate ON (Each bit controls one stage, STAGE_XON [0] for stage-1, STAGE_XON [1] for stage-2 …..)

000 0000b: no All-Gate-ON

000 0001b: Stage-1 All-Gate-ON

000 0011b: Stage-1 and Stage-2 All-Gate-ON

: :

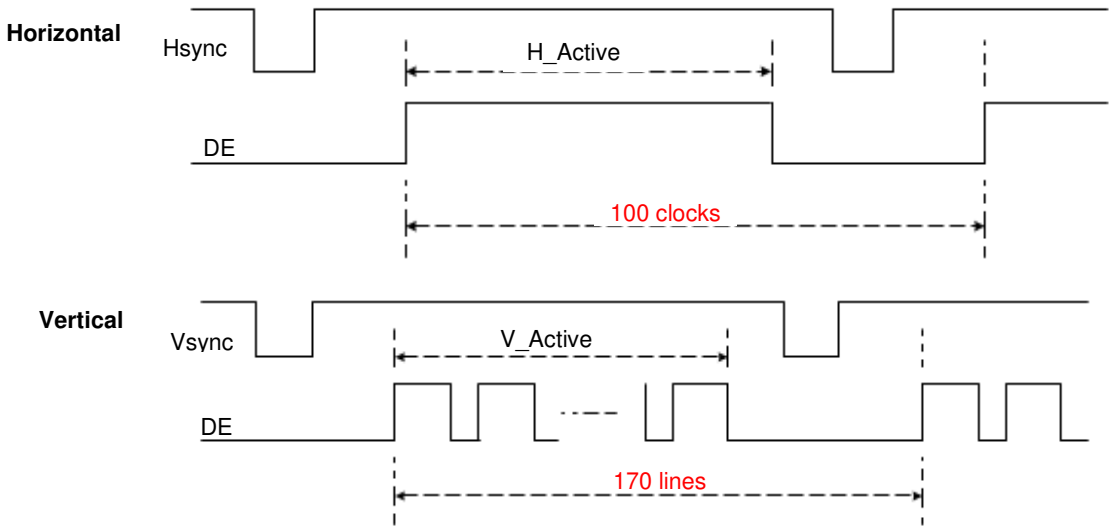
(17) PLL (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
PLL	W	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	30H
	W	1	**-**	**-**	FR[5:0]						13H

The command controls the clock frequency.

The structure supports the following frame rates:

FR[5:0]	Frame Rate	FR[5:0]	Frame Rate	FR[5:0]	Frame Rate	FR[5:0]	Frame Rate
000000	2.5 Hz	001100	32.5 Hz	011000	62.5 Hz	100100	92.5 Hz
000001	5.0 Hz	001101	35.0 Hz	011001	65.0 Hz	100101	95.0 Hz
000010	7.5 Hz	001110	37.5 Hz	011010	67.5 Hz	100110	97.5 Hz
000011	10.0 Hz	001111	40.0 Hz	011011	70.0 Hz	100111	100.0 Hz
000100	12.5 Hz	010000	42.5 Hz	011100	72.5 Hz	others	100.0 Hz
000101	15.0 Hz	010001	45.0 Hz	011101	75.0 Hz		
000110	17.5 Hz	010010	47.5 Hz	011110	77.5 Hz		
000111	20.0 Hz	**010011**	**50.0 Hz**	011111	80.0 Hz		
001000	22.5 Hz	010100	52.5 Hz	100000	82.5 Hz		
001001	25.0 Hz	010101	55.0 Hz	100001	85.0 Hz		
001010	27.5 Hz	010110	57.5 Hz	100010	87.5 Hz		
001011	30.0 Hz	010111	60.0 Hz	100011	90.0 Hz		



(18) TSC (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Temperature Sensor Command	W	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	40H
	R	1	TS[7:0]								00H

This command enables internal or external temperature sensor, and reads the result.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

TS[7:0]	Temperature (°C)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
1110_1110	-18
1110_1111	-17
1111_0000	-16
1111_0001	-15
1111_0010	-14
1111_0011	-13
1111_0100	-12
1111_0101	-11
1111_0110	-10
1111_0111	-9
1111_1000	-8
1111_1001	-7
1111_1010	-6
1111_1011	-5
1111_1100	-4
1111_1101	-3
1111_1110	-2
1111_1111	-1

TS[7:0]	Temperature(°C)
0000_0000	**0**
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
0000_0111	7
0000_1000	8
0000_1001	9
0000_1010	10
0000_1011	11
0000_1100	12
0000_1101	13
0000_1110	14
0000_1111	15
0001_0000	16
0001_0001	17
0001_0010	18
0001_0011	19
0001_0100	20
0001_0101	21
0001_0110	22
0001_0111	23
0001_1000	24

TS[7:0]	Temperature(°C)
0001_1001	25
0001_1010	26
0001_1011	27
0001_1100	28
0001_1101	29
0001_1110	30
0001_1111	31
0010_0000	32
0010_0001	33
0010_0010	34
0010_0011	35
0010_0100	36
0010_0101	37
0010_0110	38
0010_0111	39
0010_1000	40
0010_1001	41
0010_1010	42
0010_1011	43
0010_1100	44
0010_1101	45
0010_1110	46
0010_1111	47
0011_0000	48
0011_0001	49

(19) TSE (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Temperature Sensor Selection	W	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	41H
	W	1	**0**	**-**	**-**	**-**	TO[3:0]				00H

This command selects temperature option.

TO[3:0]: Temperature offset.

TO[3:0]	Calculation
0000 b	**+0 (Default)**
0001	+1
0010	+2
0011	+3
0100	+4
0101	+5
0110	+6
0111	+7

TO[3:0]	Calculation
1000	-8
1001	-7
1010	-6
1011	-5
1100	-4
1101	-3
1110	-2
1111	-1

(20) PBC (R44H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Panel Break Check	W	0	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**	44H
	R	1	**0**	**-**	**-**	**-**	**-**	**-**	**-**	PSTA	00H

This command is used to enable panel check, and to disable after reading result.

PSTA: **0: Panel check fail (panel broken)** 1: Panel check pass

(21) CDI (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
VCOM and Data Interval Setting	W	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	50H
	W	1	VBD[1:0]		DDX[1:0]		**-**	CDI[2:0]			D2H

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (10 Hsync).

VBD[1:0]: Border LUT selection

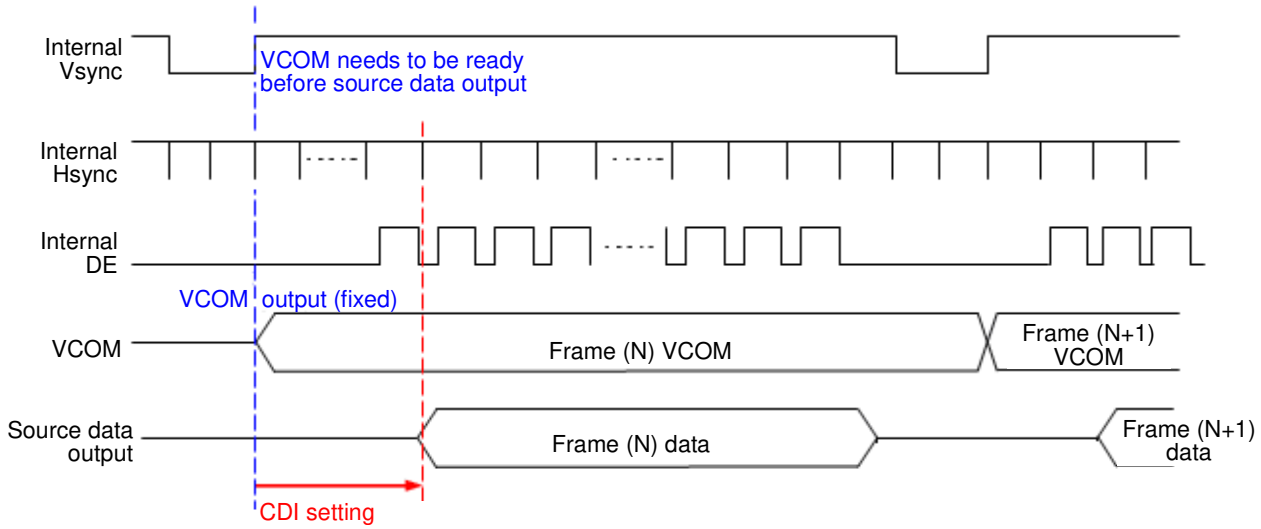
DDX[1:0]: Data polarity

DDX[1:0]	Data {NEW, OLD}	LUT
00	00	LUTW
	01	
	10	LUTB
	11	
01 (default)	00	LUTB
	01	
	10	LUTW
	11	
10	00	GND
	01	LUTW
	10	LUTB
	11	GND
11	00	GND
	01	LUTB
	10	LUTW
	11	GND

DDX[0]	VBD[1:0]	LUT
0	00	VCOM
	01	LUTW
	10	LUTB
	11	Floating
1 (default)	00	Floating
	01	LUTB
	10	LUTW
	11 (default)	VCOM

CDI[2:0]: VCOM to Data Interval. Interval time setting between VCOM and driver data. Default: 5 Hsync.

CDI[2:0]	Interval
000	7 hsync
001	6 hsync
010	5 hsync (default)
011	4 hsync
100	3 hsync
101	2 hsync
110	2 hsync
111	2 hsync



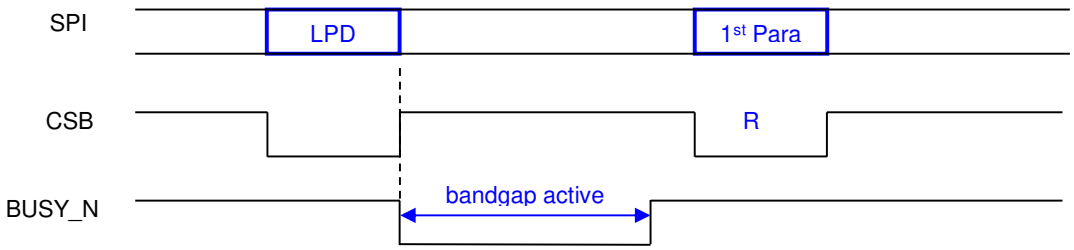
(22) LPD (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Low Power Detect	W	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	51H
	R	1	-	-	-	-	-	-	-	LPD	01H

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal Low Power Detection Flag

0: Low power input (V_{DD}<2.5V, selection by LVD_SEL[1:0] in command LVSEL)
1: Normal status (default)



(23) TCON (R60H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Timing Control	W	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	60H
	W	1	S2G[3:0]				G2S[3:0]				22H

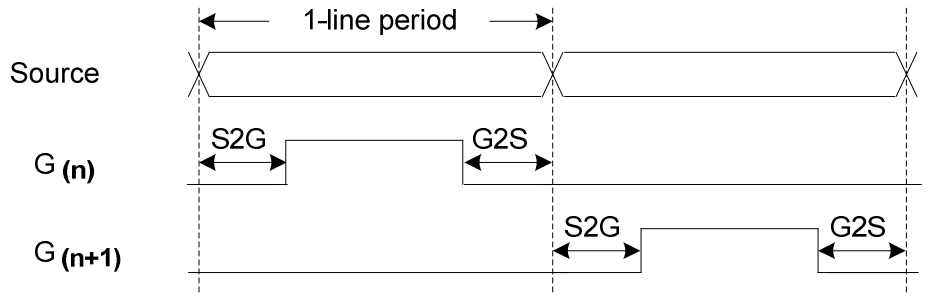
This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000 b	4
0001	8
0010	**12 (Default)**
0011	16
0100	20
0101	24
0110	28
0111	32

S2G[3:0] or G2S[3:0]	Period
1000 b	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	60
1111	64

Unit = 2 uS.



(24) TRES (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Resolution	W	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	61H
	W	1	**-**	HRES[6:3]				**0**	**0**	**0**	00H
	W	1	VRES[7:0]								00H

HRES[6:3]: Horizontal Resolution (HRES[2:0] is forced to '0')

VRES[7:0]: Vertical Resolution

Active channel calculation (assuming HST[6:0]=0, VST[7:0]=0):

Source: First active source = S0

Last active source = HRES[6:3]*8 - 1

Gate: First active gate = G0

Last active gate = VRES[7:0] - 1

Example: For 64(source) x 128(gate), assuming HST[7:0]=0, VST[8:0]=0, then

Source: First active source = S0

Last active source = S63 (Because HRES[6:3]*8 – 1 = 8*8 - 1 = 63)

Gate: First active gate = G0

Last active gate = G127 (Because VRES[7:0] -1 = 128 - 1= 127)

(25) GSST (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Gate / Source Start position	W	0	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**1**	65H
	W	1	**-**	HST[6:3]				**0**	**0**	**0**	00H
	W	1	VST[7:0]								00H

This command defines resolution start gate/source position.

HST[7:3]: Horizontal Display Start Position (Source)

VST[7:0]: Vertical Display Start Position (Gate)

Example: For 64(Source) x 128(Gate), assuming HST[6:3] = 1 and VST[7:0] = 16, then

Source:	First active source = S8	(Because HST[6:0] = HST[6:3]*8 = 1*8 = 8)
	Last active source = S71	(Because HST[6:0] + HRES[8:0] – 1 = 8 + 64 - 1 = 71)
Gate:	First active gate = G16	(Because VST[7:0] = 16)
	Last active gate = G143	(Because VST[7:0] + VRES[7:0] – 1 = 16 + 128 - 1 = 143)

(26) REV (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read IC Revision	W	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	70H
	R	1	LUT_REV0[7:0]								FFH
	R	1	LUT_REV1[7:0]								FFH
	R	1	CHIP_ID[7:0]								0EH

This command reads the version of the IC.

CHIP_REV[7:0]: Chip Revision, fixed at 0x0Eh

(27) FLG (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read Flags	W	0	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	71H
	R	1	CPOK	PTL_flag	**-**	**-**	data_flag	PON	POF	BUSY_N	02H

This command reads the IC status.

CPOK: Charge pump status

PTL_FLAG: Partial display status (high: partial mode)

data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY_N: Driver busy status (low active)

(28) CRC (R72H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Cyclic redundancy check	R	0	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**0**	72H
	R	1	CRC_MSB[7:0]								FFH
	R	1	CRC_LSB[7:0]								FFH

This command reads Cyclic redundancy check (CRC) result.

The calculation only incudes image data (DTM1 & DTM2), and don't containt DTM1(R10h) & DTM2(R13h).

Polynomial = $x^{16} + x^{12} + x^5 + 1$, initial vaulte: 16'hFFFF

The result will be reset after this command.

CRC_MSB[7:0]: Most significant bits of CRC result

CRC_LSB[7:0]: Lease significant bits of CRC result

(29) AMV (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Auto Measure VCOM	W	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	80H
	W	1	**-**	**-**	AMVT[1:0]		XON	AMVS	AMV	AMVE	10H

This command reads the IC status.

AMVT[1:0]: Auto Measure VCOM Time

00b: 3s
10b: 8s
01b: 5s (default)
11b: 10s

XON: All Gate ON of AMV

0: Gate normally scan during Auto Measure VCOM period. (default)
1: All Gate ON during Auto Measure VCOM period.

AMVS: Source output of AMV

0: Source output 0V during Auto Measure VCOM period. (default)
1: Source output VDHR during Auto Measure VCOM period.

AMV: Analog signal

0: Get VCOM value with the VV command (R81h) (default)
1: Get VCOM value in analog signal. (External analog to digital converter)

AMVE: Auto Measure VCOM Enable (/Disable)

0: No effect (default)
1: Trigger auto VCOM sensing.

(30) VV (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
VCOM Value	W	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	81H
	R	1	**-**	**-**	VV[5:0]						00H

This command gets the VCOM value.
VV[5:0]: VCOM Value Output

VV [5:0]	VCOM Voltage (V)	VV [5:0]	VCOM Voltage (V)	VV [5:0]	VCOM Voltage (V)
00 0000b	-0.10	01 0100b	-1.10	10 1000b	-2.10
00 0001b	-0.15	01 0101b	-1.15	10 1001b	-2.15
00 0010b	-0.20	01 0110b	-1.20	10 1010b	-2.20
00 0011b	-0.25	01 0111b	-1.25	10 1011b	-2.25
00 0100b	-0.30	01 1000b	-1.30	10 1100b	-2.30
00 0101b	-0.35	01 1001b	-1.35	10 1101b	-2.35
00 0110b	-0.40	01 1010b	-1.40	10 1110b	-2.40
00 0111b	-0.45	01 1011b	-1.45	10 1111b	-2.45
00 1000b	-0.50	01 1100b	-1.50	11 0000b	-2.50
00 1001b	-0.55	01 1101b	-1.55	11 0001b	-2.55
00 1010b	-0.60	01 1110b	-1.60	11 0010b	-2.60
00 1011b	-0.65	01 1111b	-1.65	11 0011b	-2.65
00 1100b	-0.70	10 0000b	-1.70	11 0100b	-2.70
00 1101b	-0.75	10 0001b	-1.75	11 0101b	-2.75
00 1110b	-0.80	10 0010b	-1.80	11 0110b	-2.80
00 1111b	-0.85	10 0011b	-1.85	11 0111b	-2.85
01 0000b	-0.90	10 0100b	-1.90	11 1000b	-2.90
01 0001b	-0.95	10 0101b	-1.95	11 1001b	-2.95
01 0010b	-1.00	10 0110b	-2.00	11 1010b	-3.00
01 0011b	-1.05	10 0111b	-2.05	11 1011b	-3.05

(31) VDCS (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Vcom DC Setting	W	0	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	82H
	W	1	**-**	**-**	VDCS[5:0]						00H

This command sets VCOM_DC value.
VDCS[5:0]: VCOM_DC Setting

VDCS [5:0]	VCOM Voltage (V)	VDCS [5:0]	VCOM Voltage (V)	VDCS [5:0]	VCOM Voltage (V)
00 0000b	-0.10	01 0100b	-1.10	10 1000b	-2.10
00 0001b	-0.15	01 0101b	-1.15	10 1001b	-2.15
00 0010b	-0.20	01 0110b	-1.20	10 1010b	-2.20
00 0011b	-0.25	01 0111b	-1.25	10 1011b	-2.25
00 0100b	-0.30	01 1000b	-1.30	10 1100b	-2.30
00 0101b	-0.35	01 1001b	-1.35	10 1101b	-2.35
00 0110b	-0.40	01 1010b	-1.40	10 1110b	-2.40
00 0111b	-0.45	01 1011b	-1.45	10 1111b	-2.45
00 1000b	-0.50	01 1100b	-1.50	11 0000b	-2.50
00 1001b	-0.55	01 1101b	-1.55	11 0001b	-2.55
00 1010b	-0.60	01 1110b	-1.60	11 0010b	-2.60
00 1011b	-0.65	01 1111b	-1.65	11 0011b	-2.65
00 1100b	-0.70	10 0000b	-1.70	11 0100b	-2.70
00 1101b	-0.75	10 0001b	-1.75	11 0101b	-2.75
00 1110b	-0.80	10 0010b	-1.80	11 0110b	-2.80
00 1111b	-0.85	10 0011b	-1.85	11 0111b	-2.85
01 0000b	-0.90	10 0100b	-1.90	11 1000b	-2.90
01 0001b	-0.95	10 0101b	-1.95	11 1001b	-2.95
01 0010b	-1.00	10 0110b	-2.00	11 1010b	-3.00
01 0011b	-1.05	10 0111b	-2.05	others	-3.00

(32) PTL (R90H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Partial Window	W	0	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	90H
	W	1	**-**	HRST[6:3]				**0**	**0**	**0**	00H
	W	1	**-**	HRED[6:3]				**1**	**1**	**1**	07H
	W	1	VRST[7:0]								00H
	W	1	VRED[7:0]								00H
	W	1	**-**	**-**	**-**	**-**	**-**	**-**	**-**	PTL_SCAN	01H

This command sets partial window.

HRST[6:3]: Horizontal start channel bank. (value 0h~9h)

HRED[6:3]: Horizontal end channel bank. (value 0h~9h). HRED must be greater than HRST.

VRST[7:0]: Vertical start line. (value 00h~9Fh)

VRED[7:0]: Vertical end line. (value 00h~9Fh). VRED must be greater than VRST.

PTL_SCAN: 0: Gates scan only inside of the partial window.
1: Gates scan both inside and outside of the partial window. (default)

(33) PIN (R91H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial In	W	0	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**1**	91H

This command makes the display enter partial mode.

(34) POUT (R92H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial Out	W	0	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	92H

This command makes the display exit partial mode and enter normal mode.

(35) PROGRAM MODE (PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enter Program Mode	W	0	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	A0H
	W	1	**0**	**0**	**0**	**0**	**0**	RGSET[2:0]			04H

After this command is issued, the chip would enter the program mode.

After the programming procedure completed, a hardware reset is necessary for leaving program mode.

RGSET[2:0]: OTP program/read address range selection.

RGSET[2:0]	OTP Program / Read Range
010	0x000 ~ 0x3FF
011	0x400 ~ 0x7FF
100 (default)	Reserved
101	Reserved
others	0x000 ~ 0x7FF

(36) ACTIVE PROGRAM (APG) (RA1H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Active Program OTP	W	0	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	A1H

After this command is transmitted, the programming state machine would be activated.

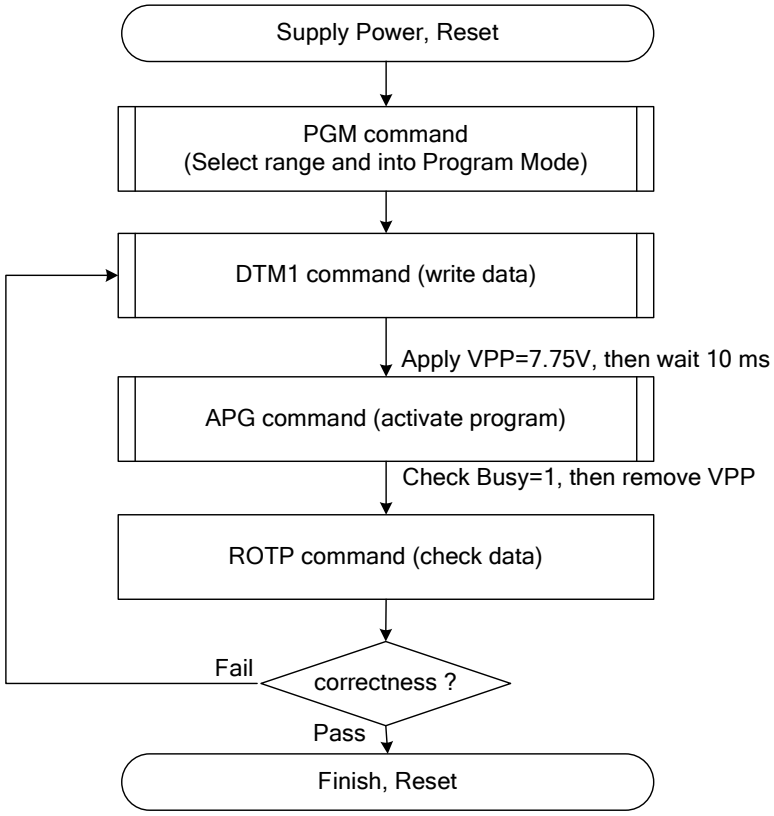
The BUSY_N flag would fall to 0 until the programming is completed.

(37) READ OTP DATA (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read OTP data for check	W	0	**1**	**0**	**1**	**0**	**0**	**0**	**1**	**0**	A2h
	R	1	Dummy								--
	R	1	The data of address 0x000 in the OTP								--
	R	1	The data of address 0x001 in the OTP								--
	R	1	:								--
	R	1	The data of address (n-1) in the OTP								--
	R	1	The data of address (n) in the OTP								--

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0x7FF.



The sequence of programming OTP.

(38) CASCADE SETTING (CCSET) (RE0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Cascade Option	W	0	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	E0h
	W	1	-	-	-	-	-	-	TSFIX	CCEN	00h

This command is used for cascade.

CCEN: Output clock enable/disable.

0: Output 0V at CL pin. (default)
1: Output clock at CL pin for slave chip.

TSFIX: Let the value of slave's temperature is same as the master's.

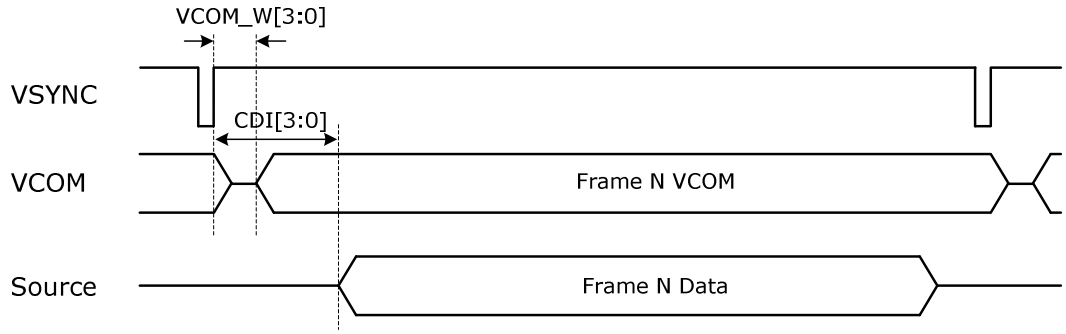
0: Temperature value is defined by internal temperature sensor / external LM75. (default)
1: Temperature value is defined by TS_SET[7:0] registers.

(39) POWER SAVING (PWS) (RE3H)

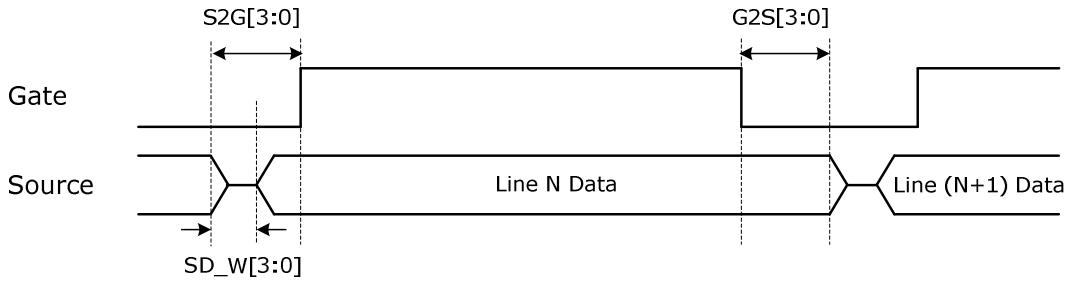
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Power Saving for VCOM & Source	W	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	E3h
	W	1	VCOM_W[3:0]				SD_W[3:0]				33h

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 2 uS)



(40) LPD VOLTAGE SELECT (LVSEL)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Select LPD Voltage	W	0	**1**	**1**	**1**	**0**	**0**	**1**	**0**	**1**	E4h
	W	1	**-**	**-**	**-**	**-**	**-**	**-**	LVD_SEL[1:0]		03h

LVD_SEL[1:0]: Low Power Voltage selection

LVD_SEL[1:0]	LPD voltage threshold
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11	< 2.5 V **(Default)**

(41) FORCE TEMPERATURE (TSSET) (RE5H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Force Temperature Value for Cascade	W	0	**1**	**1**	**1**	**0**	**0**	**1**	**0**	**1**	E5h
	W	1	TS_SET[7:0]								00h

This command is used for cascade to fix the temperature value of master and slave chip.

HOST INTERFACES

UC8175 provides 3-wire/4-wire serial interface for command and display data transferred from the MCU. The serial interface supports 8-bit mode. Data can be input/output by clocks while the chip is active (CSB =LOW). While input, data are written in order from MSB at the clock rising edge. When too many parameters are input, the chip accepts only defined parameters, and ignores undefined ones.

BS	Interface	CSB	DC	SCL	SDA
High	3-wire SPI	Available	Fix to GND	Available	Available
Low	4-wire SPI	Available	Available	Available	Available

3-wire SPI format

Data / Command is recognized with the first bit transferred. Data are transferred in the unit of 9 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 9 bits. (The serial counter is reset at the rising edge of the CSB signal.)

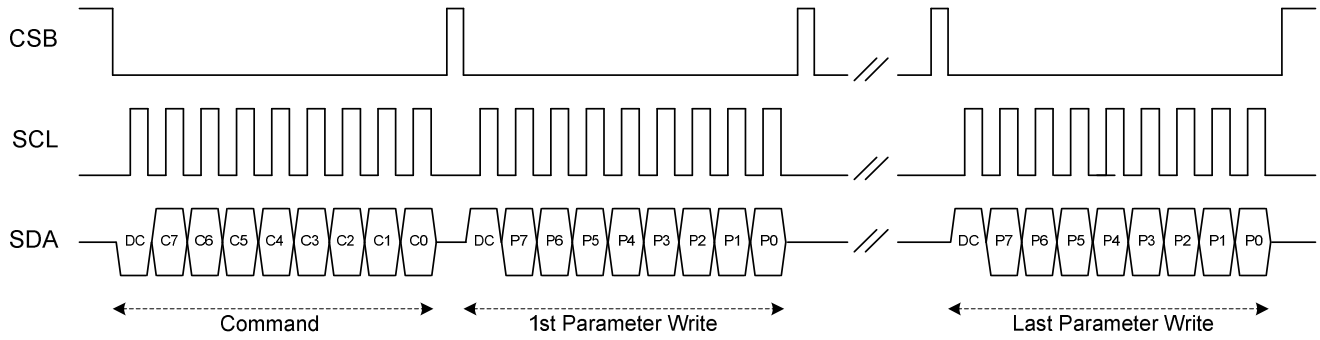


Figure: 3-wire SPI write operation

The MSB bit of data will be output at SDA pin after the 1st SCL falling edge, if the 1st input data at SDA is high. Only in the case of OTP data read, the 1st packet of output data are dummy data.

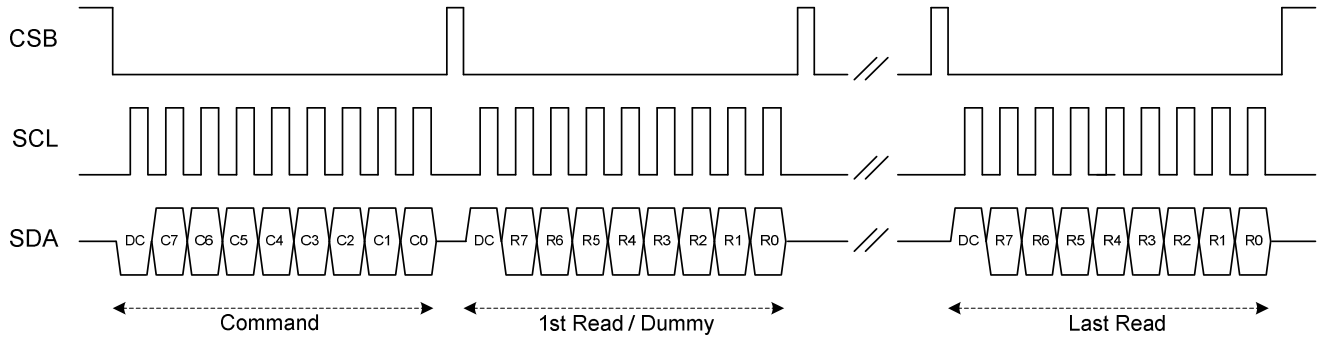


Figure: 3-wire SPI read operation

4 wire SPI format

Data / Command is recognized with DC pin. Data are transferred in the unit of 8 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 8 bits. (The serial counter is reset at the rising edge of the CSB signal.)

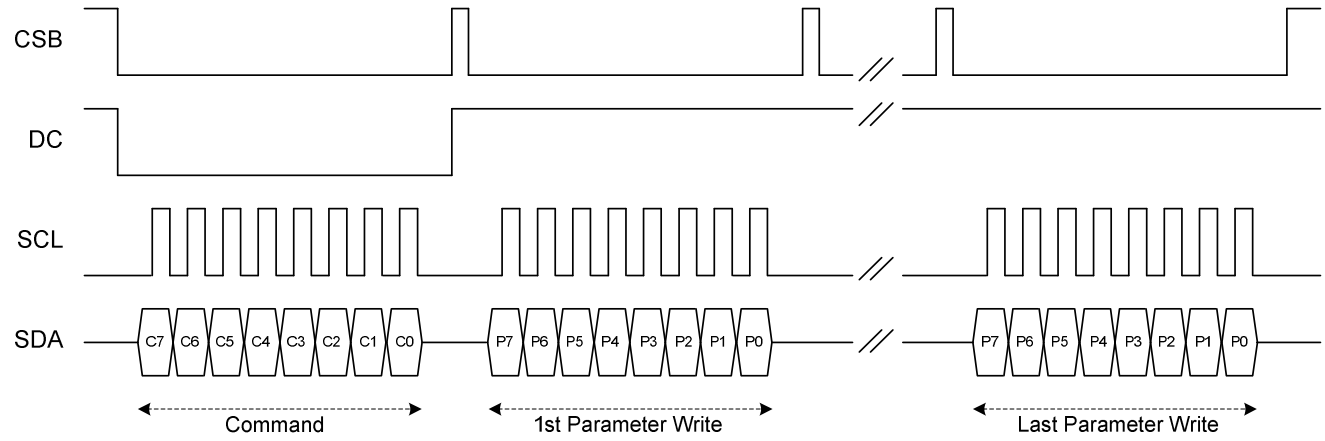


Figure: 4-wire SPI write operation

The MSB bit of data will be output at SDA pin after the CSB falling edge, if DC pin is High. Only in the case of OTP data read, the 1st packet of output data are dummy data.

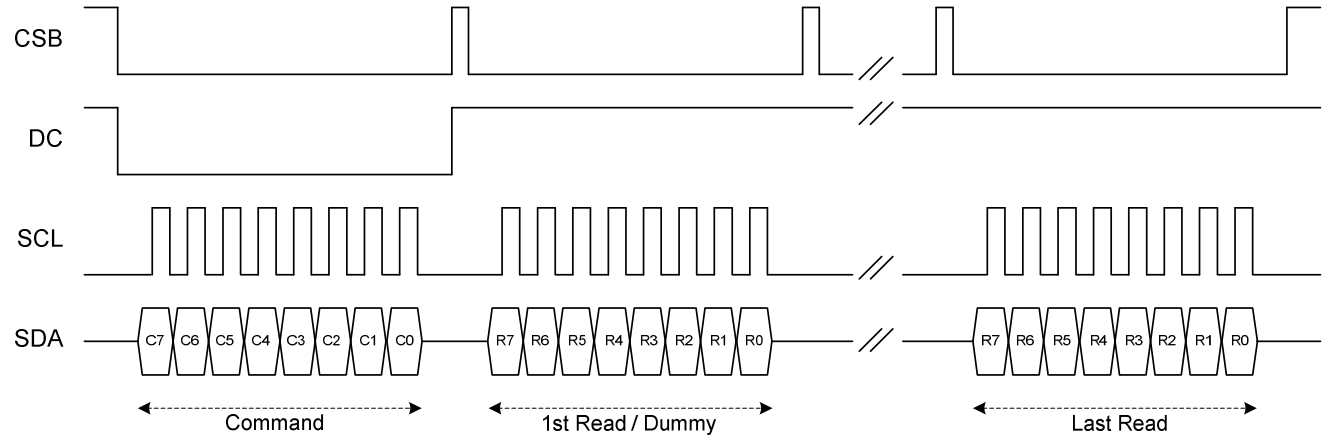
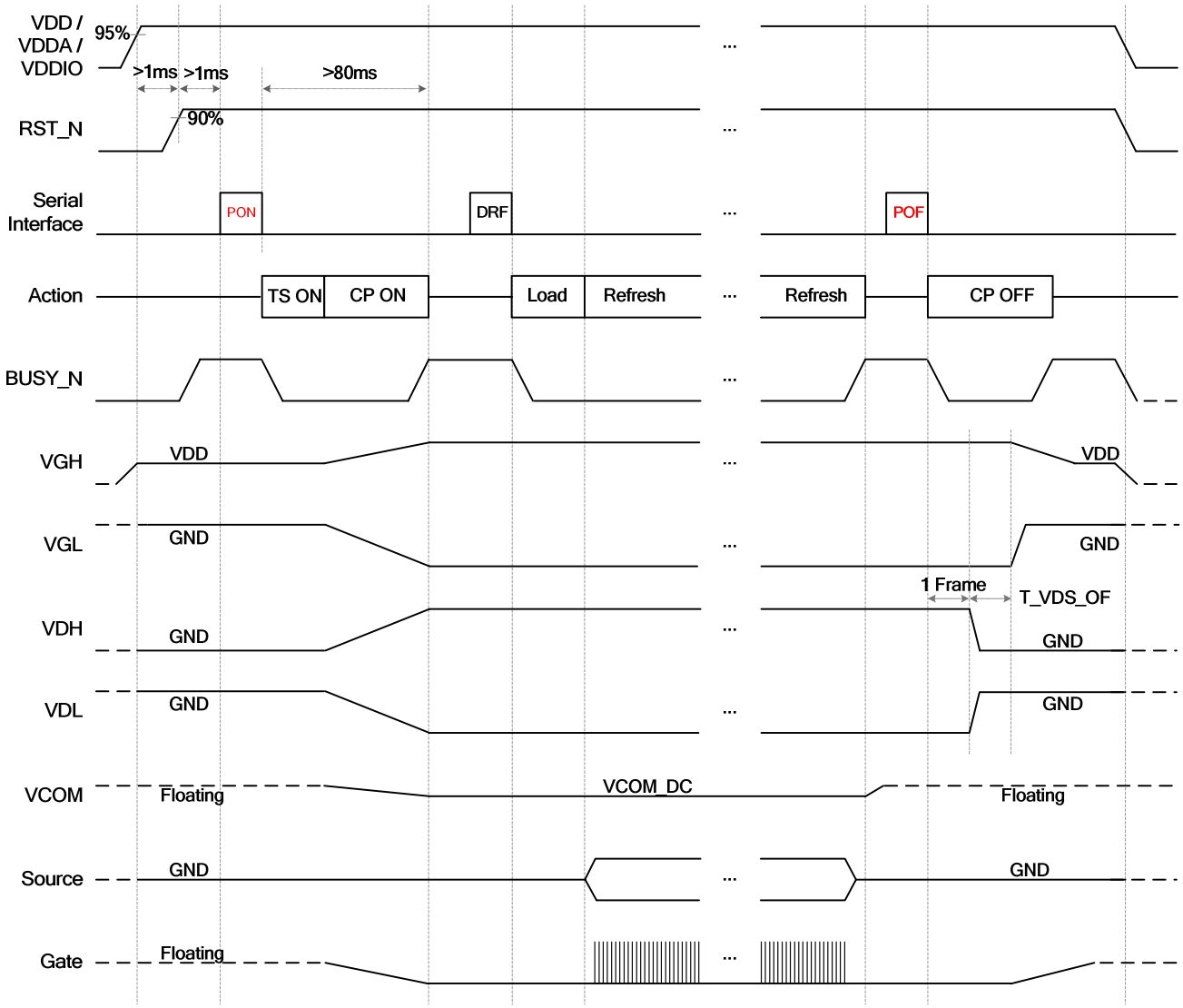


Figure: 4-wire SPI read operation

POWER MANAGEMENT

Power ON/OFF Sequence

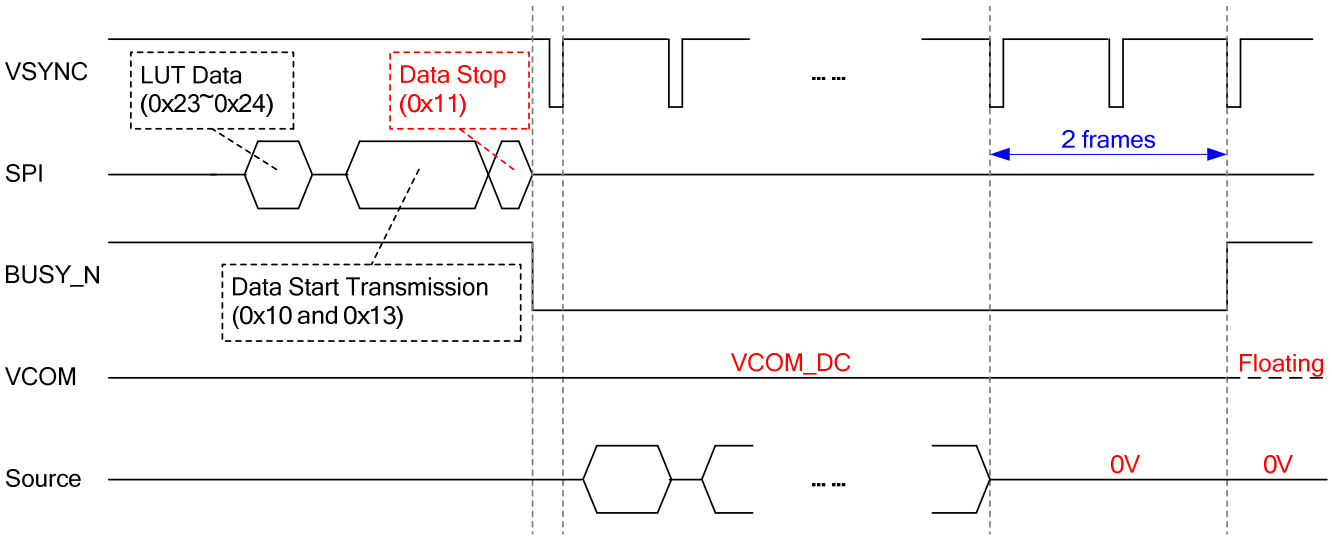
1. Temperature sensor will be activated automatically for one-time sensing before enabling booster.
2. After refreshing display, VCOM will be set to floating automatically.
3. After RST_N rising, the waiting time for internal initial processing, greater than 1mS, is necessary. Any commands transmitted to chip during this time will be ignored.



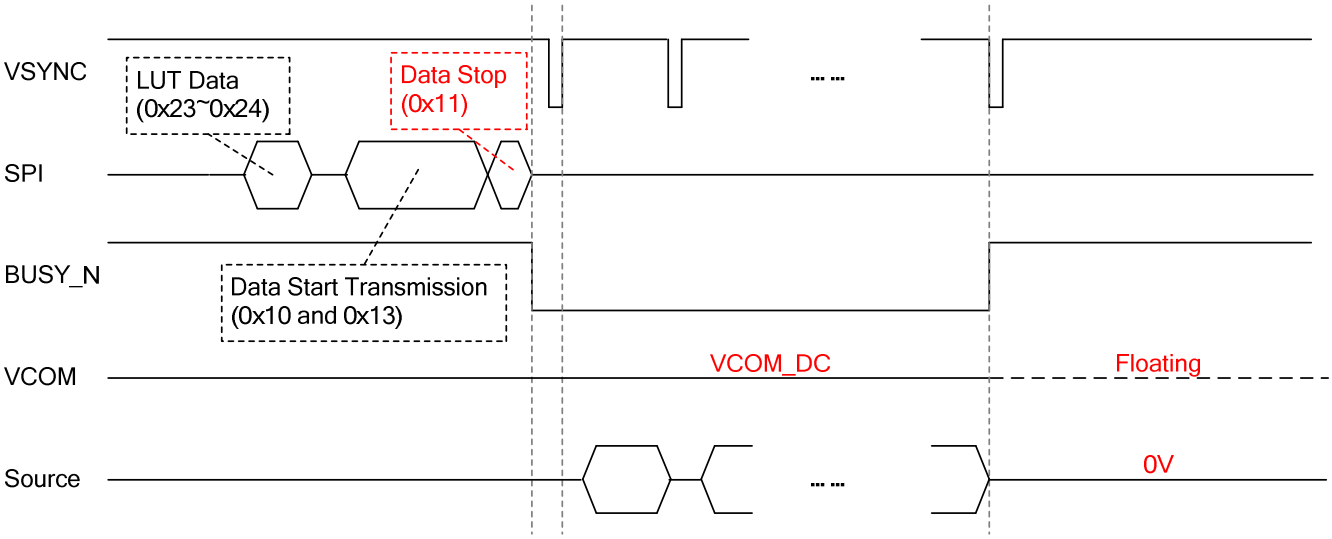
Data Transmission Waveform

Example 1: After 3 cases, the driver will send 2 frame VCOM and data to 0 V.

1. All 7 LUT stages complete.
2. meet the stage whose Times to Repeat =0
3. meet the stage whose all Number of Frames =0



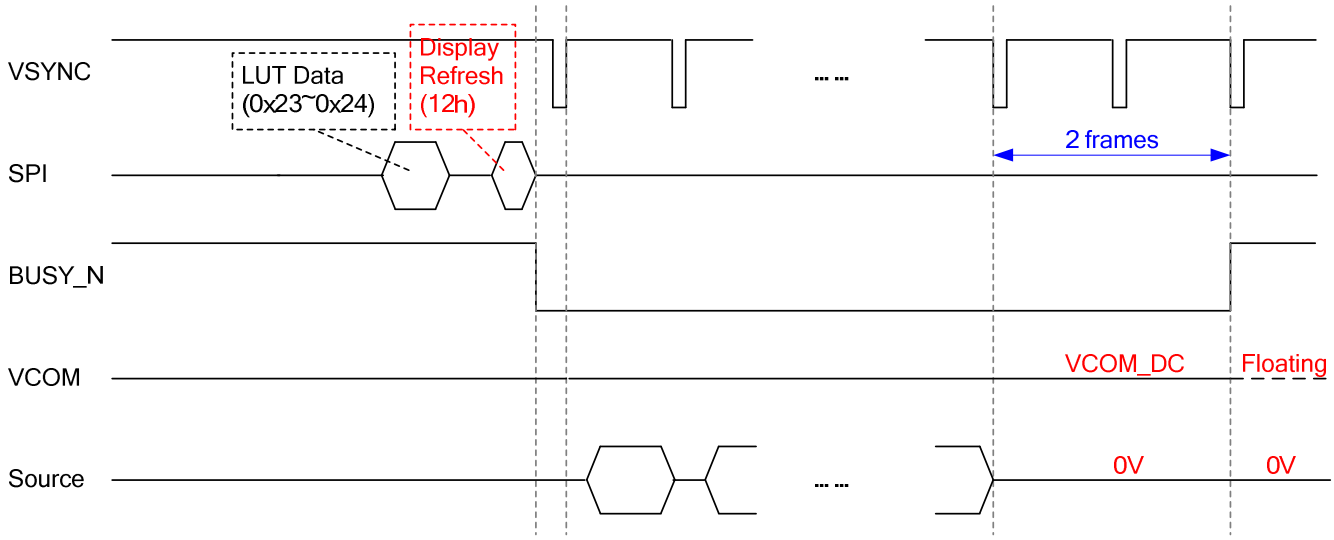
Example2: While level selection in LUT is “1111_1111b”, the driver will stop immediately.



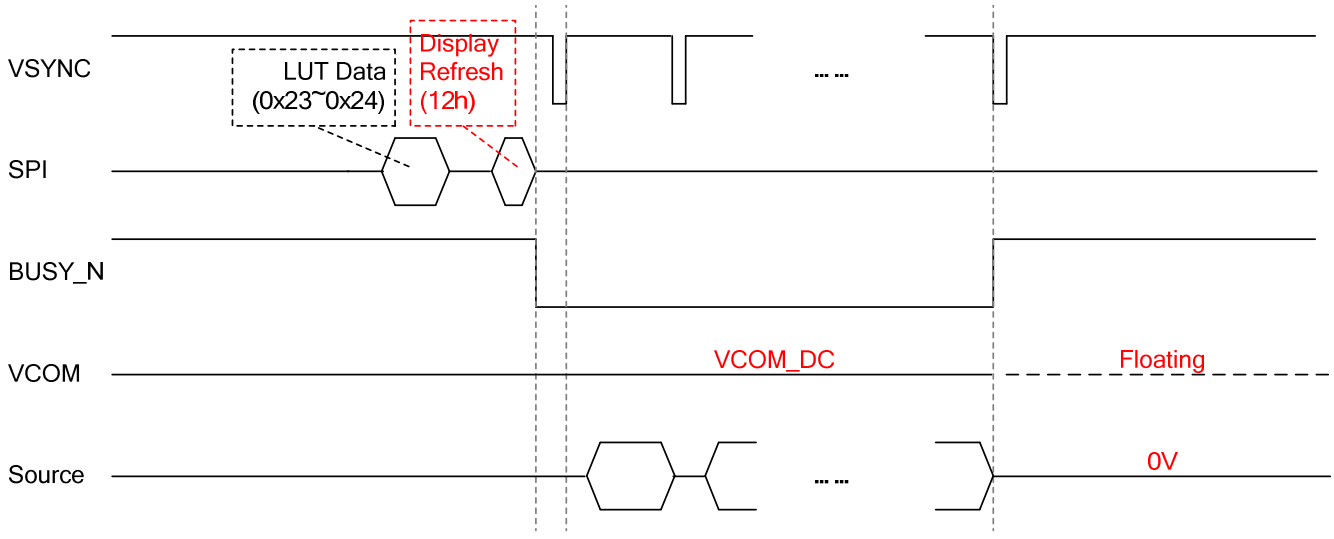
Display Refresh Waveform

Example 1: After three cases, the driver will send 2 frames VCOM and data to 0 V.

1. All 7 LUT stages complete.
2. meet the stage whose Times to Repeat = 0
3. meet the stage whose all Number of Frames = 0



Example2: While level selection in LUT is “1111_1111b”, the driver will stop immediately.



BUSY_N Signal

Commands, except reading command, are restricted by refreshing display (DRF / DSP) as listed in the table below.

BUSY_N is used to represent the status of internal action. Commands activating internal operation or calculation will cause BUSY_N falling to LOW. After actions completed, BUSY_N will return to HIGH.

Command	Refresh Restriction	BUSY_N flag
PSR	X	No action
PWR	X	No action
POF	X	Flag
PFS	X	No action
PON	X	Flag
PMES	X	Flag
CPSET	X	No action
DSLP	X	Flag
AUTO	X	Flag
DTM1	X	No action
DSP	X	Flag
DRF	X	Flag
DTM2	X	No action
LUTW	X	No action
LUTB	X	No action
LUTOPT	X	No action
PLL	X	No action
TSC	X	Flag
TSE	X	No action
PBC	X	No action
CDI	X	No action
LPD	X	Flag
TCON	X	No action
TRES	X	No action
GSST	X	No action
REV	V	No action
FLG	V	No action
AMV	X	Flag
VV	V	No action
VDCS	X	No action
PTL	X	No action
PTIN	X	No action
PTOUT	X	No action
PGM	X	No action
APG	X	Flag
ROTP	X	No action
CCSET	X	No action
PWS	X	No action
LVSEL	X	No action
TSSET	X	No action

V: Accepted, X: Ignored

OTP ADDRESS MAPPING

The size of the internal One Time Programmable (OTP) memory is 2K bytes, and the address is from 0x000 to 0x7FF. The unprogrammed bit is logic 1. Only the bit at logic 1 can be programmed to logic 0, but the bit at logic 0 can *NOT* be converted to logic 1.

There are 2 areas (0x3F0~0x3FF, 0x7F0~0x7FF) are reserved for UltraChip only. Write all 0xFF of data to skip the 2 areas. The recommended voltage of VPP during programming is 7.75V. In the other condition except for programming, let VPP floating or be connected to GND. The maximum current of VPP during programming is 5mA.

There are 2 banks in the internal OTP, and each bank has 1K bytes storage memory. The formats of each bank are the same, and the selection of bank is controlled by Check Code (0x000 and 0x400). The 2 banks are used for two times programming.

Table 1: OTP Address Map

Bank0		Bank1	
Address	Content	Address	Content
0x000	Check Code (0xA5)	0x400	Check Code (0xA5)
0x001	LUT Version 0	0x401	LUT Version 0
0x002	LUT Version 1	0x402	LUT Version 1
0x003	Temperature Boundary 0 (TB0)	0x403	Temperature Boundary 0 (TB0)
0x004	Temperature Boundary 1 (TB1)	0x404	Temperature Boundary 1 (TB1)
0x005	Temperature Boundary 2 (TB2)	0x405	Temperature Boundary 2 (TB2)
0x006	Temperature Boundary 3 (TB3)	0x406	Temperature Boundary 3 (TB3)
0x007	Temperature Boundary 4 (TB4)	0x407	Temperature Boundary 4 (TB4)
0x008	Temperature Boundary 5 (TB5)	0x408	Temperature Boundary 5 (TB5)
0x009	Temperature Boundary 6 (TB6)	0x409	Temperature Boundary 6 (TB6)
0x00A	Temperature Boundary 7 (TB7)	0x40A	Temperature Boundary 7 (TB7)
0x00B	Temperature Boundary 8 (TB8)	0x40B	Temperature Boundary 8 (TB8)
0x00C ~ 0x010	Reserved	0x40C ~ 0x410	Reserved
0x011 ~ 0x01F	Command Default Setting *(1)	0x411 ~ 0x41F	Command Default Setting *(1)
0x020 ~ 0x02F	User Define Space	0x420 ~ 0x42F	User Define Space
0x030 ~ 0x08F	TR0 *(2)	0x430 ~ 0x48F	TR0 *(2)
0x090 ~ 0x0EF	TR1 *(2)	0x490 ~ 0x4EF	TR1 *(2)
0x0F0 ~ 0x14F	TR2 *(2)	0x4F0 ~ 0x54F	TR2 *(2)
0x150 ~ 0x1AF	TR3 *(2)	0x550 ~ 0x5AF	TR3 *(2)
0x1B0 ~ 0x20F	TR4 *(2)	0x5B0 ~ 0x60F	TR4 *(2)
0x210 ~ 0x26F	TR5 *(2)	0x610 ~ 0x66F	TR5 *(2)
0x270 ~ 0x2CF	TR6 *(2)	0x670 ~ 0x6CF	TR6 *(2)
0x2D0 ~ 0x32F	TR7 *(2)	0x6D0 ~ 0x72F	TR7 *(2)
0x330 ~ 0x38F	TR8 *(2)	0x730 ~ 0x78F	TR8 *(2)
0x390 ~ 0x3EF	TR9 *(2)	0x790 ~ 0x7EF	TR9 *(2)
0x3F0 ~ 0x3FF	Reserved	0x7F0 ~ 0x7FF	Reserved

Note:

(1) See section "COMMAND DEFAULT SETTING" for more detail.

(2) See section "LUT FORMAT IN OTP" for more detail.

TEMPERATURE RANGE

The temperature selection mechanism consists of a less-than-or-equal-to operator and 9 temperature boundary settings (TBx) to determine 10 temperature ranges. The sequence of mechanism is from TB0 to TB8, as shown below. If less than 10 tempeature ranges are used, the last TBx must be set to 0x7F to end the mechanism.

Procedure Order	Comparison Condition	Action & Segment Selection
1-0. Read 0x400	Content = 0xA5 ?	Yes: Jump to Procedure 2 (Bank1), No: Jump to Procedure 1-1
1-1, Read 0x000	Content = 0xA5 ?	Yes: Jump to Procedure 2 (Bank0), No: Stop Refresh
2. Read 0x003 / 0x403	Real Temperature ≦ TB0	Use TR0's table & setting, exit
3. Read 0x004 / 0x404	Real Temperature ≦ TB1	Use TR1's table & setting, exit
4. Read 0x005 / 0x405	Real Temperature ≦ TB2	Use TR2's table & setting, exit
5. Read 0x006 / 0x406	Real Temperature ≦ TB3	Use TR3's table & setting, exit
6. Read 0x007 / 0x407	Real Temperature ≦ TB4	Use TR4's table & setting, exit
7. Read 0x008 / 0x408	Real Temperature ≦ TB5	Use TR5's table & setting, exit
8. Read 0x009 / 0x409	Real Temperature ≦ TB6	Use TR6's table & setting, exit
9. Read 0x00A / 0x40A	Real Temperature ≦ TB7	Use TR7's table & setting, exit
10. Read 0x00B / 0x40B	Real Temperature ≦ TB8	Use TR8's table & setting, exit
11. Other	Real Temperature > TB8	Use TR9's table & setting, finish

Note: TRx's content is defined in "LUT FORMAT IN OTP" section.

Example:

If temperature = -20 ºC, TR0 is selected.

If temperature = -10 ºC, TR1 is selected.

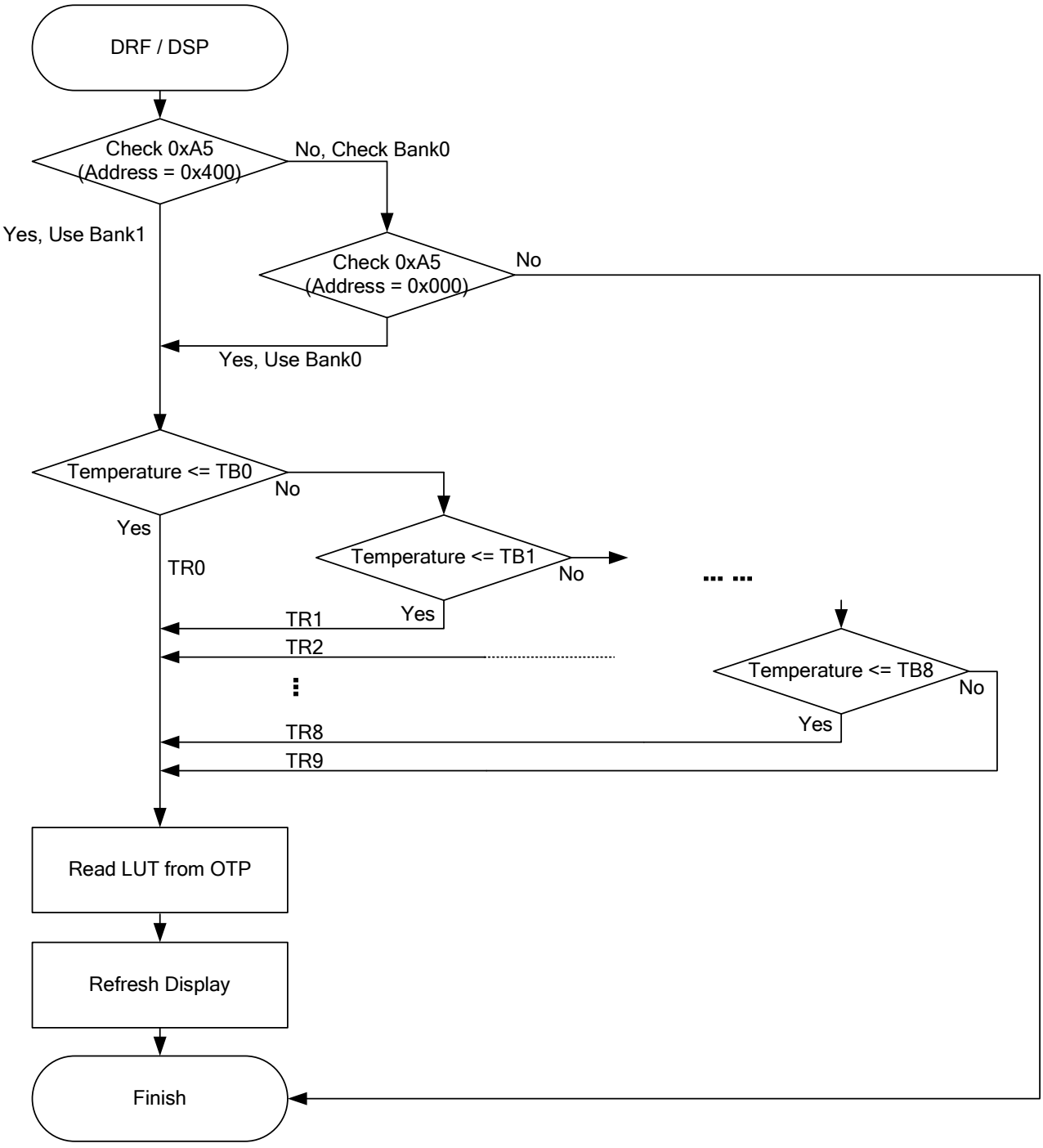
If temperature = 0 ºC, TR2 is selected.

If temperature = 20 ºC, TR4 is selected.

If temperature = 40 ºC, TR5 is selected.

If temperature > 40 ºC, TR5 is selected.

OTP Address	Content	
003h	0xF1	(-15 ºC)
004h	0xFB	(-5 ºC)
005h	0x00	(0 ºC)
006h	0x0A	(10 ºC)
007h	0x1E	(30 ºC)
008h	0x7F	-



Temperature Selection Mechanism

COMMAND DEFAULT SETTING

This function can modify the default value of command registers by the OTP content between address 0x011~0x01F (or 0x411~0x41F). The data of address 0x011 (or 0x411) is the enable key of the function. Changing default value function is used to reduce the initial code length executed by the microcontroller.

Address	D7	D6	D5	D4	D3	D2	D1	D0	Command	Registers	Original
0x011 / 0x411	#	#	#	#	#	#	#	#	Check Code	0xA5 (Enable Key)	--
0x012 / 0x412	#	#	#	--	#	#	--	--	PSR	RES[1:0], REG, UD, SHL	0x0F
0x013 / 0x413	--	--	#	#	--	--	--	--	PFS	T_VDS_OF[1:0]	0x00
0x014 / 0x414	--	--	#	#	#	#	#	#	CPSET	CPINT[1:0], CPS[1:0], CPFRQ[1:0]	0x3F
0x015 / 0x415	--	--	--	--	#	#	#	#	TSE	TO[3:0]	0x00
0x016 / 0x416	#	#	#	#	--	#	#	#	CDI	VBD[1:0], DDX[1:0], CDI[2:0]	0xD2
0x017 / 0x417	#	#	#	#	#	#	#	#	TCON	S2G[3:0], G2S[3:0]	0x22
0x018 / 0x418	--	#	#	#	#	0	0	0	TRES	HRES[6:3]	0x00
0x019 / 0x419	#	#	#	#	#	#	#	#		VRES[7:0]	0x00
0x01A / 0x41A	--	#	#	#	#	0	0	0	GSST	HST[6:3]	0x00
0x01B / 0x41B	#	#	#	#	#	#	#	#		VST[7:0]	0x00
0x01C / 0x41C	--	--	--	--	--	--	#	#	CCSET	TSFIX ,CCEN	0x00
0x01D / 0x41D	#	#	#	#	#	#	#	#	PWS	BD_W[3:0], SD_W[3:0]	0x33
0x01E / 0x41E	--	--	--	--	--	--	#	#	LVSEL	LVD_SEL[1:0]	0x03
0x01F / 0x41F	#	#	#	#	#	#	#	#	TSSET	TS_SET[7:0]	0x00

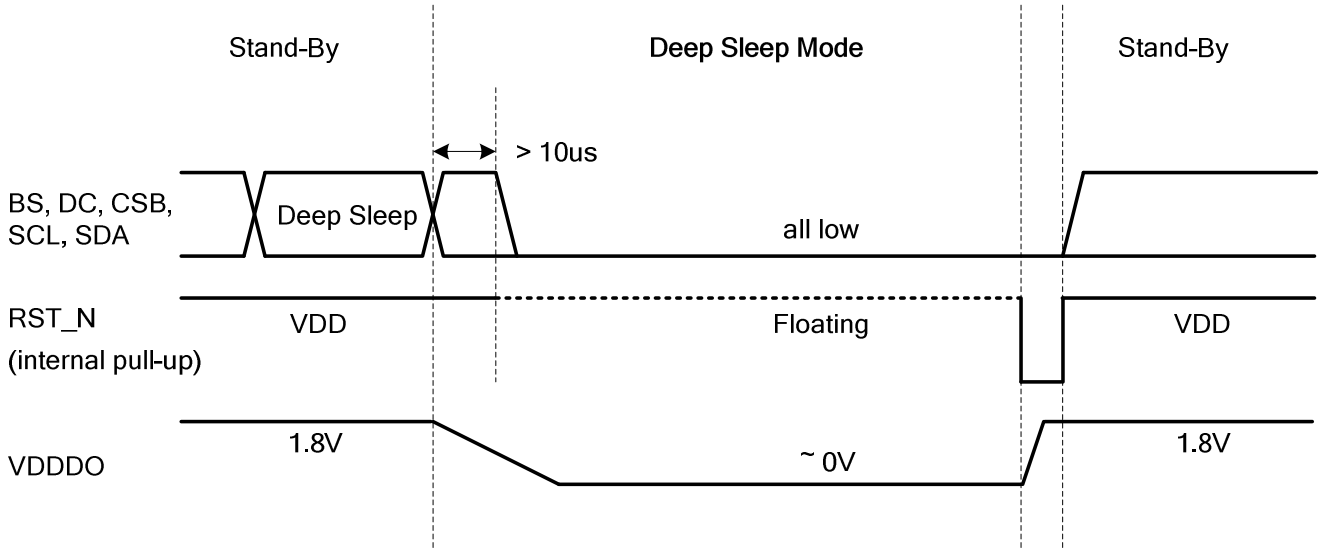
LUT FORMAT IN OTP

There are 10 TRs (temperature range) in each bank. Each TR has independant frame rate, voltage, EOPT/XON settings, LUTs and 6-byte reserved space. There are 7 stages in LUTW/LUTB, and each stage has 6-byte data. The settings will be loaded to register before display refreshing.

	Address	Content
TR0	0x030	PLL Control [5:0]
	0x031	VG Voltage [2:0]
	0x032	VDH Voltage [5:0]
	0x033	VDL Voltage [5:0]
	0x034	VCOM_DC Voltage [7:0]
	0x035	EOPT, XON [6:0]
	0x036~0x05F	LUTW (7 stages)
	0x060~0x089	LUTB (7 stages)
	0x08A~0x08F	Reserved

DEEP SLEEP MODE

After deep sleep command (R07H) is transmitted, UC8175 enters “Deep Sleep Mode”, and leaves by RST_N falling. In “Deep Sleep Mode”, the control signals are recommended tied to 0v to avoid IO leakage current. And the die must be keep away from light which causes photoelectric effect to make internal nodes unstable.



PANEL BREAK CHECK

The panel break check (PBC) function is accomplished by testing the connection of the ITO along panel edge. If the panel is broken, the loop ITO may be cut off. The connection check is judged by signal transmission from CHKGO to CHKGI.

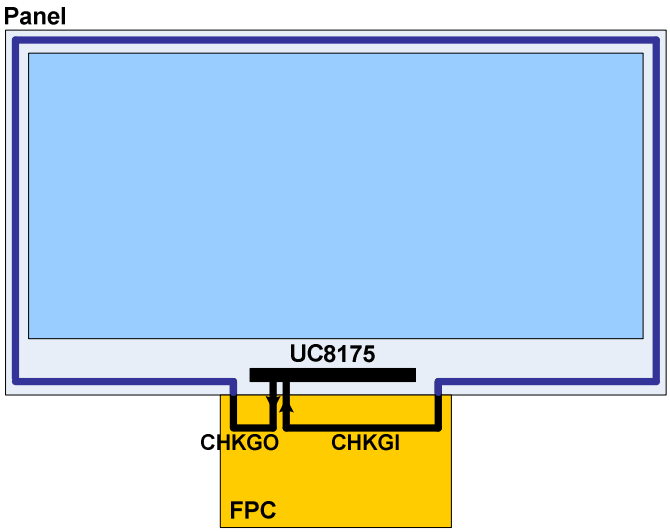


Figure: Panel break check layout example

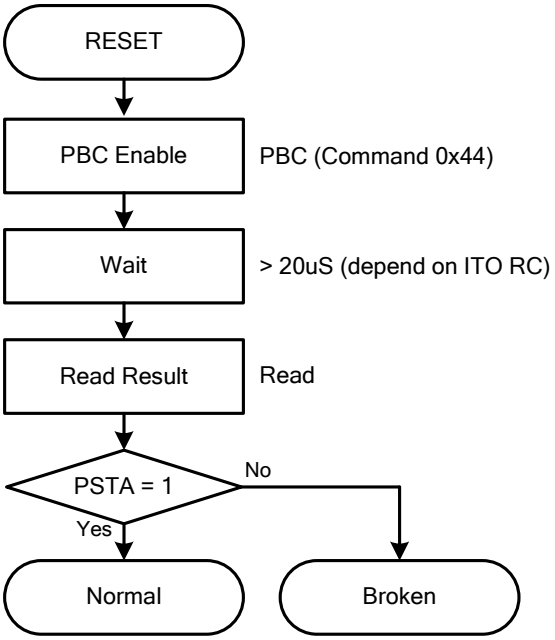
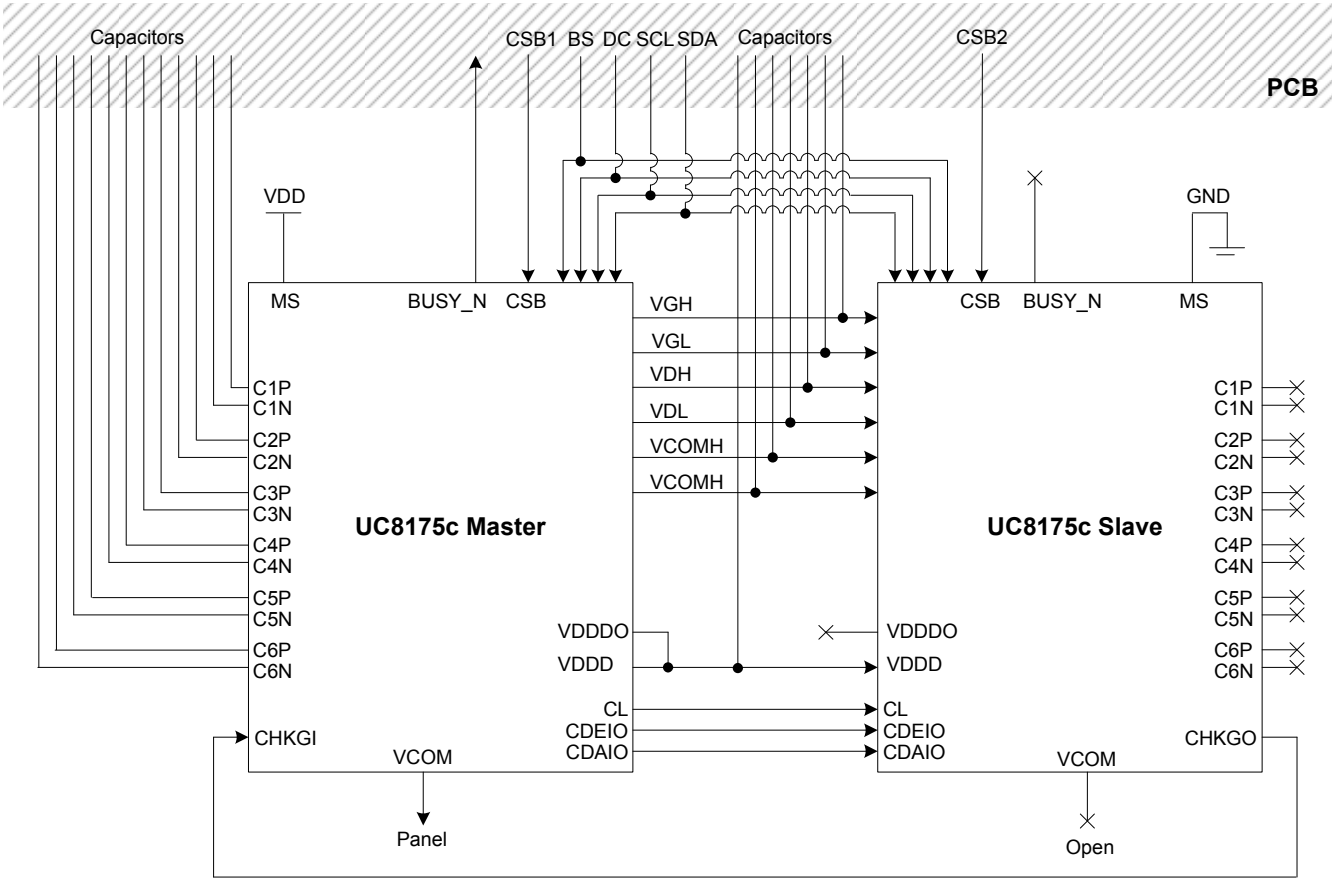


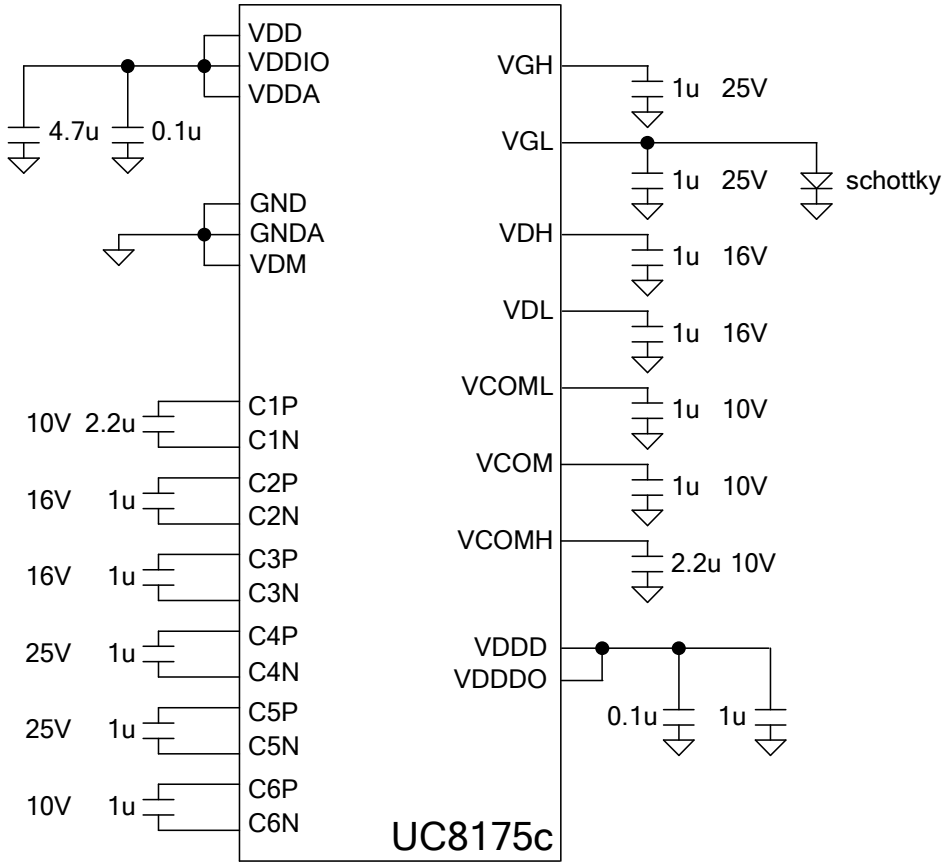
Figure: Panel Break Check (PBC) Sequence

CASCADE APPLICATION CIRCUIT



All commands sent to **Master** must be also sent to **Slave** except for data writing (DTM1 and DTM2). The display data must be separated to two parts, one is for **Master** and another is for **Slave**. They are transmitted to **Master** and **Slave** individually by using CSB1 and CSB2.

APPLICATION CIRCUIT



Recommended Device

1. Schottky Diode: Diodes SD101CWS

Recommended Resister

Item	Pins	Resistance
Power-0	VDD, GND	< 5 Ω
Power-1	VDDA, VDDIO, GNDA, VDM	< 10 Ω
Charge Pump-0	C1P, C1N	< 5 Ω
Charge Pump-1	CxP, CxN (x=2~6), VGH, VGL, VCOMH, VCOML	< 10 Ω
Regulators	VDH, VDL, VCOM, VDDD, VDDDO	< 10 Ω
Logics	MS, BS, CSB, SCL, SDA, etc.	< 50 Ω
OTP	VPP	< 20 Ω

ABSOLUTE MAXIMUM RATINGS

Signal	Item	Min	Max.	Unit
VDD, VDDIO, VDDA	Logic Supply voltage	-0.3	+6.0	V
VPP	OTP programming voltage	-0.3	+8.0	V
VI	Digital input range	-0.3	VDDIO+0.3	V
VGH-VGL	Supply range	-	+32.0	V
Source				
VDH	Analog supply voltage – positive	+11		V
VDL	Analog supply voltage -- negative	-11		V
Gate				
VGH	Analog supply voltage – positive	-0.3	+16	V
VGL	Analog supply voltage -- negative	-16	0.3	V
TSTG	Storage temperature range	-55	+125	°C

Warning:

If ICs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
VDDIO	IO supply voltage		2.3	3.3	3.6	V
VDD	Supply voltage		2.3	3.3	3.6	V
VDDA	DCDC driver supply voltage		2.3	3.3	3.6	V
VIL	LOW Level input voltage	Digital input pins	0	--	0.3xVDD	V
VIH	HIGH Level input voltage	Digital input pins	0.7xVDDIO	--	VDDIO	V
VOH	HIGH Level output voltage	Digital input pins, IOH=400uA	VDDIO-0.4	--	--	V
VOL	LOW Level Output voltage	Digital input pins, IOL=-400uA	0	--	0.4	V
IIN	Input leakage current	Digital input pins except pull-up, pull-down pin	-1	--	1	uA
RIN	Pull-up/down impedance			200		KΩ
Top	Operating temperature		-30		85	°C
dVGH	VGH Supply voltage dev		-500	0	+500	mV
VGH-VGL	Voltage Range of VGH - VGL		--		32	V
dVDH	Supply voltage dev		-300	0	+300	mV
dVDL	Supply voltage dev		-300	0	+300	mV
dVCOM	Supply voltage dev		-200	0	+200	mV
RON	Driver Output Resistance	For source driver, TOP=25°C, VOUT = ±11V		28.5	57.0	KΩ
		For gate driver, TOP=25°C, VOUT = ±16V		5.2	10.4	

VDD=VDDA=VDDIO=3.0V, TOP=25.0 °C

Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
IVDD	DCDC deep sleep current	VDDD OFF	--	0.3	0.5	uA
	DCDC stand-by current	All stopped	--	8.2	10.0	uA
	DCDC operating current	Source output VDH/VDL, Duty = 0.5, Period = 222uS, VCOM DC, No load	--	--	1.5	mA
		Source output VDH/VDL, Duty = 0.5, Period = 222uS, VCOM DC, External cap: 8.11pF, NMOS = 9.67pF	--	--	3.0	
IVDDIO	IO deep sleep current	VDDD OFF	--	0.1	0.3	uA
	IO stand-by current	Charge Pump OFF	--	0.5	4.0	uA
	IO operating current	No load	--	--	0.1	mA
IVDDA	Analog deep sleep current	VDDD OFF	--	0.1	0.3	uA
	Analog stand-by current	Charge Pump OFF	--	15.5	20.0	uA
	Analog operating current		--	--	0.2	mA

AC CHARACTERISTICS

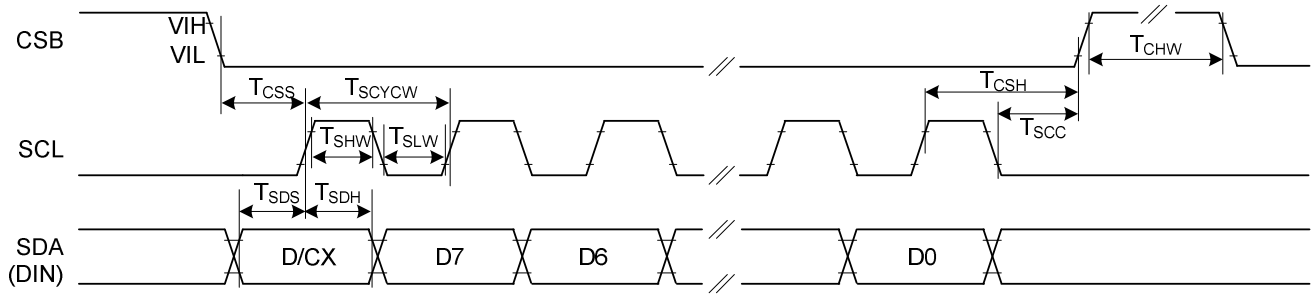


Figure: 3-wire Serial Interface Characteristics (Write mode)

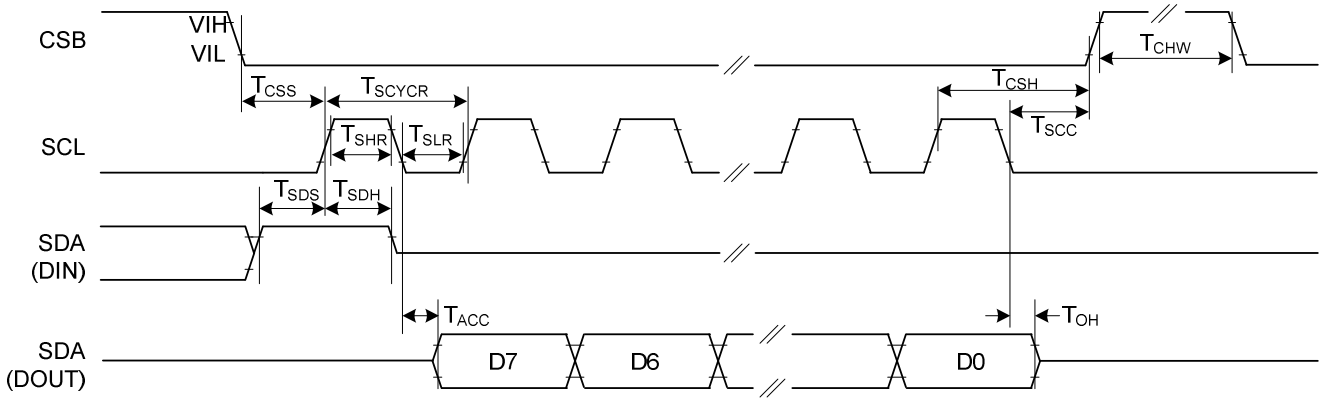


Figure: 3-wire Serial Interface Characteristics (Read mode)

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL “H” pulse width (Write)	35			ns
T_{SLW}		SCL “L” pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	200			ns
T_{SHR}		SCL “H” pulse width (Read)	60			ns
T_{SLR}		SCL “L” pulse width (Read)	60			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			200	ns
T_{OH}		Output disable time	15			ns

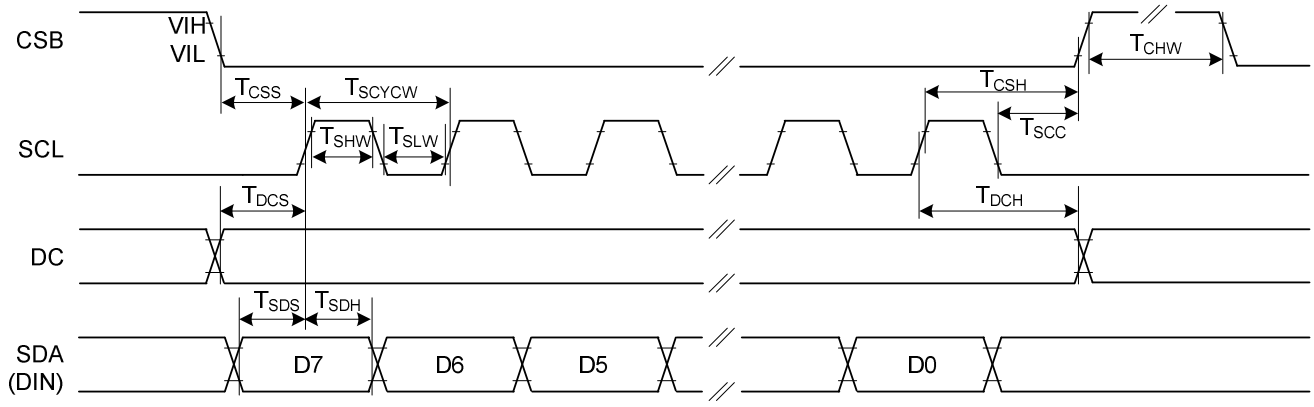


Figure: 4-wire Serial Interface Characteristics (Write mode)

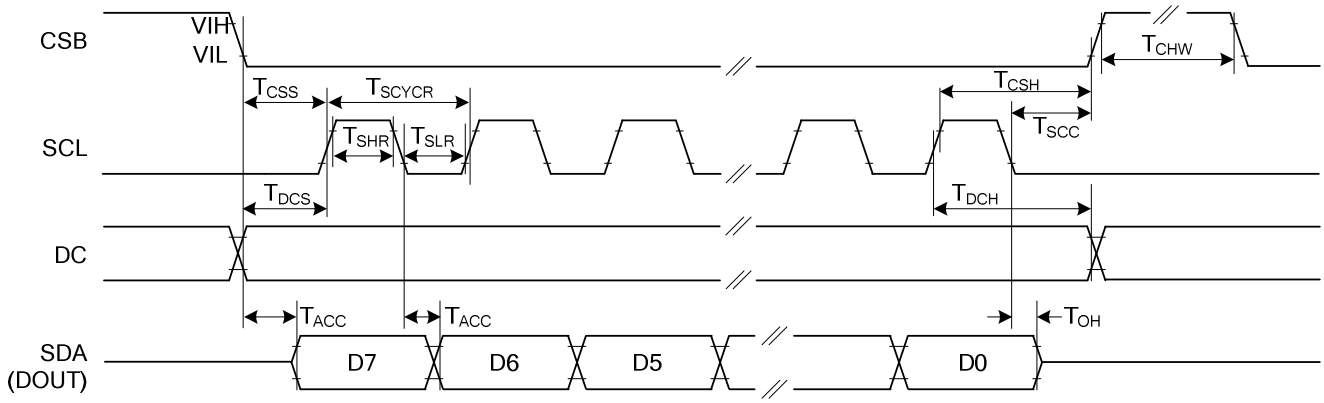


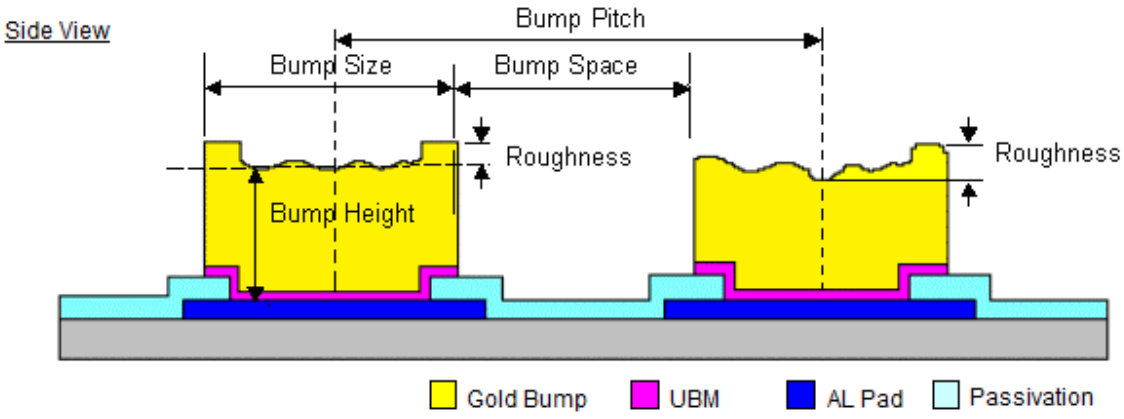
Figure: 4-wire Serial Interface Characteristics (Read mode)

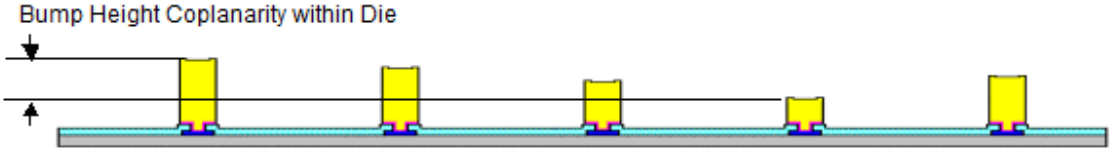
Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{CSS}	CSB	Chip select setup time	60			ns
T_{CSH}		Chip select hold time	65			ns
T_{SCC}		Chip select setup time	20			ns
T_{CHW}		Chip select setup time	40			ns
T_{SCYCW}	SCL	Serial clock cycle (Write)	100			ns
T_{SHW}		SCL “H” pulse width (Write)	35			ns
T_{SLW}		SCL “L” pulse width (Write)	35			ns
T_{SCYCR}		Serial clock cycle (Read)	200			ns
T_{SHR}		SCL “H” pulse width (Read)	60			ns
T_{SLR}		SCL “L” pulse width (Read)	60			ns
T_{DCS}	DC	DC setup time	30			ns
T_{DCH}		DC hold time	30			ns
T_{SDS}	SDA (DIN)	Data setup time	30			ns
T_{SDH}		Data hold time	30			ns
T_{ACC}	SDA (DOUT)	Access time			200	ns
T_{OH}		Output disable time	15			ns

PHYSICAL DIMENSIONS

Die Information

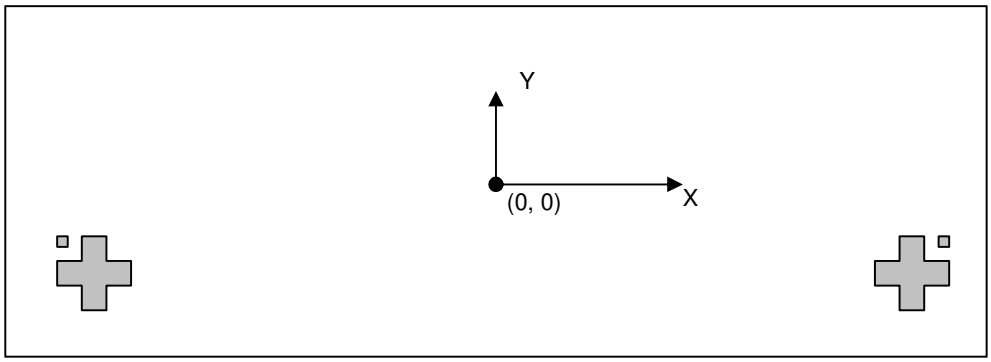
Die Size:	(3530μM±40μM) x (2730μM±40μM)
Die Thickness:	230μM±15μM
Die TTV:	(D_{MAX} – D_{MIN}) within die ⩽ 2μM
Bump Height:	15μM±3μM
	(H_{MAX} – H_{MIN}) within die ⩽ 2μM
Bump Size:	17μMx90μM ± 2μM
Bump Pitch:	30μM
Bump Space:	13μM
Hardness:	65Hv±15Hv
Bump Shear:	⩾ 5g/mil^2
Bump Area:	1530 uM^2
Total bump Area:	563060 uM^2
Coordinate Origin:	Chip center
Pad Reference:	Pad center



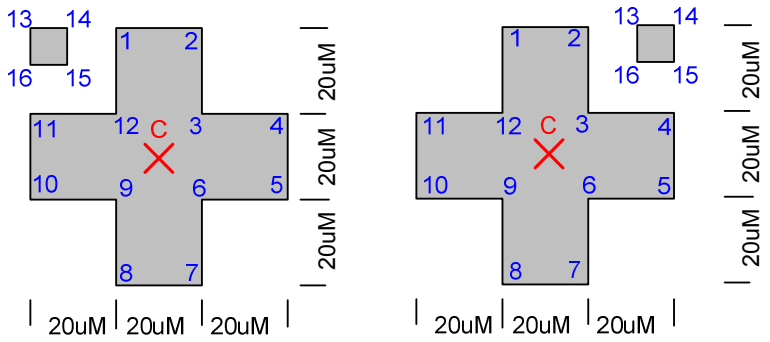


ALIGNMENT MARK INFORMATION

Alignment Mark Location:



Alignment Mark in Detail:



Coordinates:

Point	Left Mark		Right Mark	
	X	Y	X	Y
Center	-1535	-904	1535	-904
1	-1545	-874	1525	-874
2	-1525	-874	1545	-874
3	-1525	-894	1545	-894
4	-1505	-894	1565	-894
5	-1505	-914	1565	-914
6	-1525	-914	1545	-914
7	-1525	-934	1545	-934
8	-1545	-934	1525	-934
9	-1545	-914	1525	-914
10	-1565	-914	1505	-914
11	-1565	-894	1505	-894
12	-1545	-894	1525	-894
13	-1565	-874	1555	-874
14	-1555	-874	1565	-874
15	-1555	-884	1565	-884
16	-1565	-884	1555	-884

PAD COORDINATES

#	PAD	X	Y	W	H
1	C1P	-1656	-1271	28	70
2	C1P	-1610	-1271	28	70
3	C1N	-1564	-1271	28	70
4	C1N	-1518	-1271	28	70
5	C2P	-1472	-1271	28	70
6	C2P	-1426	-1271	28	70
7	C2N	-1380	-1271	28	70
8	C2N	-1334	-1271	28	70
9	C3P	-1288	-1271	28	70
10	C3P	-1242	-1271	28	70
11	C3N	-1196	-1271	28	70
12	C3N	-1150	-1271	28	70
13	C4P	-1104	-1271	28	70
14	C4P	-1058	-1271	28	70
15	C4N	-1012	-1271	28	70
16	C4N	-966	-1271	28	70
17	C5P	-920	-1271	28	70
18	C5P	-874	-1271	28	70
19	C5N	-828	-1271	28	70
20	C5N	-782	-1271	28	70
21	C6P	-736	-1271	28	70
22	C6P	-690	-1271	28	70
23	C6N	-644	-1271	28	70
24	C6N	-598	-1271	28	70
25	VGL	-552	-1271	28	70
26	VGL	-506	-1271	28	70
27	VGL	-460	-1271	28	70
28	VGL	-414	-1271	28	70
29	VGH	-368	-1271	28	70
30	VGH	-322	-1271	28	70
31	VGH	-276	-1271	28	70
32	VGH	-230	-1271	28	70
33	VDM	-184	-1271	28	70
34	VDM	-138	-1271	28	70
35	VDM	-92	-1271	28	70
36	VDM	-46	-1271	28	70
37	VDH	0	-1271	28	70
38	VDH	46	-1271	28	70
39	VDL	92	-1271	28	70
40	VDL	138	-1271	28	70
41	VDD	184	-1271	28	70
42	VDD	230	-1271	28	70
43	VDD	276	-1271	28	70
44	VDD	322	-1271	28	70
45	VDD	368	-1271	28	70
46	VDDDO	414	-1271	28	70
47	VDDD	460	-1271	28	70
48	GND	506	-1271	28	70
49	GND	552	-1271	28	70
50	GND	598	-1271	28	70
51	GND	644	-1271	28	70
52	GND	690	-1271	28	70
53	MS	736	-1271	28	70
54	VDDIO	782	-1271	28	70
55	VDDIO	828	-1271	28	70
56	BS	874	-1271	28	70
57	BUSY_N	920	-1271	28	70

#	PAD	X	Y	W	H
58	RST_N	966	-1271	28	70
59	DC	1012	-1271	28	70
60	CSB	1058	-1271	28	70
61	SCL	1104	-1271	28	70
62	SDA	1150	-1271	28	70
63	TEST5	1196	-1271	28	70
64	TEST4	1242	-1271	28	70
65	TEST2	1288	-1271	28	70
66	TEST3	1334	-1271	28	70
67	CHKGI	1380	-1271	28	70
68	CHKGO	1426	-1271	28	70
69	CDEIO	1472	-1271	28	70
70	CDAIO	1518	-1271	28	70
71	CL	1564	-1271	28	70
72	VDDA	1610	-1271	28	70
73	VDDA	1656	-1271	28	70
74	GNDA	1671	-1182	70	28
75	GNDA	1671	-1136	70	28
76	VPP	1671	-1090	70	28
77	VPP	1671	-1044	70	28
78	VDM	1671	-998	70	28
79	VDM	1671	-952	70	28
80	VCOM	1671	-906	70	28
81	VCOM	1671	-860	70	28
82	G<0>	1681	-796.147	90	17
83	G<2>	1681	-768.147	90	17
84	G<4>	1681	-740.147	90	17
85	G<6>	1681	-712.147	90	17
86	G<8>	1681	-684.147	90	17
87	G<10>	1681	-656.147	90	17
88	G<12>	1681	-628.147	90	17
89	G<14>	1681	-600.147	90	17
90	G<16>	1681	-572.147	90	17
91	G<18>	1681	-544.147	90	17
92	G<20>	1681	-516.147	90	17
93	G<22>	1681	-488.147	90	17
94	G<24>	1681	-460.147	90	17
95	G<26>	1681	-432.147	90	17
96	G<28>	1681	-404.147	90	17
97	G<30>	1681	-376.147	90	17
98	G<32>	1681	-348.147	90	17
99	G<34>	1681	-320.147	90	17
100	G<36>	1681	-292.147	90	17
101	G<38>	1681	-264.147	90	17
102	G<40>	1681	-236.147	90	17
103	G<42>	1681	-208.147	90	17
104	G<44>	1681	-180.147	90	17
105	G<46>	1681	-152.147	90	17
106	G<48>	1681	-124.147	90	17
107	G<50>	1681	-96.147	90	17
108	G<52>	1681	-68.147	90	17
109	G<54>	1681	-40.147	90	17
110	G<56>	1681	-12.147	90	17
111	G<58>	1681	15.853	90	17
112	G<60>	1681	43.853	90	17
113	G<62>	1681	71.853	90	17
114	G<64>	1681	99.853	90	17

#	PAD	X	Y	W	H
115	G<66>	1681	127.853	90	17
116	G<68>	1681	155.853	90	17
117	G<70>	1681	183.853	90	17
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203	S<34>	165	1281	17	90
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#	PAD	X	Y	W	H
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251	DUMMY	-1307	1281	17	90
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261	G<141>	-1587	1281	17	90
262	G<139>	-1615	1281	17	90
263	G<137>	-1643	1281	17	90
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265	DUMMY	-1681	1163.853	90	17
266	DUMMY	-1681	1135.853	90	17
267	DUMMY	-1681	1107.853	90	17
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271	G<129>	-1681	995.853	90	17
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273	G<125>	-1681	939.853	90	17
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275	G<121>	-1681	883.853	90	17
276	G<119>	-1681	855.853	90	17
277	G<117>	-1681	827.853	90	17
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336	VCOM	-1671	-860	70	28
337	VCOM	-1671	-906	70	28
338	VDM	-1671	-952	70	28
339	VDM	-1671	-998	70	28
340	VCOMH	-1671	-1044	70	28
341	VCOMH	-1671	-1090	70	28
342	VCOML	-1671	-1136	70	28
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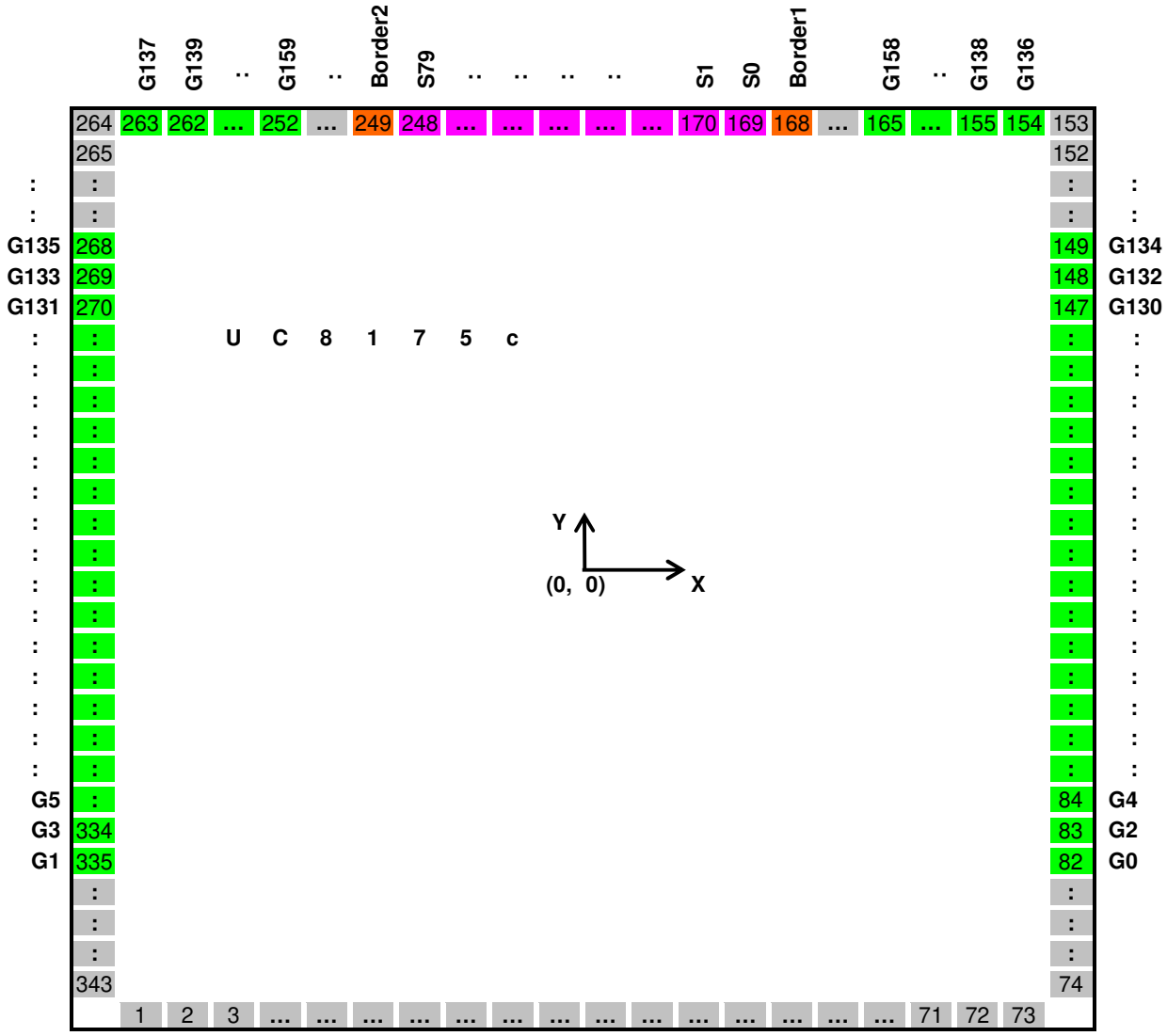
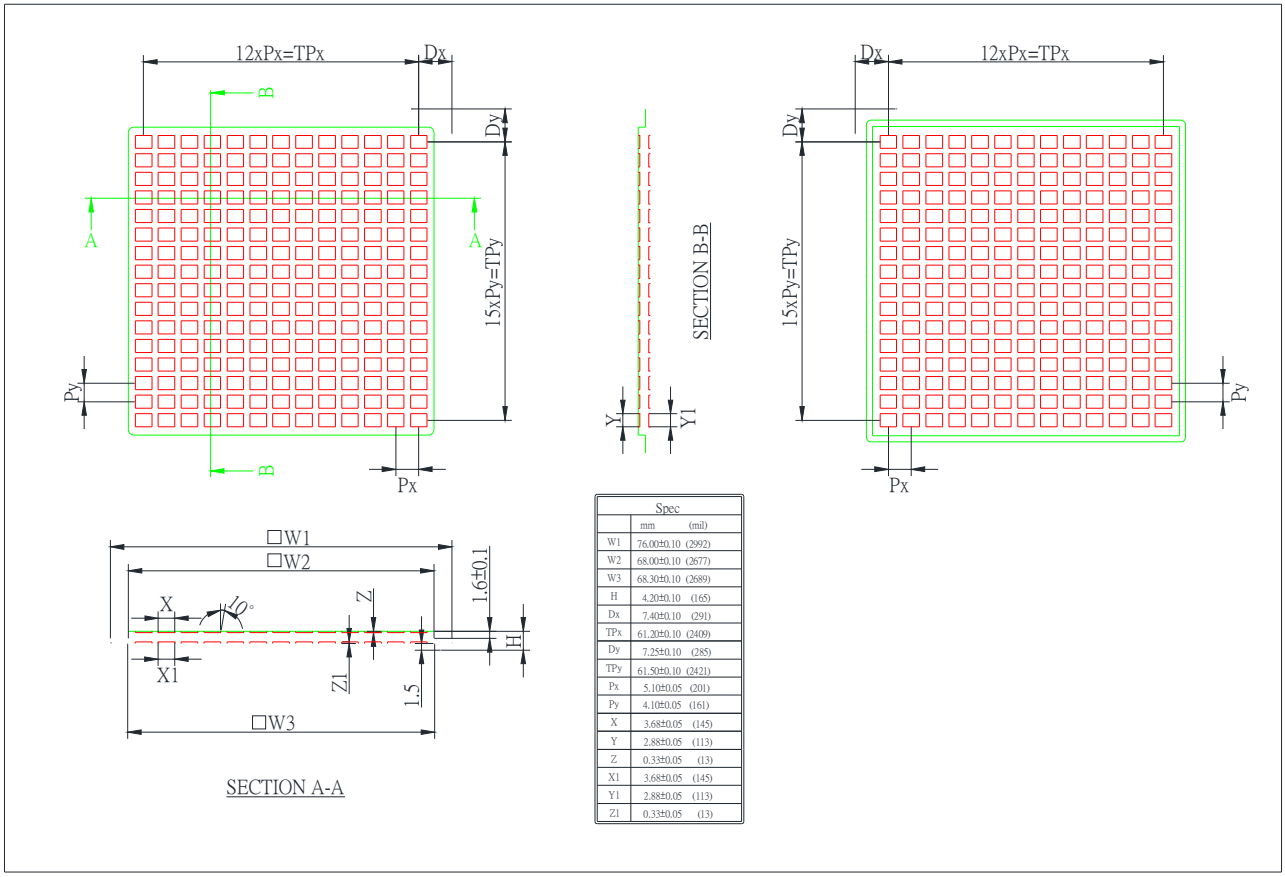
I/O Pad Arrangement



TRAY INFORMATION

3-Inch Tray



Spec		
	mm	(mil)
W1	76.00±0.10	(2992)
W2	68.00±0.10	(2677)
W3	68.30±0.10	(2689)
H	4.20±0.10	(165)
Dx	7.40±0.10	(291)
TPx	61.20±0.10	(2409)
Dy	7.25±0.10	(285)
TPy	61.50±0.10	(2421)
Px	5.10±0.05	(201)
Py	4.10±0.05	(161)
X	3.68±0.05	(145)
Y	2.88±0.05	(113)
Z	0.33±0.05	(13)
X1	3.68±0.05	(145)
Y1	2.88±0.05	(113)
Z1	0.33±0.05	(13)

REVISION HISTORY

Revision	Contents	Date
0.6	First release	Jan. 29 2018
0.7	1. page 39, COMMAND DEFAULT SETTING , CCSET add D0:CCEN 2. page 48, modify the diagram of 4-wire Serial Interface Characteristics (Read mode)	November 28, 2018
0.71	Page 23, REV (R70H) add Chip ID code Page 48,49 , Serial clock cycle (Read) 150ns→200ns	July 25, 2019
0.8	Revise Command Default Setting、Physical Dimensions	May 22, 2020