JD79651AB

Rev. 1.0

User Guide

All-in-one driver with TCON for Color application

fitipower integrated technology Inc.

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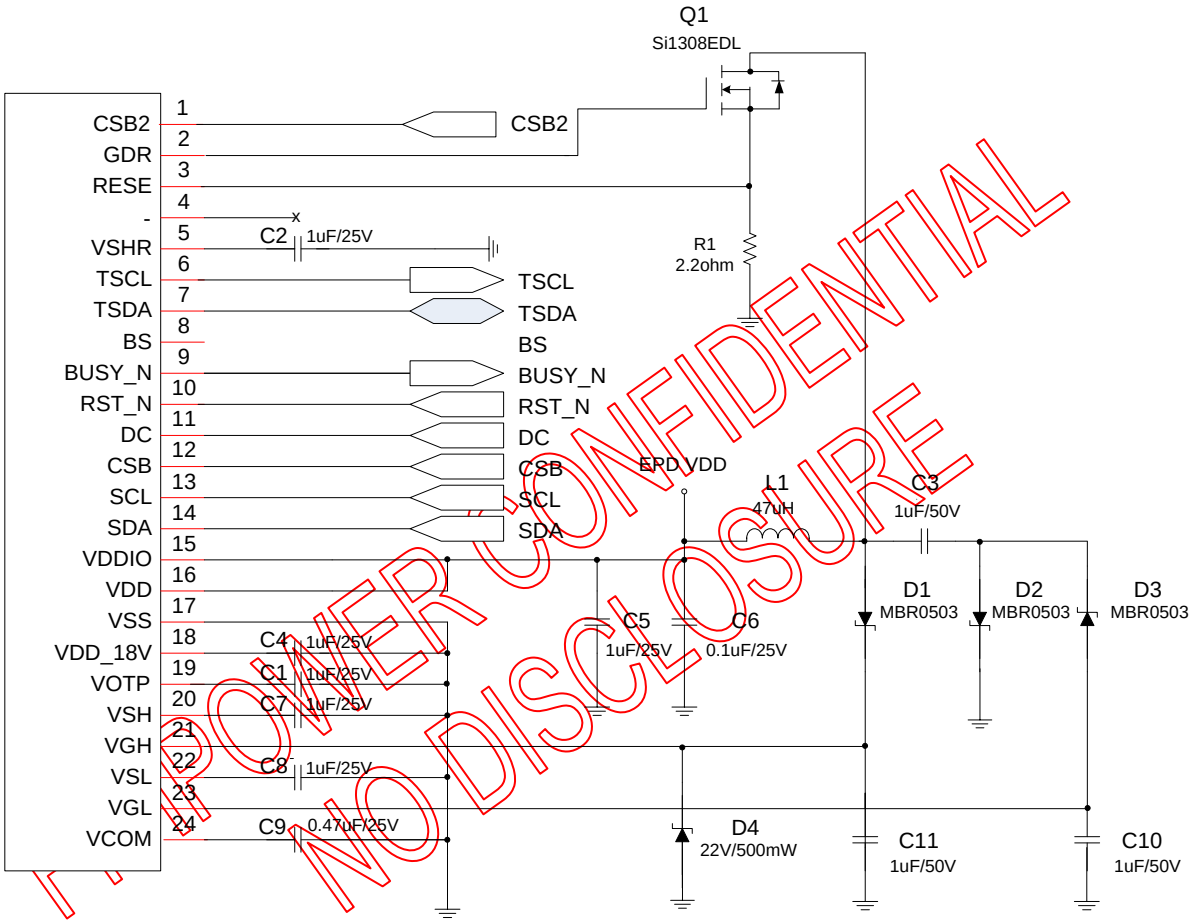
1. APPLICATION CIRCUIT



Note:

1.Power board 可共用新的及其他 compatible IC 的應用電路

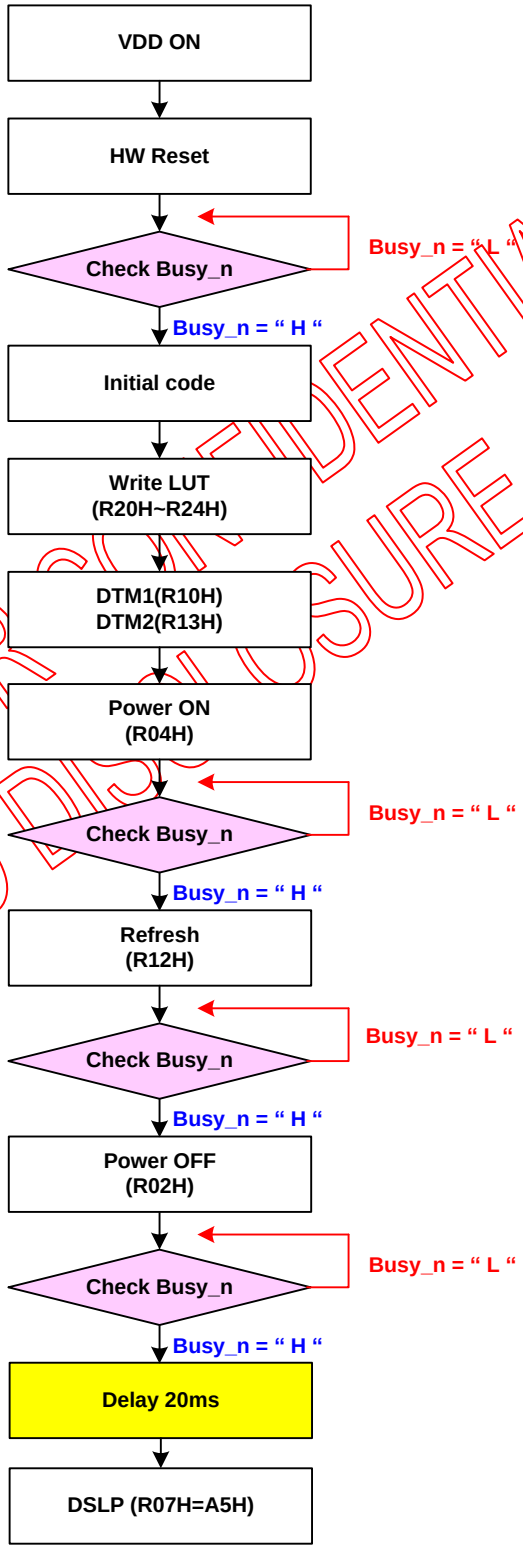
2.OTP 燒錄時，建議 VOTP 需加上電容(1uF)

3.VGH 需加上 Zener-Diode(D4)

4.NMOS(Q1) : VDS>25V、 ID>500mA、VGS(th)<1.5V、 Ciss<200pF、RDS(on)<400mΩ

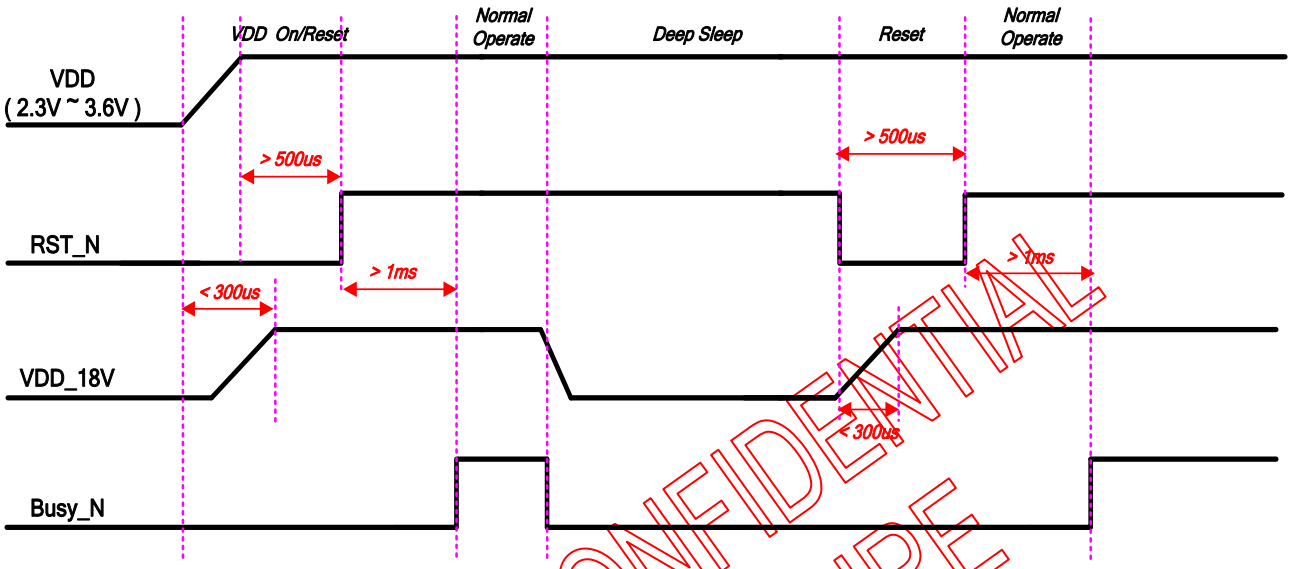
2. DISPLAY FLOW

2.1 Flow



Note: OTP 燒錄後的模組 display flow 不需再寫 LUT

2.3 HW Reset



Note:

1. 重新上電後，務必作 hw reset(low->high)來作重置，確認 IC 回到最初狀態
2. Reset 後需偵測 busy_n 拉 high，來確定此時 IC 重置完成進至 normal 狀態，可以再進行其他動作
3. 進入 deep sleep mode 後，digital 電壓 VDD_18V 已關無法在下 command，如需持續操作要透過外部 hw reset(RST_N : low->high)來喚醒

2.4 Initial Code

2.4.1 Before OTP Model

Description	Address(Hex)	Data(Hex)					Note
Fiti Cmd	4D	55	-	-	-	-	
	87	28	-	-	-	-	
	88	00					
User Cmd	00	EF		-	-	-	
	01	03	00	3F	3F	24	
	06	CF	15	12	-	-	
	26	0F	-	-	-	-	
	30	3C					
	50	57	-	-	-	-	
	61	B0	01	08	-	-	176S x 264G resolution setting
	82	19	-	-	-	-	
	E8	A8	-	-	-	-	

2.4.2 After OTP Model

Description	Address(Hex)	Data(Hex)
Fiti Cmd	4D	55
	87	28
	88	00

Note:

1.上述 user command 的 data 為參考值，需依實際模組狀況調整

2.各面板解析度參考設定如下:

Description	Address(Hex)	Data(Hex)			Resolution
Resolution Setting	61	68	00	D4	104S x 212G
	61	98	00	98	152S x 152G
	61	90	00	C8	144S x 200G
	61	80	00	FA	128S x 250G
	61	80	01	28	128S x 296G
	61	98	01	28	152S x 296G
	61	B0	01	08	176S x 264G

Resolution setting for panel application

2.5 Look-UP Table (LUT)

以下 LUT waveform 為常溫簡單的例子，實際對應的 LUT waveform 需依實際模組 fine tuning；詳細參數設定內容在請參考 register description。

2.5.1 BW Mode Waveform

Name	Address (Hex)	Group 1						Group 2						Group 3					
		P01	P02	P03	P04	P05	P06	P07	P08	P09	P10	P11	P12	P13	P14	P15	P16	P17	P18
LUTC	20	00	28	19	23	00	01	00	03	03	00	00	05	00	08	08	00	00	03
LUTWW	21	10	28	19	23	00	01	90	03	03	00	00	05	90	08	08	00	00	03
LUTBW	22	10	28	19	23	00	01	90	03	03	00	00	05	90	08	08	00	00	03
LUTWB	23	88	28	19	23	00	01	90	03	03	00	00	05	90	08	08	00	00	03
LUTBB	24	88	28	19	23	00	01	90	03	03	00	00	05	90	08	08	00	00	03

Name	Address (Hex)	Group 4						Group 5						Group 6					
		P19	P20	P21	P22	P23	P24	P25	P26	P27	P28	P29	P30	P31	P32	P33	P34	P35	P36
LUTC	20	00	0A	02	05	05	05	00	00	00	00	00	00	00	00	00	00	00	00
LUTWW	21	08	0A	02	05	05	05	00	00	00	00	00	00	00	00	00	00	00	00
LUTBW	22	08	0A	02	05	05	05	00	00	00	00	00	00	00	00	00	00	00	00
LUTWB	23	41	0A	02	05	05	05	00	00	00	00	00	00	00	00	00	00	00	00
LUTBB	24	41	0A	02	05	05	05	00	00	00	00	00	00	00	00	00	00	00	00

Name	Address (Hex)	Group 7					
		P37	P38	P39	P40	P41	P42
LUTC	20	00	00	00	00	00	00
LUTWW	21	00	00	00	00	00	00
LUTBW	22	00	00	00	00	00	00
LUTWB	23	00	00	00	00	00	00
LUTBB	24	00	00	00	00	00	00

Note: VGH/VGL=+/-20V、VSH/VSL=+/-15V @ Frame rate=50Hz

2.5.2 BWR Mode Waveform (for R1.2 Film Application)

Name	Address (Hex)	Group 1						Group 2						Group 3					
		P01	P02	P03	P04	P05	P06	P07	P08	P09	P10	P11	P12	P13	P14	P15	P16	P17	P18
LUTC	20	00	37	05	29	35	01	00	02	02	02	02	0A	00	0F	02	02	0F	03
LUTR	22	0A	37	05	29	35	01	66	02	02	02	02	0A	99	0F	02	02	0F	03
LUTW	23	50	37	05	29	35	01	66	02	02	02	02	0A	99	0F	02	02	0F	03
LUTB	24	08	37	05	29	35	01	66	02	02	02	02	0A	99	0F	02	02	0F	03

Name	Address (Hex)	Group 4						Group 5						Group 6					
		P19	P20	P21	P22	P23	P24	P25	P26	P27	P28	P29	P30	P31	P32	P33	P34	P35	P36
LUTC	20	00	08	03	07	00	03	00	04	08	19	02	04	00	0F	07	01	1E	04
LUTR	22	24	08	03	07	00	03	2C	04	08	19	02	04	2F	0F	07	01	1E	04
LUTW	23	80	08	03	07	00	03	02	04	08	19	02	04	20	0F	07	01	1E	04
LUTB	24	04	08	03	07	00	03	40	04	08	19	02	04	04	0F	07	01	1E	04

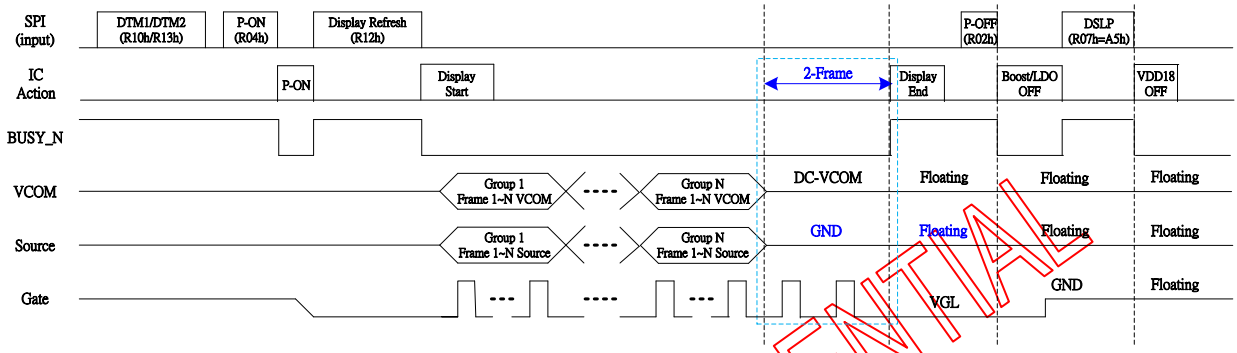
Name	Address (Hex)	Group 7						Group 8						Group 9					
		P37	P38	P39	P40	P41	P42	P43	P44	P45	P46	P47	P48	P49	P50	P51	P52	P53	P54
LUTC	20	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
LUTR	22	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
LUTW	23	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
LUTB	24	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

Name	Address (Hex)	Group 10					
		P55	P56	P57	P58	P59	P60
LUTC	20	00	00	00	00	00	00
LUTR	22	00	00	00	00	00	00
LUTW	23	00	00	00	00	00	00
LUTB	24	00	00	00	00	00	00

Note: VGH/VGL=+/-20V、VSH/VSL=+/-15V、VSHR=7.6V @ Frame rate=50Hz

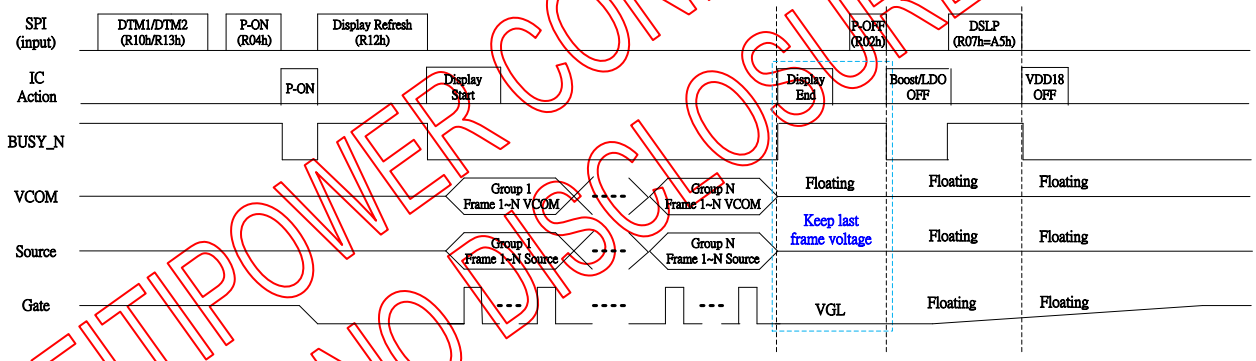
2.5.3 2-Frame ON/OFF of Source

A. 2 frame on - 針對使用在 R1.2(BWR)film 上，適用於 10℃以上設定



. B. 2 frame off - 針對使用在 R1.2(BWR)film 上，適用於 10℃以下設定

設定方式為在 display LUT 結束後，LUTC(R20h) level selection 加上"11"。



2.6 Busy_N Flag

部份 cmd.執行時 busy_n 會拉 low 則 IC 進入工作狀態，工作結束時會再拉回 high；建議執行會 flag 的 cmd.時，MCU 需等 busy_n 拉 high 後再執行其他工作。

Register	Refresh Restriction	BUSY_N flag
R00H(PSR)	X	No action
R01H(PWR)	X	No action
R02H(POF)	X	Flag
R03H(PFS)	X	No action
R04H(PON)	X	Flag
R05H(PMES)	X	No action
R06H(BTST)	X	No action
R07H(DSLP)	X	Flag
R10H(DTM1)	X	No action
R11H(DSP)	Valid only read	Flag
R12H(DRF)	X	Flag
R13H(DTM2)	X	No action
R14(PDTM1)	X	No action
R15(PDTM2)	X	No action
R16(PDRF)	X	Flag
R20H(LUTC)	X	No action
R21H(LUTWW)	X	No action
R22H(LUTBW/LUTR)	X	No action
R23H(LUTWB/LUTW)	X	No action
R24H(LUTBB/LUTB)	X	No action
R25H(LUTC Option)	X	No action
R26H(SET_STG)	Valid in BWR mode	No action
R30H(OSC)	X	No action
R40H(TSC)	Valid only read	Flag
R41H(TSE)	X	No action
R42H(TSW)	X	Flag
R43H(TSR)	Valid only read	Flag
R50H(CDI)	X	No action
R51H(LPD)	Valid only read	Flag
R60H(TCON)	X	No action
R61H(TRES)	X	No action
R62H(TSGS)	X	No action
R70H(REV)	Valid only read	No action
R71H(FLG)	Valid only read	No action
R80H(AMV)	X	Flag
R81H(VV)	Valid	No action
R82H(VDCS)	X	No action
RA0H(PGM)	X	No action
RA1H(APG)	X	Flag
RA2H(ROTP)	X	Flag
RE0H(CCSET)	X	No action
RE5H(TSSET)	X	No action
RE6H(LVSEL)	X	No action
RE7H(PBC)	Valid only read	No action
RE8H(PWS)	X	No action
RE9H(AUTO)	Valid in standby	Flag
REFH(CHKSUM_PG)	X	Flag
RF0H (RM_LUT_CMD	X	No action
RF1H (SET_OTP_BANK)	X	No action
RF2H (RD_CHKSUM)	X	No action
RF3H (CAL_CHKSUM)	X	Flag

3. REGISTER DESCRIPTION

D/CX:0:Command/1:Data

3.1 User Command

3.1.1 R00H(PSR): Panel Setting Register

R00H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PSR	W	0	0	0	0	0	0	0	0	0	00H
1st Parameter	W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	8Fh
2nd Parameter	W	1	VCD	IMCP	BTLDOF	VCMZ	TS	VGL_TIEG	NORG	VC_LUTZ	8Dh

NOTE: "-" Don't care, can be set to VDD or GND level

Description

- The command defines as :

1st Parameter:

Bit	Name	Description
0	RST_N	RST_N function 1: no effect. (default) 0: Booster OFF, Register data are set to their default values, and SEG/BG/VCOM:floating
1	SHD_N	SHD_N function 0 : Booster OFF, register data are kept, and SEG/BG/VCOM are kept floating. 1 : Booster on. (default)
2	SHL	SHL function 0: Shift left; First data=Sn→Sn-1 →⋯→S2→Last data=S1. 1: Shift right: First data=S1→S2 →⋯→Sn-1→Last data=Sn. (default)
3	UD	UD function 0:Scan down; First line=Gn→Gn-1 →⋯→G2→Last line=G1. 1:Scan up; First line=G1→G2 →⋯→Gn-1→Last line=Gn. (default)
4	BWR	Color selection setting 0: Pixel with B/W/Red. Run both LU1 and LU2. (default) 1: Pixel with B/W. Run LU1 only
5	REG_EN	LUT selection setting 0 : Using LUT from OTP(default) 1 : Using LUT from register
7-6	RES[1,0]	Resolution setting 00: Display resolution is 96x230 (default) 01: Display resolution is 96x252 10: Display resolution is 128x296 11: Display resolution is 160x296

Notes:

1. **When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off. SD output and VCOM will base on previous condition and keep floating.**
2. **When RST_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. SD output and VCOM will base on previous condition and keep floating.**

2nd parameter

Bit	Name	Description
0	VC_LUTZ	VCOM status function 0 : Display off, VCOM keep to power off 1 : Display off, VCOM is set to floating (default)
1	NORG	VCOM status function 0 : No effect (default) 1 : Expect refreshing display, VCOM is tied to GND
2	VGLTIEG	VGL power off status function 0 : Power off, VGL will be floating 1 : Power off, VGL will be tied to GND (default)
3	TS	Temperature sensing will be activated automatically one time 0 : Before enabling refresh, temperature sensing on 1 : Before enabling booster, temperature sensing on (default)
4	VCMZ	VCOM status function 0 : No effect (default) 1 : VCOM is always floating
5	BTLDOF	Turn off booster and LDO at same time 0 : Off (default) 1 : On
6	IMCP	SRAM function of KW mode 0 : normal (default) 1 : copy new sram data to old sram data after refreshing
7	VCD	AC-VCOM driver function 0 : over-driver off 1 : over-driver on (default)

Restriction

3.1.2 R01H(PWR): Power Setting Register

R01H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWR	W	0	0	0	0	0	0	0	0	1	01h
1st Parameter	W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03h
2nd Parameter	W	1	-	-	-	-	VCOM_HV	VGHL_LV [2]	VGHL_LV [1]	VGHL_LV [0]	00h
3rd Parameter	W	1	-	-	VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	26h
4th Parameter	W	1	-	-	VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	26h
5th Parameter	W	1	-	VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	06h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as :

1st Parameter:

Bit	Name	Description
0	VDG_EN	**Gate power selection.** 0 : External VDNS power from VGH/VGL pins. (VDNG_EN open) 1 : Internal DCDC function for generate VGH/VGL. (default)
1	VDS_EN	**Source power selection.** 0 : External source power from VSH/VSL/VSHR pins. 1 : Internal DC/DC function for generate VSH/VSL/VSHR (default)

2nd Parameter:

Bit	Name	Description
2-0	VGHL_LV	**VGHL_LV Voltage Level.** 000: VGH=20 v, VGL=-20v 001: VGH=19 v, VGL=-19v 010: VGH=18 v, VGL=-18v 011: VGH=17 v, VGL=-17v 100: VGH=16 v, VGL=-16v 101: VGH=15 v, VGL=-15v
3	VCOM_HV	**VCOM Voltage Level** 0: VCOMH=VSH+VCOMDC,VCOML=VSL+VCOMDC(default) 1: VCOMH=VGH, VCOML=VGL

3rd Parameter: Internal VSH power selection for B/W LUT.

Bit	Name	Description
5-0	VSH	**Internal VSH power selection.**

VSH[5:0]		Voltage(V)	VSH[5:0]		Voltage(V)
000000	00h	2.4	100000	20h	8.8
000001	01h	2.6	100001	21h	9
000010	02h	2.8	100010	22h	9.2
000011	03h	3	100011	23h	9.4
000100	04h	3.2	100100	24h	9.6
000101	05h	3.4	100101	25h	9.8
000110	06h	3.6	100110	26h	10
000111	07h	3.8	100111	27h	10.2
001000	08h	4	101000	28h	10.4
001001	09h	4.2	101001	29h	10.6
001010	0Ah	4.4	101010	2Ah	10.8
001011	0Bh	4.6	101011	2Bh	11
001100	0Ch	4.8	101100	2Ch	11.2
001101	0Dh	5	101101	2Dh	11.4
001110	0Eh	5.2	101110	2Eh	11.6
001111	0Fh	5.4	101111	2Fh	11.8
010000	10h	5.6	110000	30h	12
010001	11h	5.8	110001	31h	12.2
010010	12h	6	110010	32h	12.4
010011	13h	6.2	110011	33h	12.6
010100	14h	6.4	110100	34h	12.8
010101	15h	6.6	110101	35h	13
010110	16h	6.8	110110	36h	13.2
010111	17h	7	110111	37h	13.4
011000	18h	7.2	111000	38h	13.6
011001	19h	7.4	111001	39h	13.8
011010	1Ah	7.6	111010	3Ah	14
011011	1Bh	7.8	111011	3Bh	14.2
011100	1Ch	8	111100	3Ch	14.4
011101	1Dh	8.2	111101	3Dh	14.6
011110	1Eh	8.4	111110	3Eh	14.8
011111	1Fh	8.6	111111	3Fh	15

4th Parameter: Internal VSL power selection for B/W LUT.

Bit	Name	Description
5-0	VSL	**Internal VSL power selection.**

VSL[5:0]		Voltage(V)	VSL[5:0]		Voltage(V)
000000	00h	-2.4	100000	20h	-8.8
000001	01h	-2.6	100001	21h	-9
000010	02h	-2.8	100010	22h	-9.2
000011	03h	-3	100011	23h	-9.4
000100	04h	-3.2	100100	24h	-9.6
000101	05h	-3.4	100101	25h	-9.8
000110	06h	-3.6	100110	26h	-10
000111	07h	-3.8	100111	27h	-10.2
001000	08h	-4	101000	28h	-10.4
001001	09h	-4.2	101001	29h	-10.6
001010	0Ah	-4.4	101010	2Ah	-10.8
001011	0Bh	-4.6	101011	2Bh	-11
001100	0Ch	-4.8	101100	2Ch	-11.2
001101	0Dh	-5	101101	2Dh	-11.4
001110	0Eh	-5.2	101110	2Eh	-11.6
001111	0Fh	-5.4	101111	2Fh	-11.8
010000	10h	-5.6	110000	30h	-12
010001	11h	-5.8	110001	31h	-12.2
010010	12h	-6	110010	32h	-12.4
010011	13h	-6.2	110011	33h	-12.6
010100	14h	-6.4	110100	34h	-12.8
010101	15h	-6.6	110101	35h	-13
010110	16h	-6.8	110110	36h	-13.2
010111	17h	-7	110111	37h	-13.4
011000	18h	-7.2	111000	38h	-13.6
011001	19h	-7.4	111001	39h	-13.8
011010	1Ah	-7.6	111010	3Ah	-14
011011	1Bh	-7.8	111011	3Bh	-14.2
011100	1Ch	-8	111100	3Ch	-14.4
011101	1Dh	-8.2	111101	3Dh	-14.6
011110	1Eh	-8.4	111110	3Eh	-14.8
011111	1Fh	-8.6	111111	3Fh	-15

5th Parameter:

Bit	Name	Description
6-0	**VSHR**	**Internal VSL power selection.**

VSHR[6:0]		Voltage(V)	VSHR[6:0]		Voltage(V)	VSHR[6:0]		Voltage(V)
0000000	00h	2.4	0011101	1Dh	5.3	0111010	3Ah	8.2
0000001	01h	2.5	0011110	1Eh	5.4	0111011	3Bh	8.3
0000010	02h	2.6	0011111	1Fh	5.5	0111100	3Ch	8.4
0000011	03h	2.7	0100000	20h	5.6	0111101	3Dh	8.5
0000100	04h	2.8	0100001	21h	5.7	0111110	3Eh	8.6
0000101	05h	2.9	0100010	22h	5.8	0111111	3Fh	8.7
0000110	06h	3	0100011	23h	5.9	1000000	40h	8.8
0000111	07h	3.1	0100100	24h	6	1000001	41h	8.9
0001000	08h	3.2	0100101	25h	6.1	1000010	42h	9
0001001	09h	3.3	0100110	26h	6.2	1000011	43h	9.1
0001010	0Ah	3.4	0100111	27h	6.3	1000100	44h	9.2
0001011	0Bh	3.5	0101000	28h	6.4	1000101	45h	9.3
0001100	0Ch	3.6	0101001	29h	6.5	1000110	46h	9.4
0001101	0Dh	3.7	0101010	2Ah	6.6	1000111	47h	9.5
0001110	0Eh	3.8	0101011	2Bh	6.7	1001000	48h	9.6
0001111	0Fh	3.9	0101100	2Ch	6.8	1001001	49h	9.7
0010000	10h	4	0101101	2Dh	6.9	1001010	4Ah	9.8
0010001	11h	4.1	0101110	2Eh	7	1001011	4Bh	9.9
0010010	12h	4.2	0101111	2Fh	7.1	1001100	4Ch	10
0010011	13h	4.3	0110000	30h	7.2	1001101	4Dh	10.1
0010100	14h	4.4	0110001	31h	7.3	1001110	4Eh	10.2
0010101	15h	4.5	0110010	32h	7.4	1001111	4Fh	10.3
0010110	16h	4.6	0110011	33h	7.5	1010000	50h	10.4
0010111	17h	4.7	0110100	34h	7.6	1010001	51h	10.5
0011000	18h	4.8	0110101	35h	7.7	1010010	52h	10.6
0011001	19h	4.9	0110110	36h	7.8	1010011	53h	10.7
0011010	1Ah	5	0110111	37h	7.9	1010100	54h	10.8
0011011	1Bh	5.1	0111000	38h	8	1010101	55h	10.9
0011100	1Ch	5.2	0111001	39h	8.1	1010110	56h	11

Note: VSH>VSHR

Restriction	

3.1.3 R02H(POF): Power OFF Command

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
POF	W	0	0	0	0	0	0	0	1	0	02H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power off command, driver will power off base on power off sequence. ● After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N signal will rise from low to high. ● Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. ● SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.
Restriction	This command only active when BUSY_N = "1".

3.1.4 R04H (PON): Power ON Command

R04H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PON	W	0	0	0	0	0	0	1	0	0	04H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ● After power on command, driver will power on base on power on sequence. ● After power on command, BUSY_N signal will drop from high to low. When finishing the power on sequence, BUSY_N signal will rise from low to high.
Restriction	This command only active when BUSY_N = "1".

3.1.5 R06H(BTST): Booster Soft Start Command

R06H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	1	1	0	06H
1st Parameter	W	1	BT_PHA[7]	BT_PHA[6]	BT_PHA[5]	BT_PHA[4]	BT_PHA[3]	BT_PHA[2]	BT_PHA[1]	BT_PHA[0]	17h
2nd Parameter	W	1	BT_PHB[7]	BT_PHB[6]	BT_PHB[5]	BT_PHB[4]	BT_PHB[3]	BT_PHB[2]	BT_PHB[1]	BT_PHB[0]	17h
3rd Parameter	W	1	-	-	BT_PHC[5]	BT_PHC[4]	BT_PHC[3]	BT_PHC[2]	BT_PHC[1]	BT_PHC[0]	17h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command define as follows:

1st Parameter:

Bit	Name	Description
2-0	Driving strength of phase A	000: period 1 001: period 2 010: period 3 011: period 4 100: period 5 101: period 6 110: period 7 111: period 8 (default)
5-3		000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
7-6	Soft start period of phase A	00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

2nd Parameter:

Bit	Name	Description
2-0	Driving strength of phase B	000: period 1 001: period 2 010: period 3 011: period 4 100: period 5 101: period 6 110: period 7 111: period 8 (default)
5-3		000: Strength 1 001: Strength 2 010: Strength 3 (default) 011: Strength 4 100: Strength 5 101: Strength 6 110: Strength 7 111: Strength 8
7-6	Soft start period of phase B	00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS

<table>
<tr><td>Description</td><td>3rd Parameter:
<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>2-0</td><td>Minimum OFF time setting of GDR in phase C</td><td>000: period 1
001: period 2
010: period 3
011: period 4
100: period 5
101: period 6
110: period 7
111: period 8 (default)</td></tr>
<tr><td>5-3</td><td>Driving strength of phase C</td><td>000: Strength 1
001: Strength 2
010: Strength 3 (default)
011: Strength 4
100: Strength 5
101: Strength 6
110: Strength 7
111: Strength 8</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td></td></tr>
</table>

3.1.6 R07H(DSLP): Deep Sleep Command

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSLP	W	0	0	0	0	0	0	1	1	1	07H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be excited if check code = 0xA5.
Restriction	This command only active when BUSY_N = "1".

3.1.7 R10H(DTM1): Data Start Transmission 1 Register

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM1	W	0	0	0	0	1	0	0	0	0	10H
1st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
2nd Parameter	W	1									00h
…	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. **In B/W mode, this command writes "OLD" data to SRAM.** **In B/W/Red mode, this command writes "B/W" data to SRAM.** In Program mode, this command writes "OTP" data to SRAM for programming.
Restriction	

3.1.8 R12H(DRF): Display Refresh Command

R12H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DRF	W	0	0	0	0	1	0	0	1	0	12H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as : ■ While users send this command, driver will refresh display (data/VCOM) base on SRAM data and LUT. After display refresh command, BUSY_N signal will become "0".
Restriction	This command only actives when BUSY_N = "1"

3.1.9 R13H(DTM2): Data Start Transmission 2 Register

R13H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM2	W	0	0	0	0	1	0	0	1	1	13H
1st Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
2nd Parameter	W	1									00h
…	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

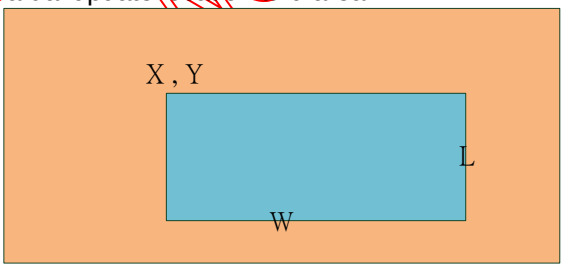
NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. **In B/W mode, this command writes "NEW" data to SRAM.** **In B/W/Red mode, this command writes "RED" data to SRAM.**
Restriction	

3.1.10 R14H(PDTM1): Partial Data Start transmission 1 Register

R14H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDTM1	W	0	0	0	0	1	0	1	0	0	14H
1st Parameter	W	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	00h
2nd Parameter										Y[8]	00h
3rd Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	00h
4th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	00h
5th Parameter										L[8]	00h
6th Parameter	W	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	00h
7th Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

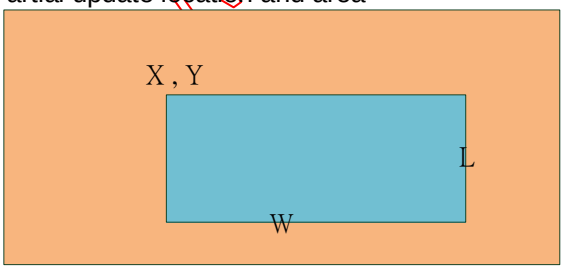
NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "OLD" data to SRAM. In B/W/Red mode, this command writes "B/W" data to SRAM. Partial update location and area  **Note: X and W should be the multiple of 8.**
Restriction	

3.1.11 R15H (PDTM2): Partial Data Start transmission 2 Register

R15H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDTM2	W	0	0	0	0	1	0	1	0	0	15H
1st Parameter	W	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	00h
2nd Parameter										Y[8]	00h
3rd Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	00h
4th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	00h
5th Parameter										L[8]	00h
6th Parameter	W	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	00h
7th Parameter	W	1	KPixel1	KPixel2	KPixel3	KPixel4	KPixel5	KPixel6	KPixel7	KPixel8	00h
	W	1									00h
Mth Parameter	W	1	KPixel(n-7)	KPixel(n-6)	KPixel(n-5)	KPixel(n-4)	KPixel(n-3)	KPixel(n-2)	KPixel(n-1)	KPixel(n)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel. In B/W mode, this command writes "NEW" data to SRAM. In B/W/Red mode, this command writes "RED" data to SRAM. Partial update location and area  **Note: X and W should be the multiple of 8.**
Restriction	

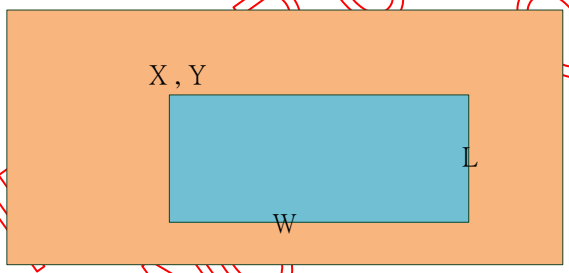
3.1.12 R16H (PDRF): Partial Display Refresh Command

R16H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PDRF	W	0	0	0	0	1	0	1	1	0	16H
1st Parameter	W	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0	00h
			DFV_EN							Y[8]	00h
3rd Parameter	W	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]	00h
4th Parameter	W	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0	00h
										L[8]	00h
6th Parameter	W	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

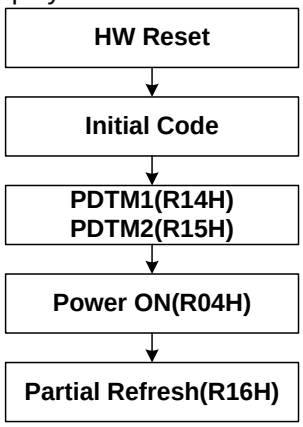
-The command define as follows:
While user sent this command, driver will refresh display (data/VCOM) base on SRAM data and LUT.
Only the area (X,Y, W, L) would update, the others pixel output would follow VCOM LUT
After display refresh command, BUSY_N signal will become "0".



Note: X and W should be the multiple of 8.

DFV_EN: data follow VCOM function on display area.
DFV_EN=1: Only effective in B/W mode, if pixel from "New data" SRAM equal to "Old data" SRAM on display area, this pixel output would follow VCOM LUT.
DFV_EN=0: Data doesn't follow VCOM LUT.

Partial display flow :



Restriction

This command only active when BUSY_N = "1".

3.1.13 R20H(LUTC): LUT for VCOM

R20H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTC	W	0	0	0	1	0	0	0	0	0	20H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~13th Parameter	W	1	2nd state								00h
….	W	1	3rd ~9th state								00h
55th ~60n Parameter	W	1	10th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: This register is set for VCOM LUT. This command stores VCOM Look-Up Table with 10 states of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat. If BWR=0 (BWR mode), User could choose 7~10 groups by R26H (SET_STG) If BWR=1 (BW mode), only 7 groups are used.
Restriction	This command only actives when BUSY_N = "1".

Define	Description
Level selection [1:0]	00: -VCM_DC 01: VSH+VCM_DC. 10: VSL+VCM_DC. 11: Floating.
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame … 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 00000001: 1 … 11111110: 254 11111111: 255

3.1.14 R21H(LUTWW): W2W LUT

R21H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTWW	W	0	0	0	1	0	0	0	0	1	21H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter	W	1	2nd state								00h
….	W	1	3rd ~6th state								00h
37th ~42th Parameter	W	1	7th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:

This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.

Define	Description
Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times

Restriction: This command only actives when BUSY_N = "1".

3.1.15 R22H(LUTBW/LUTR): Black to White LUT or Red LUT Register

R22H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTBW/LUTR	W	0	0	0	1	0	0	0	1	0	22H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter	W	1	2nd state								00h
….	W	1	3rd ~9th state								00h
55th ~60th Parameter	W	1	10th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- The command defines as: This command stores White-to-White Look-Up Table with 10 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat. If BWR=0 (BWR mode), User could choose 7~10 groups by R26H (SET_STG) If BWR=1 (BW mode), only 7 groups are used.
Restriction	This command only actives when BUSY_N = "1".

Define	Description
Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times

3.1.16 R23H(LUTWB/LUTW): White to Black LUT or White LUT Register

R23H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTWB/LUTW	W	0	0	0	1	0	0	0	1	1	23H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter	W	1	2nd state								00h
….	W	1	3rd ~6th state								00h
37th ~42th Parameter	W	1	7th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

- The command defines as:

This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.

Define	Description
Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times

Restriction: This command only actives when BUSY_N = "1".

3.1.17 R24H(LUTBB/LUTB): Black to Black LUT or Black LUT Register

R24H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LUTBB/LUTB	W	0	0	0	1	0	0	1	0	0	24H
1st Parameter	W	1	1st Level selection [1:0]		2nd Level selection [1:0]		3rd Level selection [1:0]		4th level selection[1:0]		00h
2nd Parameter	W	1	1st Frame number [7:0]								00h
3rd Parameter	W	1	2nd Frame number [7:0]								00h
4th Parameter	W	1	3rd Frame number[7:0]								00h
5th Parameter	W	1	4th Frame number[7:0]								00h
6th Parameter	W	1	Repeat numbers[7:0]								00h
7th~12th Parameter	W	1	2nd state								00h
….	W	1	3rd ~6th state								00h
37th ~42th Parameter	W	1	7th state								00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	- The command defines as: This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.

Define	Description
Level selection [1:0]	00: GND 01: VSH 10: VSL 11: VSHR
Frame number [7:0]	00000000 :0 frame 00000001: 1 frame . 11111110: 254 frame 11111111: 255 frame
Repeat numbers [7:0]	00000000 : 0 time 00000001: 1 time . 11111110: 254 times 11111111: 255 times

Restriction	This command only actives when BUSY_N = "1".

3.1.18 R26H (SET_STG): Set VCOM/Red States

R26H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
SET_STG	W	0	0	0	1	0	0	1	1	0	26H
1st Parameter	W	1	-	-	-	-	vcom_stg_sel[1:0]		b2w_stg_sel[1:0]		00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	This command is used to set VCOM/Red LUT states Function of vcom_stg_sel [1:0]/ b2w_stg_sel[1:0] are shown below Value / Stages: 00 / 7; 01 / 8; 10 / 9; 11 / 10 Default is set as 7 stages.
Restriction	These settings are valid for BWR mode.

3.1.19 R30H(PLL): PLL Control Register

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PLL	W	0	0	0	1	1	0	0	0	0	30H
1st Parameter	W	1	-	-	M[2:0]			N[2:0]			3Ch

NOTE: "-" Don't care, can be set to VDD or GND level

Description

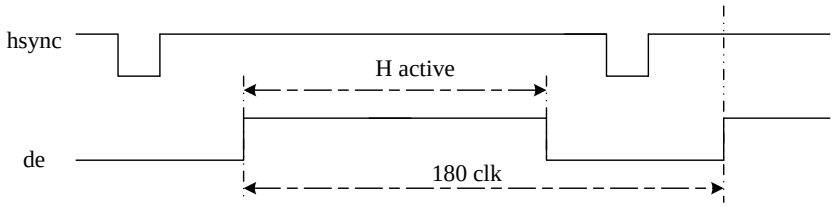
-The command defines as:

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

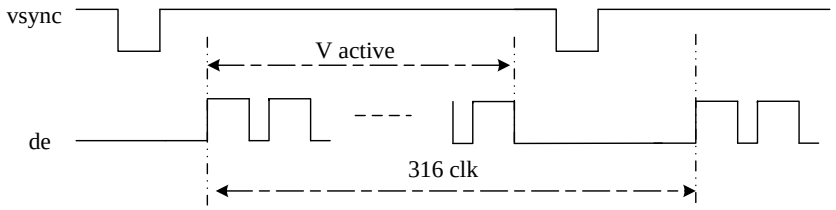
M	N	Frame rate	M	N	Frame rate	M	N	Frame rate	M	N	Frame rate
1	1	29HZ	3	1	86HZ	5	1	150HZ	7	1	200HZ
	2	14HZ		2	43HZ		2	72HZ		2	100HZ
	3	10HZ		3	29HZ		3	48HZ		3	67HZ
	4	7HZ		4	21HZ		4	36HZ		4	50HZ
	5	6HZ		5	17HZ		5	29HZ		5	40HZ
	6	5HZ		6	14HZ		6	24HZ		6	33HZ
	7	4HZ		7	12HZ		7	20HZ		7	29HZ
2	1	57HZ	4	1	114HZ	6	1	171HZ			
	2	29HZ		2	57HZ		2	86HZ			
	3	19HZ		3	38HZ		3	57HZ			
	4	14HZ		4	29HZ		4	43HZ			
	5	11HZ		5	23HZ		5	34HZ			
	6	10HZ		6	19HZ		6	29HZ			
	7	8HZ		7	16HZ		7	24HZ			

remark

-Horizental



-Vertical



Restriction

3.1.20 R40H(TSC): Temperature Sensor Command

R40H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	0	40H
1st Parameter	R	1	D10/TS[9]	D9/TS[8]	D8/TS[7]	D7/TS[6]	D6/TS[5]	D5/TS[4]	D4/TS[3]	D3/TS[2]	-
2nd Parameter	R	1	D2/TS[1]	D1/ TS[0]	D0	-	-	-	-	-	-

NOTE: "-" Don't care, can be set to VDD or GND level

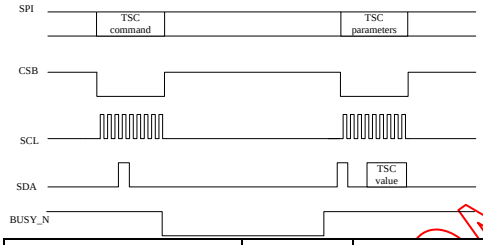
Description

-The command define as follows:

This command indicates the temperature value.

If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.

If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value



TS[9:2]/D[10:3]	T (°C)	TS[9:2]/D[10:3]	T (°C)	TS[9:2]/D[10:3]	T (°C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

TS[1:0]	T (°C)
00	+0
01	+0.25
10	+0.5
11	+0.75

Restriction: This command only actives when BUSY_N = "1".

3.1.21 R41H(TSE): Temperature Sensor Calibration Register

R41H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSE	W	0	0	1	0	0	0	0	0	1	41H
1st Parameter	W	1	TSE	-	-	-	TO[3]	TO[2]	TO[1]	TO[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the driver IC temperature sensor enable and calibration function.

Bit	Description
2-0	mean temperature offset value 000:0℃ 001:1℃ 010:2℃ …. 111:7℃
3	Positive and negative value 0:"+" 1: "-"
7	Internal temperature sensor enable 0: Internal temperature sensor enable.(default) 1: Internal temperature sensor disable, using external temperature sensor.

For example:
1100: - 4℃
0111: + 7℃

Restriction

3.1.22 R50H(CDI): VCOM and DATA Interval Setting Register

R50H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CDI	W	0	0	1	0	1	0	0	0	0	50H
1st Parameter	W	1	VBD[1]	VBD[0]	DDX[1]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	D7h

NOTE: "-" Don't care, can be set to VDD or GND level

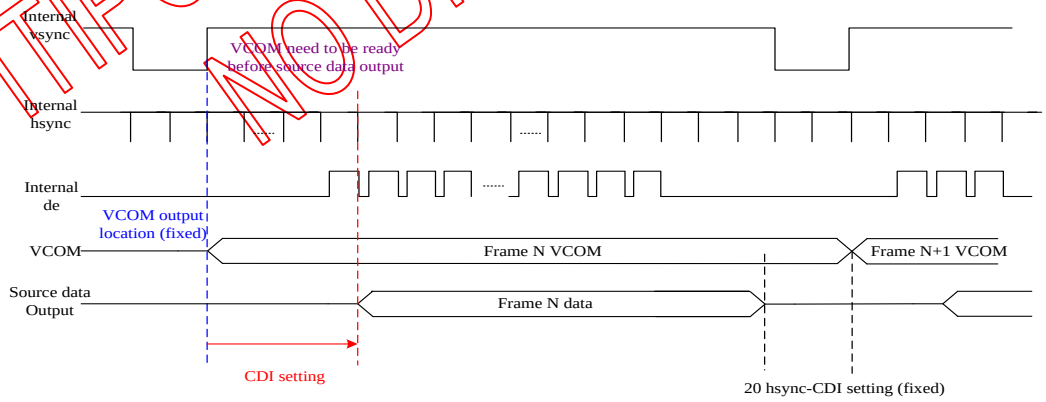
Description

-The command defines as:

CDI[1:0]:

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (20hsync).

Bit	Name	Description
3-0	CDI[3:0]	Vcom and data interval 0000: 17 hsync 0001:16 hsync 0010:15 hsync 0011:14 hsync 0100:13 hsync 0101:12 hsync 0110:11 hsync 0111:10 hsync 1000:9 hsync 1001:8 hsync 1010:7 hsync 1011:6 hsync 1100:5 hsync 1101:4 hsync 1110:3 hsync 1111:2 hsync



VBD[1:0]: Border data selection.

B/W/Red mode(BWR=0)

Bit 4	Bit7-6	Description
DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTR
	10	LUTW
	11	LUTB
1 (default)	00	LUTB
	01	LUTW
	10	LUTR
	11 (default)	Floating

B/W mode (BWR=1)

Bit 4	Bit7-6	description
DDX[0]	VBD[1:0]	LUT
0	00	Floating
	01	LUTBW (1->0)
	10	LUTWB (0->1)
	11	Floating
1 (default)	00	Floating
	01	LUTWB (0->1)
	10	LUTBW (1->0)
	11	Floating

DDX[1:0]: Data polarity
1. DDX[1] for RED data, DDX[0] for BW data in the B/W/Red mode
2. DDX[0] for B/W mode

B/W/Red mode(BWR=0)

Bit 5-4	Description	
DDX[1:0]	Data (DTM2, DTM1)	LUT
00	00	LUTW
	01	LUTB
	10	LUTR
	11	LUTR
01 (default)	00	LUTB
	01	LUTW
	10	LUTR
	11	LUTR
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTB
11	00	LUTR
	01	LUTR
	10	LUTB
	11	LUTW

B/W mode (BWR=1)

Bit 5-4	Description	
DDX[0]	Data (B/W)	LUT
0	00	LUTWW (0->0)
	01	LUTBW(1->0)
	10	LUTWB(0->1)
	11	LUTBB(1->1)
1 (default)	00	LUTBB(0->0)
	01	LUTWB(1->0)
	10	LUTBW(0->1)
	11	LUTWW(1->1)

Restriction	

3.1.23 R51H(LPD): Lower Power Detection Register

R51H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LPD	W	0	0	1	0	1	0	0	0	1	51H
1st Parameter	R	1	-	-	-	-	-	-	-	LPD	--

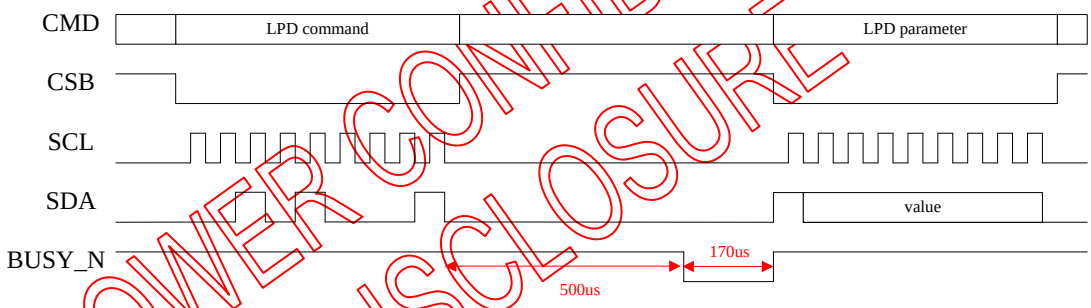
NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the input power condition. Host can read this data to understand the battery's condition.
When LPD="1", system input power is normal.
When LPD="0", system input power is lower (VDD<2.5v, which could be select in RE4H (LVSEL)).

1st Parameter:

Bit 0	LPD
0	Low power input.
1	Normal status.



Restriction

- This command only actives when BUSY_N = "1".

3.1.24 R60H(TCON): TCON Setting

R60H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TCON	W	0	0	1	1	0	0	0	0	0	60H
1st Parameter	W	1	S2G[3]	S2G[2]	S2G[1]-	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	22h

NOTE: "-" Don't care, can be set to VDD or GND level

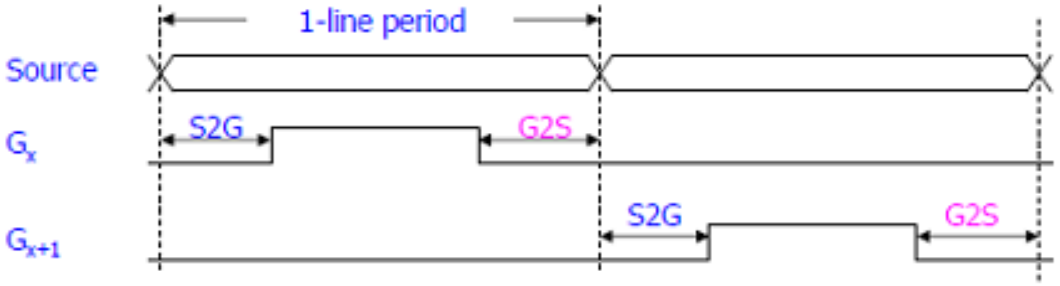
Description

- The command define Non-overlap period of gate and source as below:

1st Parameter:

Bit	Name	Description
7-0	S2G[3:0] G2S[3:0]	0000: 4 clock 0001: 8 clock 0010: 12 clock (default) 0011:16 clock 0100: 20 clock 0101: 24 clock 0110: 28 clock 0111: 32 clock 1000: 36 clock 1001: 40 clock 1010: 44 clock 1011: 48 clock 1100: 52 clock 1101: 56 clock 1110: 60 clock 1111: 64 clock

Period=660ns



Restriction

3.1.25 R61H(TRES): Resolution Setting

R61H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TRES	W	0	0	1	1	0	0	0	0	1	61H
1st Parameter	W	1	HRES[7]	HRES[6]	HRES[5]	HRES[4]	HRES[3]	-	-	-	00h
2nd Parameter	W	1	-	-	-	-	-	-	-	VRES[8]	00h
3th Parameter	W	1	VRES[7]	VRES[6]	VRES[5]	VRES[4]	VRES[3]	VRES[2]	VRES[1]	VRES[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: When using register: Horizontal display resolution = HRES Vertical display resolution = VRES Channel disable calculation: GD : First G active = G0; LAST active GD= first active +VRES[8:0] -1 SD : First active channel: =S0 ; LAST active SD= first active +HRES[7:3]*8-1 EX :128X296 GD: First G active = G0 LAST active GD= 0+296-1= 295; (G295) SD : First active channel: =S0 LAST active SD=0+16*8-1=127; (S127) R61H = 80h, 01h, 28h (解析度直接轉 16 進制即為設定值) **Note: Only supports source 176 ch for source 160ch. above**
Restriction	

3.1.26 R62H(TSGS): Source & gate start setting

R62H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSGS	W	0	0	1	1	0	0	0	1	0	62H
1st Parameter	W	1	S_start (7)	S_start (6)	S_start (5)	S_start (4)	S_start (3)	--	--	--	00h
2nd Parameter	W	1				gscan				G_start [8]	ooh
3rd Parameter	W	1	G_start (7)	G_start (6)	G_start (6)	G_start (4)	G_start (3)	G_start (2)	G_start (1)	G_start (0)	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: 1.S_Start [8:0] describe which source output line is the first date line 2.G_Start[8:0] describe which gate line is the first scan line 3. gscan :Gate scan select 0: Normal scan 1: Cascade type 2 scan
Restriction	S_Start should be the multiple of 8

3.1.27 R68H(IVOTP): Internal VOTP

R68H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
IVOTP	W	0	0	1	1	0	1	0	0	0	68H
1st Parameter	W	1	Internal VOTP[7:0]								00h

Description	- The command can selective external/external VOTP Cmd.(0x68) + Parameter(0x00) : External VOTP (default) Cmd.(0x68) + Parameter(0xA7) : Internal VOTP
Restriction	

3.1.28 R70H(REV): REVISION Register

R70H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
REV	W	0	0	1	1	1	0	0	0	0	70H
1st Parameter	R	1	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]	FFh
2nd Parameter	R	1	REV[15]	REV[14]	REV[13]	REV[12]	REV[11]	REV[10]	REV[9]	REV[8]	FFh

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command defines as: The LUT_REV is read from OTP address = 0x001.& 0x002
Restriction	This command only actives when BUSY_N = "1".

3.1.29 R71H (FLG): Status register

R71H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
FLG	W	0	0	1	1	1	0	0	0	1	71H
1st Parameter	R	1	-		I2C_ERR	II2C_BUSYN	Data_flag	PON	POF	BUSY_N	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

Bit	Name	Description
5	I^2C_ERR	I2C master error status
4	II^2C_BUSYN	I2C master busy status (low active)
3	Data_flag	Driver has already received one frame data
2	PON	PON 0: Not in PON mode 1: In PON mode
1	POF	POF 0: Not in POF mode(default) 1: In POF mode
0	BUSY_N	Driver busy status(low active)

Restriction: User can send this command in any time. It doesn't have restriction of BUSY_N.

3.1.30 R80H(AMV): Auto Measure VCOM Register

R80H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AMV	W	0	1	0	0	0	0	0	0	0	80H
1st Parameter	W	1	-	-	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	10h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command indicates the IC status. Host can read this data to understand the IC status.

1st Parameter:

Bit	Name	Description
0	AMVE	AMVE: Auto Measure Vcom Setting 0: Auto measure VCOM disable (default) 1: Auto measure VCOM enable
1	AMV	AMV: Analog signal 0:Get Vcom value from R81h(default) 1:Get Vcom value in analog signal
2	AMVS	AMVS: setting for Source output of AMV 0: Source output 0V during Auto Measure VCOM period. (default) 1: Source output VSHR during Auto Measure VCOM period.
3	XON	XON: setting for all Gate ON of AMV 0: Gate normally scan during Auto Measure VCOM period. (default) 1: All Gate ON during Auto Measure VCOM period.
5-4	AMVT[1:0]	The sensing time of VCOM detection 00: 3s 01: 5s (default) 10: 8s 11: 10s

After VCOM sensing, use cmd. R81H to return VCOM value

Note:
1.VCOM設定至最小-0.1V(R82h=00h)
2.外部穩壓電容floating

Restriction: This command only actives when BUSY_N = "1".

3.1.31 R81H(VV): VCOM Value register

R81H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VV	W	0	1	0	0	0	0	0	0	1	81H
1st Parameter	R	1	-	-	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command could get the VCOM value

1st Parameter:

Bit	Name	Description
5-0	VV[5:0]	VCOM value

VCOM[5:0]		Voltage(V)	VCOM[5:0]		Voltage(V)	VCOM[5:0]		Voltage(V)
000000	00h	-0.1	010100	14h	-1.1	101000	28h	-2.1
000001	01h	-0.15	010101	15h	-1.15	101001	29h	-2.15
000010	02h	-0.2	010110	16h	-1.2	101010	2Ah	-2.2
000011	03h	-0.25	010111	17h	-1.25	101011	2Bh	-2.25
000100	04h	-0.3	011000	18h	-1.3	101100	2Ch	-2.3
000101	05h	-0.35	011001	19h	-1.35	101101	2Dh	-2.35
000110	06h	-0.4	011010	1Ah	-1.4	101110	2Eh	-2.4
000111	07h	-0.45	011011	1Bh	-1.45	101111	2Fh	-2.45
001000	08h	-0.5	011100	1Ch	-1.5	110000	30h	-2.5
001001	09h	-0.55	011101	1Dh	-1.55	110001	31h	-2.55
001010	0Ah	-0.6	011110	1Eh	-1.6	110010	32h	-2.6
001011	0Bh	-0.65	011111	1Fh	-1.65	110011	33h	-2.65
001100	0Ch	-0.7	100000	20h	-1.7	110100	34h	-2.7
001101	0Dh	-0.75	100001	21h	-1.75	110101	35h	-2.75
001110	0Eh	-0.8	100010	22h	-1.8	110110	36h	-2.8
001111	0Fh	-0.85	100011	23h	-1.85	110111	37h	-2.85
010000	10h	-0.9	100100	24h	-1.9	111000	38h	-2.9
010001	11h	-0.95	100101	25h	-1.95	111001	39h	-2.95
010010	12h	-1	100110	26h	-2	111010	3Ah	-3
010011	13h	-1.05	100111	27h	-2.05			

Restriction

3.1.32 R82H(VDCS): VCOM_DC Setting Register

R82H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VDCS	W	0	1	0	0	0	0	0	1	0	82H
1st Parameter	W	1	-	-	VDCS[5]	VDCS [4]	VDCS [3]	VDCS [2]	VDCS [1]	VDCS [0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command defines as:
This command set the VCOM DC value. Driver will base on this value for VCM_DC.

1st Parameter:

Bit	Name	Function
5-0	VDCS[5:0]	VCOM value

VCOM[5:0]		Voltage(V)	VCOM[5:0]		Voltage(V)	VCOM[5:0]		Voltage(V)
000000	00h	-0.1	010100	14h	-1.1	101000	28h	-2.1
000001	01h	-0.15	010101	15h	-1.15	101001	29h	-2.15
000010	02h	-0.2	010110	16h	-1.2	101010	2Ah	-2.2
000011	03h	-0.25	010111	17h	-1.25	101011	2Bh	-2.25
000100	04h	-0.3	011000	18h	-1.3	101100	2Ch	-2.3
000101	05h	-0.35	011001	19h	-1.35	101101	2Dh	-2.35
000110	06h	-0.4	011010	1Ah	-1.4	101110	2Eh	-2.4
000111	07h	-0.45	011011	1Bh	-1.45	101111	2Fh	-2.45
001000	08h	-0.5	011100	1Ch	-1.5	110000	30h	-2.5
001001	09h	-0.55	011101	1Dh	-1.55	110001	31h	-2.55
001010	0Ah	-0.6	011110	1Eh	-1.6	110010	32h	-2.6
001011	0Bh	-0.65	011111	1Fh	-1.65	110011	33h	-2.65
001100	0Ch	-0.7	100000	20h	-1.7	110100	34h	-2.7
001101	0Dh	-0.75	100001	21h	-1.75	110101	35h	-2.75
001110	0Eh	-0.8	100010	22h	-1.8	110110	36h	-2.8
001111	0Fh	-0.85	100011	23h	-1.85	110111	37h	-2.85
010000	10h	-0.9	100100	24h	-1.9	111000	38h	-2.9
010001	11h	-0.95	100101	25h	-1.95	111001	39h	-2.95
010010	12h	-1	100110	26h	-2	111010	3Ah	-3
010011	13h	-1.05	100111	27h	-2.05			

Restriction

3.1.33 RA0H(PGM): Program Mode

RA0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTIN	W	0	1	0	1	0	0	0	0	0	A0H
1st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is issued, the chip would enter the program mode. The mode would return to standby by hardware reset.
Restriction	

3.1.34 RA1H(APG): Active Program

RA1H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
APG	W	0	1	0	1	0	0	0	0	1	A1H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.
Restriction	The BUSY flag would change state from 0 to 1 while the programming is completed.

3.1.35 RA2H(ROTP): Read OTP Data

RA2H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
ROTP	W	0	1	0	1	0	0	0	1	0	A2H
1st Parameter	R	1	Dummy								-
2nd Parameter	R	1	The data of address 0x0000 in the OTP								-
3rd Parameter	R	1	The data of address 0x0001 in the OTP								-
4th Parameter	R	1	The data of address 0x0002 in the OTP								-
5th Parameter	R	1	The data of address 0x0003 in the OTP								-
6th~(m-1)th Parameter	R	1	…..								-
mth Parameter	R	1	The data of address (n) in the OTP								-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	-The command define as follows: The command is used for reading the content of OTP for checking the data of programming. The value of (n) is depending on the amount of programmed data, the max address = 0x17FF.
Restriction	This command only actives when BUSY_N = "1".

3.1.36 RE0H(CCSET): Cascade Setting

RE0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CCSET	W	0	1	1	1	0	0	0	0	0	E0H
1st Parameter	W	1	-	-	-	-	-	-	TSFIX	CCEIN	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

This command is used for cascade.

1st Parameter:

Bit	
0	Output clock enable/disable. 0: Output 0V at CL pin. (default) 1: Output clock at CL pin for slave chip.
1	Let the value of slave's temperature is same as the master's. 0: Temperature value is defined by internal temperature sensor / external LM75. (default) 1: Temperature value is defined by TS_SET [7:0] registers.
2	Cascade direction 0 : Master(right side output) -> Slave(left side input) 1 : Slave(right side input) <- master(left side output)
3	Cascade LR Select 0:Pin 1:Register(cce_lr)

Restriction

This command only actives when BUSY_N = "1".

3.1.37 RE5H(TSET): Force Temperature

RE5H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSSET	W	0	1	1	1	0	0	1	0	1	E5H
1st Parameter	W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

-The command define as follows:

This command is used to fix the temperature value of master and slave chip in cascade

1st Parameter:

TS_SET[7:0]	T (°C)	TS_SET[7:0]	T (°C)	TS_SET[7:0]	T (°C)
11100111	-25	00000000	0	00011001	25
11101000	-24	00000001	1	00011010	26
11101001	-23	00000010	2	00011011	27
11101010	-22	00000011	3	00011100	28
11101011	-21	00000100	4	00011101	29
11101100	-20	00000101	5	00011110	30
11101101	-19	00000110	6	00011111	31
11101110	-18	00000111	7	00100000	32
11101111	-17	00001000	8	00100001	33
11110000	-16	00001001	9	00100010	34
11110001	-15	00001010	10	00100011	35
11110010	-14	00001011	11	00100100	36
11110011	-13	00001100	12	00100101	37
11110100	-12	00001101	13	00100110	38
11110101	-11	00001110	14	00100111	39
11110110	-10	00001111	15	00101000	40
11110111	-9	00010000	16	00101001	41
11111000	-8	00010001	17	00101010	42
11111001	-7	00010010	18	00101011	43
11111010	-6	00010011	19	00101100	44
11111011	-5	00010100	20	00101101	45
11111100	-4	00010101	21	00101110	46
11111101	-3	00010110	22	00101111	47
11111110	-2	00010111	23	00110000	48
11111111	-1	00011000	24	00110001	49

Restriction

3.1.38 RE6H(LVSEL): LVD voltage Select

RE6H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LVSEL	W	0	1	1	1	0	0	1	1	0	E6H
1st Parameter	W	1	-	-	-	-	-	-	LVD_SEL[1]	LVD_SEL[0]	03h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	LVD_SEL[1:0]: Low power voltage selection 1st Parameter:

LVD_SEL[1:0]	LVD Value
00	< 2.2 V
01	< 2.3 V
10	< 2.4 V
11 (default)	< 2.5 V

Restriction	

3.1.39 RE7H(PBC): Panel Break Check

RE7H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PBC	W	0	1	1	1	0	0	1	1	1	E7H
1st Parameter	R	1	-	-	-	-	-	-	-	PSTA	-

NOTE: "-" Don't care, can be set to VDD or GND level

Description	This command is used to enable panel check, and to disable after reading result. 1st Parameter:

D0	Description
0	Panel check fail (panel broken).
1	Panel check pass

Restriction	

3.1.40 RE8H(PWS): Power Saving

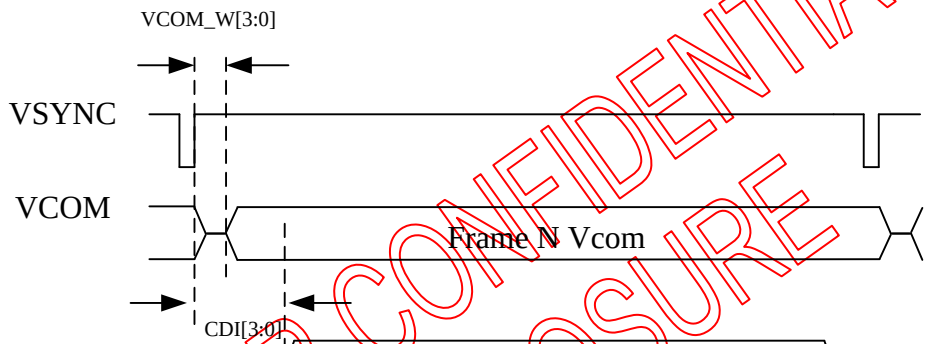
RE8H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWS	W	0	1	1	1	0	1	0	0	0	E8H
1st Parameter	W	1	VCOM_W[3]	VCOM_W[2]	VCOM_W[1]	VCOM_W[0]	SD_W[3]	SD_W[2]	SD_W[2]	SD_W[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

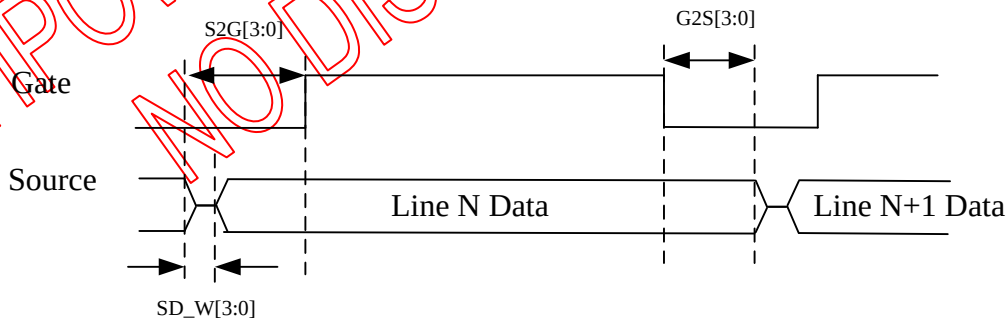
Description

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.1st Parameter:

VCOM_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 660nS)



Restriction

3.1.41 RE9H(AUTO): AUTO Sequence

RE9H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AUTO	W	0	1	1	1	0	1	0	0	1	E9H
1st Parameter	W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	00h

NOTE: "-" Don't care, can be set to VDD or GND level

Description	The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP. AUTO (0xE9) + Code(0xA5) = (PON->DRF->POF) AUTO (0xE9) + Code(0xA7) = (PON->DRF->POF->DSLP)
Restriction	

3.1.42 RF0H(RM_LUT_CMD): Remap LUT Command

RF0H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RM_LUT_CMD	W	0	1	1	1	1	0	0	0	0	F0H
1st Parameter	W	1	-	-	-	tr10_lut_en	rmp2_table_sel[3]	rmp2_table_sel[2]	rmp2_table_sel[1]	rmp2_table_sel[0]	1Fh
2nd Parameter	W	1	-	-	-	tr9_lut_en	rmp1_table_sel[3]	rmp1_table_sel[2]	rmp1_table_sel[1]	rmp1_table_sel[0]	1Fh

NOTE: "-" Don't care, can be set to VDD or GND level

Description: The command is used for indicating backup OTP blocks to remap for LUTs

Addr (hex)	OTP Bank 0 (3K Bytes)	Addr (hex)	OTP Bank 1 (3K Bytes)
00h~0Fh	Temp. segment	C00h~C0Fh	Temp. segment
20h~60h	Default setting	C20h~C60h	Default setting
100h	TR0 WF	D00h	TR0 WF
200h	TR1 WF	E00h	TR1 WF
300h	TR2 WF	F00h	TR2 WF
400h	TR3 WF	1000h	TR3 WF
500h	TR4 WF	1100h	TR4 WF
600h	TR5 WF	1200h	TR5 WF
700h	TR6 WF	1300h	TR6 WF
800h	TR7 WF	1400h	TR7 WF
900h	TR8 WF	1500h	TR8 WF
A00h	TR9 WF / Backup 1	1600h	TR9 WF / Backup 1
B00h	TR10 WF / Backup 2	1700h	TR10 WF / Backup 2

1st Parameter:

tr10_lut_en :

Value	Function
1	OTP Address B00h~BFFh is used as "TR10 WF"
0	OTP Address B00h~BFFh is used as "Backup 2", And you can replace one of TR0 ~TR9.

rmp2_tab_sel [3:0] :

Only be functional when tr10_lut_en is set "0", target LUTs to be replaced is shown below

Value	Target LUTs
0001	TR0
0010	TR1
0011	TR2
0100	TR3
0101	TR4
0110	TR5
0111	TR6
1000	TR7
1001	TR8
1010	TR9
1011~1111	None

2nd Parameter

tr9_lut_en :

Value	Function
1	OTP Address B00h~BFFh is used as “TR9 WF”
0	OTP Address B00h~BFFh is used as “Backup 1”, And you can replace one of TR0 ~TR8.

rmp1_tab_sel[3:0]

Only be functional when tr9_lut_en is set “0”, target LUTs to be replaced is shown below

Value	Target LUTs
0001	TR0
0010	TR1
0011	TR2
0100	TR3
0101	TR4
0110	TR5
0111	TR6
1000	TR7
1001	TR8
1010~1111	None

Note: If rmp1_tab_sel = rmp2_tab_sel , the control hardware will reload “backup 1” block to replace target LUT.

Restriction

3.1.43 RF1H(SET_OTP_BANK): Set OTP Program Bank

RF1H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
SET_OTP_BANK	W	0	1	1	1	1	0	0	0	1	F1H
1st Parameter	W	1	-	-	-	-	-	-	LUT_bank0	reg_bank0	03h

NOTE: "-" Don't care, can be set to VDD or GND level

Description

This command is used to set program bank for registers and LUTs

Addr (hex)	OTP Bank 0 (3K Bytes)	Addr (hex)	OTP Bank 1 (3K Bytes)
00h~0Fh	Temp. segment	C00h~C0Fh	Temp. segment
20h~60h	Default setting	C20h~C60h	Default setting
100h~BFFh	LUTs	D00h~17FFh	LUTs

reg_bank:

Value	Function
1	Program "Temp. segment" and "Default Setting" in bank 0
0	Program "Temp. segment" and "Default Setting" in bank 1

LUT_bank:

Value	Function
1	Program "LUTs" in bank 0
0	Program "LUTs" in bank 1

Restriction

3.1.44 RF2H(RD_CHKSUM): Read Checksum Information

RF2H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RD_CHKSUM	W	0	1	1	1	1	0	0	1	0	F2H
1st ~9th Parameter	R	1	Checksum from "TR0 WF" to "TR8 WF"								-
10th Parameter	R	1	Checksum of "TR9 WF / backup 1"								-
11th Parameter	R	1	Checksum of "TR10 WF / backup 2"								-
12th Parameter	R	1	Checksum comparison result from "TR0 WF" to "TR7 WF"								-
13th Parameter	R	1	Checksum comparison result from "TR8" and "TR10 WF / backup 2"								-

NOTE: "-" Don't care, can be set to VDD or GND level

Description

This command is to read checksum information from OTP.
1st to 11th Parameter : Checksum from "TR0 WF" to "TR10 WF / backup 2"
12th Parameter

D7	D6	D5	D4	D3	D2	D1	D0
fault_TR7	fault_TR6	fault_TR5	fault_TR4	fault_TR3	fault_TR2	fault_TR1	fault_TR0

13th Parameter

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	fault_TR10 / fault_backup2	fault_TR9 / fault_backup1	fault_TR9

definition of fault_TRx / fault_backup_x

Value	Function
0	Checksum comparison : Equal
1	Checksum comparison : Not Equal

Note: Last 2 bytes data 中的 bit 代表相對應溫段的 LUT 是否燒錄正確 (0:正確 / 1:錯誤)
(Ex： 燒錄正確的情況下此處 2 個 byte 皆會讀到"00")

Restriction

3.1.45 RF3H(CAL_CHKSUM): Calculate Checksum

RF3H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CAL_CHKSUM	W	0	1	1	1	1	0	0	1	1	F3H

NOTE: "-" Don't care, can be set to VDD or GND level

Description	This command is used to Calculate Checksum of LUT Table
Restriction	

3.1 FITI Command

FITI command 為 IC 內部相關功能控制的 register；使用 FITI cmd.前皆需先下 0x4Dh=AAh 後方可使用，相關內容可參考下表。

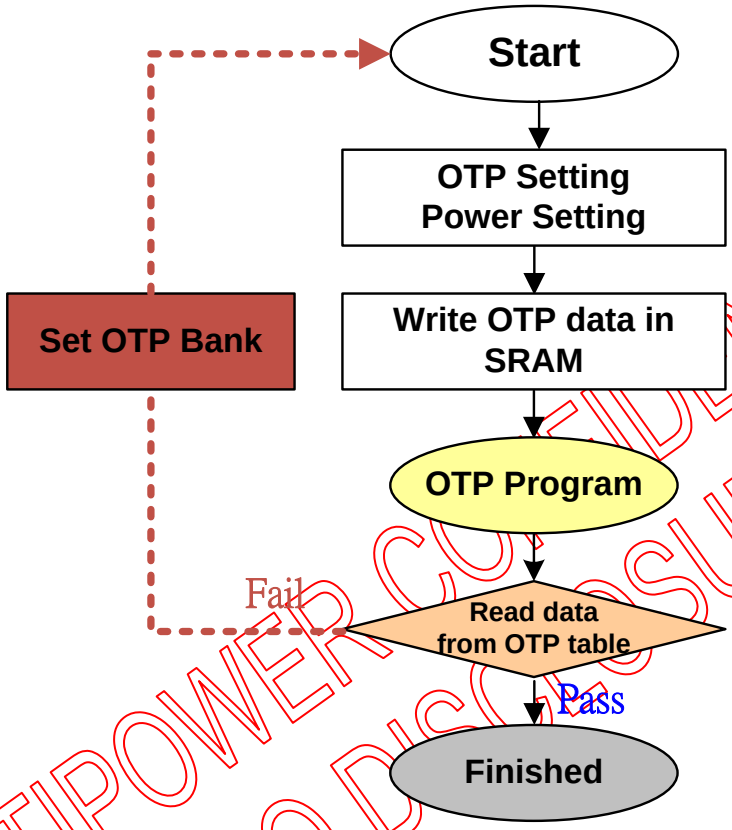
W/R	Address (Hex)	Data (Hex)	Description
W	4D	AA	Enter FITI cmd.
W	BA	2A	After power-off, source keep “HZ” [default]
		0A	After power-off, source keep “GND”
W	BB	02	After display end, source keep “HZ” [default]
		00	After display end, source keep “GND”
W	87	20	R06h(BTST) cannot be used [default]
		28	R06h(BTST) normal use
W	88	00	OSC clk. on
		80	OSC clk. off
W	90	00	R00H_2 BTPOF/IMCP/VCD disable
		10	R00H_2 BTPOF enable
		20	R00H_2 IMCP enable
		40	R00H_2 VCD enable
W	91	0D	R00H_2 VC_LUTZ/NORG/TIEG/TS_AUTO disable
		1D	R00H_2 VC_LUTZ enable
		2D	R00H_2 NORG enable
		4D	R00H_2 TIEG enable
		8D	R00H_2 TS_AUTO enable
W	B4	00	Source 2 frame off – after power-off, VGL keep “HZ” [default]
		80	Source 2 frame off – after power-off, VGL keep “GND”
W	B6	00	Normal – after power-off, VGL keep “HZ”
		80	Normal – after power-off, VGL keep “GND” [default]

3.2 IC Vender ID Read

W/R	Address (Hex)	Data (Hex)	Description
W	F9	00	
R	96	XX	讀取 0x96 會得到 Vender_ID: **61**

4. OTP FLOW AND CONTENT

4.1 Normal OTP Flow



4.1.1 External VOTP Detail Flow

A. ROTP(RA2H) check

Addr.(Hex)	Start Addr.	Counts	R/W	Data(Hex)	Comment
				1.HW reset 2.Check Busy_N = "H"	
F1	1	1	W	0X	03 : Use Bank 0 / 00 : Use Bank 1
A0	1	1	W	A5	PG MODE
10	1	3072	W	XX	寫入欲燒入的 OTP data
				VOTP/VPP 接 7.5V	
A1	0	0	W	-	APG
				1.Delay 20ms 2.Check Busy_N = "H" 3.VOTP/VPP off	
OTP Read				4.HW reset 5.Check Busy_N = "H"	
4D	1	1	W	AA	Setting OTP read mode (normal mode)
C0	1	1	W	20	
A2	1	3073 or 6145	R	XX	檢查 OTP 是否有燒錄成功： - P0 為 dummy - Bank 0: P1~P3072 為燒入的 data (P97~P256 為 FITI 使用，可忽略) - Bank 1: P3073~P6144 為燒入的 data (P3169~P3328 為 FITI 使用，可忽略)

B. CRC(RF2H) check

Addr.(Hex)	Start Addr.	Counts	R/W	Data(Hex)	Comment
				1.HW reset 2.Check Busy_N = "H"	
F1	1	1	W	0X	03 : Use Bank 0 / 00 : Use Bank 1
A0	1	1	W	A5	PG MODE
10	1	3072	W	XX	寫入欲燒入的 OTP data
				VOTP/VPP 接 7.5V	
A1	0	0	W	-	APG
				1.Delay 20ms 2.Check Busy_N = "H" 3.VOTP/VPP off	
CRC Read					
F3	0	0	W	-	計算 OTP checksum
				Delay 10ms	
F2	1	13	R	XX	Read checksum value

4.1.2 Internal VOTP Detail Flow

A. ROTP(RA2H) check

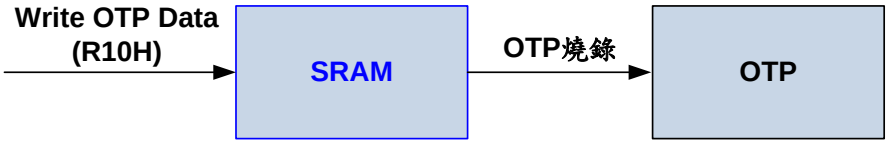
Addr.(Hex)	Start Addr.	Counts	R/W	Data(Hex)	Comment
1.HW reset 2.Check Busy_N = "H"					
F1	1	1	W	0X	03 : Use Bank 0 / 00 : Use Bank1
4D	1	1	W	AA	Setting internal VOTP & Power setting
C0	1	1	W	10	
68	1	1	W	A7	
01	1	5	W	03, 00, 3F, 3F, 35	
87	1	1	W	28	
AF	1	1	W	5D	
06	1	3	W	CF, 15, 12	
04	0	0	W	-	VOTP/VPP Power-on
Check Busy_N = "H"					
A0	1	1	W	A5	PG MODE
10	1	3072	W	XX	寫入欲燒入的 OTP data
A1	0	0	W		APG
1.Delay 20ms 2.Check Busy_N = "H"					
OTP Read				3.HW reset 4.Check Busy_N = "H"	
4D	1	1	W	AA	Setting OTP read mode (normal mode)
C0	1	1	W	20	
A2	1	3073 or 6145	R	XX	檢查 OTP 是否有燒錄成功： - P0 為 dummy - Bank 0: P1~P3072 為燒入的 data (P97~P256 為 FITI 使用，可忽略) - Bank 1: P3073~P6144 為燒入的 data (P3169~P3328 為 FITI 使用，可忽略)

B. CRC(RF2H) check

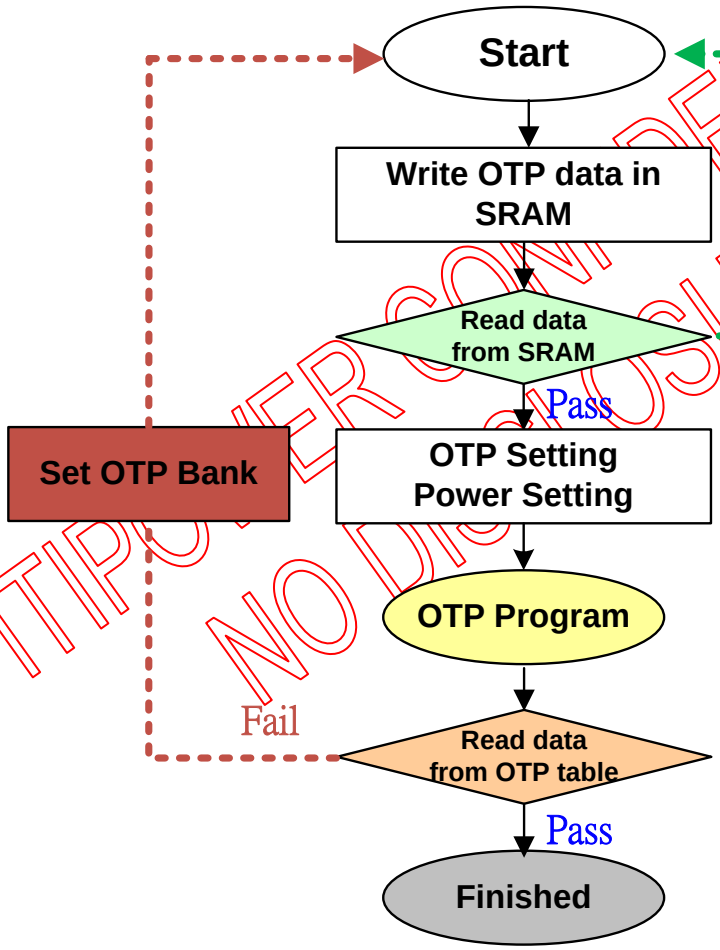
Addr.(Hex)	Start Addr.	Counts	R/W	Data(Hex)	Comment
1.HW reset 2.Check Busy_N = "H"					
F1	1	1	W	0X	03 : Use Bank 0 / 00 : Use Bank1
4D	1	1	W	AA	Setting internal VOTP & Power setting
C0	1	1	W	10	
68	1	1	W	A7	
01	1	5	W	03, 00, 3F, 3F, 35	
87	1	1	W	28	
AF	1	1	W	5D	
06	1	3	W	CF, 15, 12	
04	0	0	W	-	VOTP/VPP Power-on
Check Busy_N = "H"					
A0	1	1	W	A5	PG MODE
10	1	3072	W	XX	寫入欲燒入的 OTP data
A1	0	0	W	-	APG
1.Delay 20ms 2.Check Busy_N = "H"					
CRC Read					
F3	0	0	W	-	計算 OTP checksum
Delay 10ms					
F2	1	13	R	XX	Read checksum value

4.2 OTP Flow with SRAM Detection

A. Block digram



B. Flow



4.2.1 External VOTP Detail Flow with SRAM Detection

A. ROTP(RA2H) check

Addr.(Hex)	Start Addr.	Counts	R/W	Data(Hex)	Comment
1.HW reset 2.Check Busy_N = "H"					
A0	1	1	W	A5	PG MODE
10	1	3072	W	XX	寫入欲燒入的 OTP data
1.HW reset 2.Check Busy_N = "H"					
61	1	3	W	B0, 01, 28	Setting Max. Resolution
F5	1	4220	R	XX	Read OTP SRAM (Note)
Check SRAM data 與寫入的 OTP data 是否相同 (OK：執行後續燒錄動作、NG：重新連接模組，進新複測)					
1.HW reset 2.Check Busy_N = "H"					
F1	1	1	W	0X	03 : Use Bank 0 / 00 : Use Bank 1
A0	1	1	W	A5	PG MODE
10	**0**	**0**	**W**	-	由於前面寫過 data，所以此處不用寫入 data
VOTP/VPP 接 7.5V					
A1	0	0	W	-	APG
1.Delay 20ms 2.Check Busy_N = "H" 3.VOTP/VPP off					
OTP Read 4.HW reset 5.Check Busy_N = "H"					
4D	1	1	W	AA	Setting OTP read mode (normal mode)
C0	1	1	W	20	
A2	1	3073 or 6145	R	XX	檢查 OTP 是否有燒錄成功： - P0 為 dummy - Bank 0: P1~P3072 為燒入的 data (P97~P256 為 FITI 使用，可忽略) - Bank 1: P3073~P6144 為燒入的 data (P3169~P3328 為 FITI 使用，可忽略)

B. CRC(RF2H) check

Addr.(Hex)	Start Addr.	Counts	R/W	Data(Hex)	Comment
1.HW reset 2.Check Busy_N = "H"					
A0	1	1	W	A5	PG MODE
10	1	3072	W	XX	寫入欲燒入的 OTP data
1.HW reset 2.Check Busy_N = "H"					
61	1	3	W	B0, 01, 28	Setting Max. Resolution
F5	1	4220	R	XX	Read OTP SRAM (Note)
Check SRAM data 與寫入的 OTP data 是否相同 (OK：執行後續燒錄動作、NG：重新連接模組，進新複測)					
1.HW reset 2.Check Busy_N = "H"					
F1	1	1	W	0X	03 : Use Bank 0 / 00 : Use Bank 1
A0	1	1	W	A5	PG MODE
10	**0**	**0**	**W**	**-**	由於前面寫過 data，所以此處不用寫入 data
VOTP/VPP 接 7.5V					
A1	0	0	W	-	APG
CRC Read				1.Delay 20ms 2.Check Busy_N = "H" 3.VOTP/VPP off	
F3	0	0	W	-	計算 OTP checksum
Delay 10ms					
F2	1	13	R	XX	Read checksum value

4.2.2 Internal VOTP Detail Flow with SRAM Detection

A. ROTP(RA2H) check

Addr.(Hex)	Start Addr.	Counts	R/W	Data(Hex)	Comment
1.HW reset 2.Check Busy_N = "H"					
A0	1	1	W	A5	PG MODE
10	1	3072	W	XX	寫入欲燒入的 OTP data
1.HW reset 2.Check Busy_N = "H"					
61	1	3	W	B0, 01, 28	Setting Max. Resolution
F5	1	4220	R	XX	Read OTP SRAM (Note)
Check SRAM data 與寫入的 OTP data 是否相同 (OK：執行後續燒錄動作、NG：重新連接模組，進新複測)					
1.HW reset 2.Check Busy_N = "H"					
F1	1	1	W	0X	03 : Use Bank 0 / 00 : Use Bank1
4D	1	1	W	AA	Setting internal VOTP & Power setting
C0	1	1	W	10	
68	1	1	W	A7	
01	1	5	W	03, 00, 3F, 3F, 35	
87	1	1	W	28	
AF	1	1	W	5D	
06	1	3	W	CF, 15, 12	
04	0	0	W	-	VOTP/VPP Power-on
Check Busy_N = "H"					
A0	1	1	W	A5	PG MODE
10	**0**	**0**	**W**	**-**	由於前面寫過 data，所以此處不用寫入 data
A1	0	0	W	-	APG
1.Delay 20ms 2.Check Busy_N = "H"					
OTP Read				3.HW reset 4.Check Busy_N = "H"	
4D	1	1	W	AA	Setting OTP read mode (normal mode)
C0	1	1	W	20	
A2	1	3073 or 6145	R	XX	檢查 OTP 是否有燒錄成功： - P0 為 dummy - Bank 0: P1~P3072 為燒入的 data (P97~P256 為 FITI 使用，可忽略) - Bank 1: P3073~P6144 為燒入的 data (P3169~P3328 為 FITI 使用，可忽略)

B. CRC(RF2H) check

Addr.(Hex)	Start Addr.	Counts	R/W	Data(Hex)	Comment
1.HW reset 2.Check Busy_N = "H"					
A0	1	1	W	A5	PG MODE
10	1	3072	W	XX	寫入欲燒入的 OTP data
1.HW reset 2.Check Busy_N = "H"					
61	1	3	W	B0, 01, 28	Setting Max. Resolution
F5	1	4220	R	XX	Read OTP SRAM (Note)
Check SRAM data 與寫入的 OTP data 是否相同 (OK：執行後續燒錄動作、NG：重新連接模組，進新複測)					
1.HW reset 2.Check Busy_N = "H"					
F1	1	1	W	0X	03 : Use Bank 0 / 00 : Use Bank1
4D	1	1	W	AA	Setting internal VOTP & Power setting
C0	1	1	W	10	
68	1	1	W	A7	
01	1	5	W	03, 00, 3F, 3F, 35	
87	1	1	W	28	
AF	1	1	W	5D	
06	1	3	W	CF, 15, 12	
04	0	0	W	-	VOTP/VPP Power-on
Check Busy_N = "H"					
A0	1	1	W	A5	PG MODE
10	**0**	**0**	**W**	**-**	由於前面寫過 data，所以此處不用寫入 data
A1	0	0	W	-	APG
CRC Read				1.Delay 20ms 2.Check Busy_N = "H"	
F3	0	0	W	-	計算 OTP checksum
Delay 10ms					
F2	1	13	R	XX	Read checksum value

Note:

1. SRAM 讀取的資料前兩筆為 dummy data

2.SRAM 讀取的 OTP 資料與寫入的 OTP data MSB-LSB 為相反

Example1	Write data	Read SRAM data
Hex	A2	45
Bin	10100010	01000101

3.從 SRAM 讀取的 OTP 資料非連續序列

- **每 16 個 bytes 會空 6 個 bytes 為無效數據，需空掉此 6 個 bytes 後的 16 bytes 才是接下來的寫入 data**

1st SRAM read	0x00 ~ 0x15
dummy data	0x16 ~ 0x21
2nd SRAM read	0x22 ~ 0x37
dummy data	0x38 ~ 0x43
⋮	
dummy data	0x4196 ~ 0x4201
192th SRAM read	0x4202 ~ 0x4217
dummy data	0x4128 ~ 0x4133

4.3 OTP Content

OTP bank 0 (3K bytes)		OTP bank 1 (3K bytes)	
Address(Hex)	**Content**	**Address(Hex)**	**Content**
000~01F	Temp. segment	C00~C1F	Temp. segment
020~04D	Default setting	C20~C4D	Default setting
100~1FF	TR0 WF	D00~DFF	TR0 WF
200~2FF	TR1 WF	E00~EFF	TR1 WF
300~3FF	TR2 WF	F00~FFF	TR2 WF
400~4FF	TR3 WF	1000~10FF	TR3 WF
500~5FF	TR4 WF	1100~11FF	TR4 WF
600~6FF	TR5 WF	1200~12FF	TR5 WF
700~7FF	TR6 WF	1300~13FF	TR6 WF
800~8FF	TR7 WF	1400~14FF	TR7 WF
900~9FF	TR8 WF	1500~15FF	TR8 WF
A00~AFF	TR9 WF / Backup 1	1600~16FF	TR9 WF / Backup 1
B00~BFF	TR10 WF / Backup 2	1700~17FF	TR10 WF / Backup 2

Description	OTP Address(Hex)	Note
Temp.	000 ~ 01F	0x000 = A5
User Cmd	020~ 04D	1. 0x020 = A5h 2. Reserved 需填入 FFh 即可: 0x00D ~ 0x01F、0x02B、0x02F ~ 0x032、0x042、0x046 ~ 0x048、0x04A、0x04E ~ 0x05F **3. 0x00D~0x014 可讓客戶任意燒錄需要的資訊於此處，若無使用填入 “FFh”即可** 4. 0x049、0x04B ~ 0x04D 如為 single chip 此處也填 FFh
FITI Cmd	060 ~ 0FF	此區域 OTP data 全部填入 FFh
LUT	100 ~ BFF	此區域沒有用到的溫段 LUT 位置皆填入 FFh

4.3.1 Temperature Segment

Address (Dec)	Address (Hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	000	otp_chk (A5)							
1	001	otp_ver [7:0]							
2	002	otp_ver [15:8]							
3	003	otp_temp0							
4	004	otp_temp1							
5	005	otp_temp2							
6	006	otp_temp3							
7	007	otp_temp4							
8	008	otp_temp5							
9	009	otp_temp6							
10	00A	otp_temp7							
11	00B	otp_temp8 (optional)							
12	00C	otp_temp9 (optional)							
13~31	00D ~ 01F	Reserved							

Note:

1. Temp. segment 內 0x000 OTP data 需設定為 A5h

2. otp_temp N-1 ≦ TR N < otp_temp N ≦ TR N+1 < otp_temp N+1

(EX: otp_temp4=20 度、otp_temp5=25 度，T-sensing 溫度為 20 度~24 度，此時會去抓 TR5 WF)

3.最高溫度點需設 7F (EX:切 7 個溫段 otp_temp6 需設 7F)

4.3.2 Default Setting

Cmd.	Addr. (Dec)	Addr. (Hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value (Hex)
--	32	020	Enable OTP Setting (0xA5)								A5
R00H_1	33	021	RES[1:0]		REG_EN	BWR	UD	SHL	SHD_N	RST_N	8F
R01H	34	022	-	-	-	-	-	-	VDS_EN	VDG_EN	03
	35	023	-	-	-	-	VCOM_HV	VGHL_LV[2:0]			00
	36	024	-	-	VSH[5:0]						26
	37	025	-	-	VSL[5:0]						26
	38	026	-	VSHR[6:0]							06
R03H	39	027	-	-	VSH_OFF[1:0]		VSL_OFF[1:0]		VSHR_OFF[1:0]		00
R06H	40	028	BT_PHA[7:0]								17
	41	029	BT_PHB[7:0]								17
	42	02A	-	-	BT_PHC[5:0]						17
R00H_2	43	02B	VCD	IMCP	BTPOF	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	8D
R16H	44	02C	DFV_EN	-	-	-	-	-	-	-	00
RE6H	45	02D	-	-	-	-	-	-	LVD_SEL[1:0]		03
RE8H	46	02E	VCOM_W[3:0]				SD_W[3:0]				00
--	47 ~ 50	02F~032	Reserved								FF
R30H	51	033	-	-	M[2:0]			N[2:0]			3A
R41H	52	034	TSE	-	-	-	TO[3:0]				00
R42H	53	035	WATTR[7:0]								00
	54	036	WMSB[7:0]								00
	55	037	WLSB[7:0]								00
R50H	56	038	VBD[1:0]		DDX[1:0]		CDI[3:0]				D7
R60H	57	039	S2G[3:0]				G2S[3:0]				22
R26H	58	03A	-	-	-	-	VCOM_STG_SEL[1:0]		B2W_STG_SEL[1:0]		00
R61H	59	03B	HRES[7:3]					-	-	-	00
	60	03C	-	-	-	-	-	-	-	VRES[8]	00
	61	03D	VRES[7:0]								00
R80H	62	03E	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE	10
R82H	63	03F	-	VDCS[6:0]							00
RE0H	64	040	-	-	-	-	CCE_SEL	CCE_LR	TSFIX	CCEIN	00
RE5H	65	041	TS_SET[7:0]								00
--	66	042	Reserved								FF
R62H	67	043	S_Start[7:3]					-	-	-	00
	68	044	-	-	-	G_Scan	-	-	-	G_Start[8]	00
	69	045	G_Start[7:0]								00
RF0H	70	046	-	-	-	tr10_lut_en	rmp2_table_sel				1F
	71	047	-	-	-	tr9_lut_en	rmp1_table_sel				1F
RF1H	72	048	-	-	-	-	-	-	LUT_Bank0	REG_Bank0	03
	Slave setting										
R00H	73	049	slv_res[1:0]		slv_reg_en	slv_bwr	slv_ud	slv_shl	-	slv_rst_n	FF
--	74	04A	Reserved								FF
R62H	75	04B	slv_sstart[7:3]					-	-	-	FF
	76	04C	-	-	-	slv_gscan	-	-	-	slv_gstart[8]	FF
	77	04D	slv_gstart[7:0]								FF

Note:

1.Default setting 內 0x020 OTP data 需設定為 A5h

2.OTP 0x048 燒入值會依照 register cmd.(RF1H)下 code 值來做燒入

3.上表 value 請參考，需依實際 initial code 為主來填入

4.3.3 LUT Setting

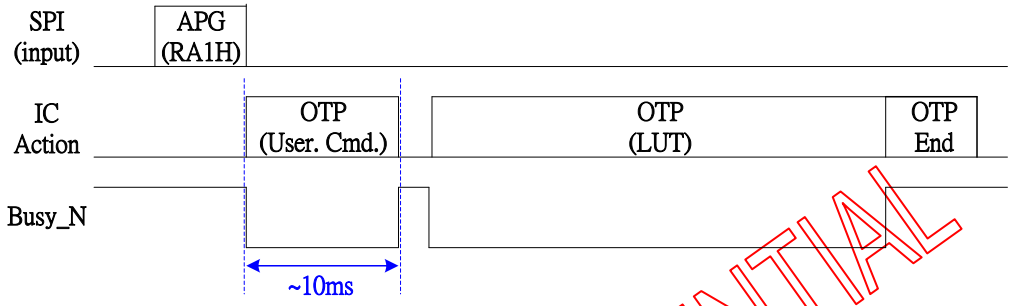
TR0~10 WF is the same as TR0 defined as below:

Description		Addr.(dec)	Addr.(Hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	PS1
TR0 WF	Voltage	256	100			M[2:0]			N[2:0]			
		257	101			VSH[5:0]						
		258	102			VSL[5:0]						
		259	103		VSHR[6:0]							
		260	104			VDCS[5:0]						
		261	105		VGHL_LV[2:0]					XON[9:8]		
		262	106	XON[7:0]								
		263	107							VCOMH[9:8]		
		264	108	VCOMH[7:0]								
	LUTC	265	109	1st Level selection[1:0]		2nd Level selection[1:0]		3rd Level selection[1:0]		4th Level selection[1:0]		Stage 1
		266	10A	1st Frame number[7:0]								
		267	10B	2nd Frame number[7:0]								
		268	10C	3rd Frame number[7:0]								
		269	10D	4th Frame number[7:0]								
		270	10E	Repeat number[7:0]								
		271	10F	Stage 2 ~ Stage 10								
		324	144									
	LUTWW	325	145	1st Level selection[1:0]		2nd Level selection[1:0]		3rd Level selection[1:0]		4th Level selection[1:0]		Stage 1
		326	146	1st Frame number[7:0]								
		327	147	2nd Frame number[7:0]								
		328	148	3rd Frame number[7:0]								
		329	149	4th Frame number[7:0]								
		330	14A	Repeat number[7:0]								
		331	14B	Stage 2 ~ Stage 7								
		366	16E									
	LUTBW / LUTR	367	16F	1st Level selection[1:0]		2nd Level selection[1:0]		3rd Level selection[1:0]		4th Level selection[1:0]		Stage 1
		368	170	1st Frame number[7:0]								
		369	171	2nd Frame number[7:0]								
		370	172	3rd Frame number[7:0]								
		371	173	4th Frame number[7:0]								
		372	174	Repeat number[7:0]								
		373	175	Stage 2 ~ Stage 10								
		426	1AA									
	LUTWB / LUTW	427	1AB	1st Level selection[1:0]		2nd Level selection[1:0]		3rd Level selection[1:0]		4th Level selection[1:0]		Stage 1
		428	1AC	1st Frame number[7:0]								
		429	1AD	2nd Frame number[7:0]								
		430	1AE	3rd Frame number[7:0]								
		431	1AF	4th Frame number[7:0]								
		432	1B0	Repeat number[7:0]								
		433	1B1	Stage 2 ~ Stage 7								
		468	1D4									
	LUTBB / LUTB	469	1D5	1st Level selection[1:0]		2nd Level selection[1:0]		3rd Level selection[1:0]		4th Level selection[1:0]		Stage 1
		470	1D6	1st Frame number[7:0]								
		471	1D7	2nd Frame number[7:0]								
		472	1D8	3rd Frame number[7:0]								
		473	1D9	4th Frame number[7:0]								
		474	1DA	Repeat number[7:0]								
		475	1DB	Stage 2 ~ Stage 7								
		510	1FE									

Note: TR0~10 WF table value will be defined according to the panel performance

4.4 BUSY_N flag of OTP Program

RA1H 燒錄的期間，OTP 會分成兩部份(user cmd. & LUT)去燒錄，所以 busy_n 會分兩次拉 low，建議下 APG(RA1H) cmd.後，**delay 20ms** 再做 busy_n 拉 high 的偵測，來確定是否燒錄完成。



5. REVISION HISTORY

Revision	Content	Date
1.0	New Issue	2019/12/27