EK79652AA

Rev. 0.1

PRELIMINARY DATA SHEET

All-in-one driver with TCON for Color application

fitipower integrated technology Inc.

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All-in-one driver with TCON for Color application

1. GENERAL DESCRIPTION

This driver is an all-in-one driver with timing controller for color application. The outputs have 1-bit white/black and 1-bit red resolution output per pixel. The timing controller provides control signals for the source driver and gate drivers.

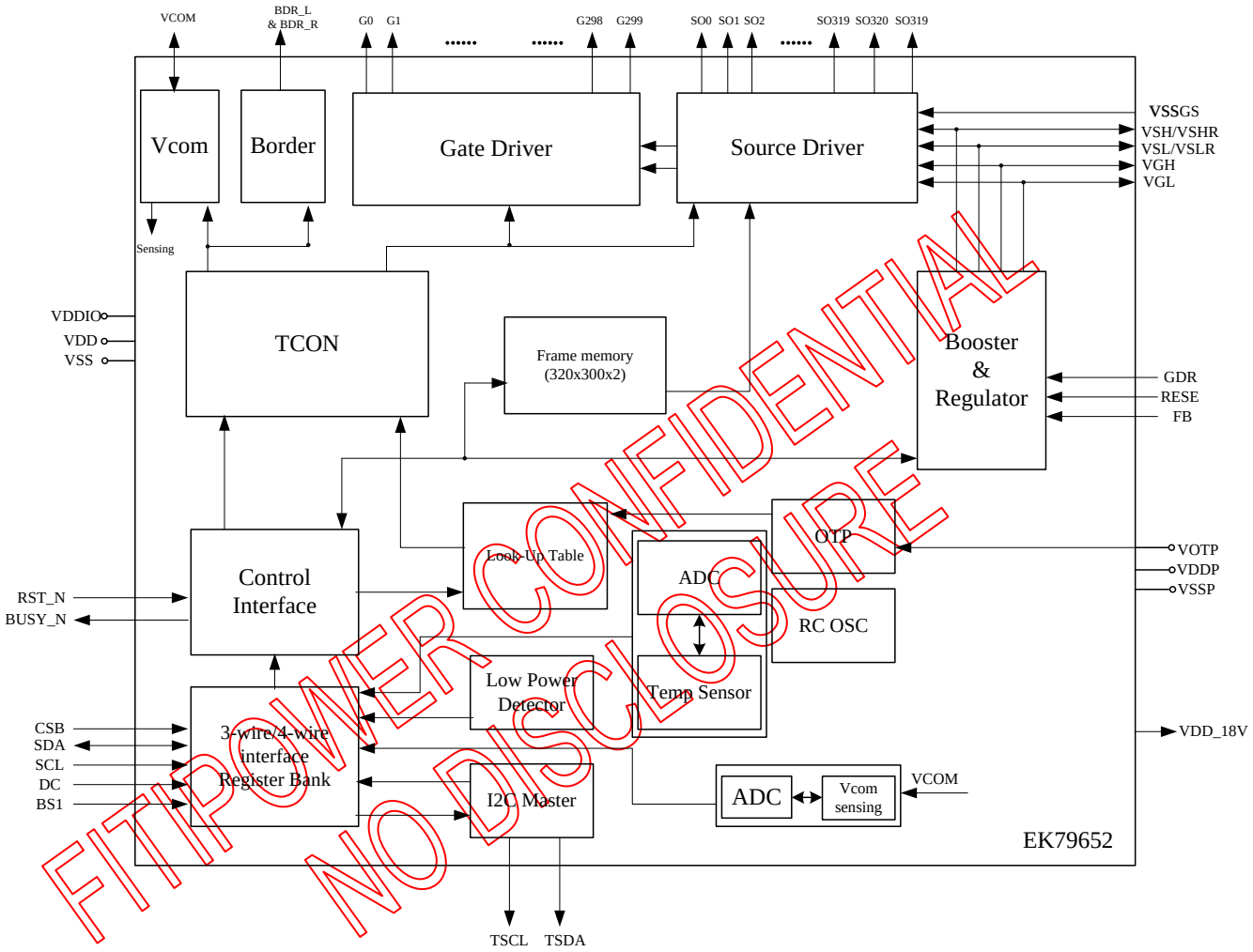
The DC-DC controller allows to generate the source output voltage VSH/VSL (+/-2.4V~+/-11V). The chip also includes an output buffer for the supply of the common electrode (VCOMAC or VCOMDC). The system is configurable through a 3-wire/4-wire (SPI) serial.

2. FEATURES

- System-on-chip (SOC) for color application
- Timing controller support several all resolution (maximum resolution 320x300)
- Support source & gate driver function:
  - 320 Outputs source driver with 1-bit white/black & 1-bit red per pixel:
    - Output dynamic range: VSH (+2.4~+11V)& VSL (-2.4~-11V) (programmable, black/white)
      VSHR: +/-2.4~+/-11V (programmable, red)
    - Output deviation: 0.1V
    - Left and Right shift capability
  - 300 Output gate driver:
    - Output dynamic range: VGH and VGL: +16V, -15V
    - Up and Down shift capability
- Common electrode level
  - AC-VCOM and DC-VCOM
  - Support sensing function (6-bit digital status)
  - Support LUT
- Charge Pump: On-chip booster and regulator
- Built in Frame memory maximum: (320 x 300 x 1 bit) x 2 SRAM
- Built in temperature sensor:
  - On-Chip: On-Chip: -25~50 ^{o}C ± 2.0^{o}C / 8-bit status
  - Off-Chip: -55~125^{o}C ± 2.0^{o}C / 11-bit status (I^2C/LM75)
- Support LPD, Low Power detection (V_{DD}<2.5V)
- OCS : On-chip RC oscillator

- 3-wire/4-wire (SPI) serial interface for system configuration: Clock rate up to 20MHz
- Digital supply voltage: 2.3~3.6V
- Support cascade

3. BLOCK DIAGRAM



4. PIN DESCRIPTION

4.1 Pin define

Pin Name	Pin Type	I/O Structure	Description
Serial Communication Interface			
CSB	I	Type 2	Serial communication chip select.
SDA	I/O	Type 4	Serial communication data input.
SCL	I	Type 3	Serial communication clock input.
DC	I	Type 2	Serial communication Command/Data input L: Command H: data (default)
Control Interface			
RST_N	I	Type 2	Global reset pin. Low reset. **(normal pull high)** When RST_N become low, driver will reset. All register will reset to default value. all driver function will disable. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.
BUSY_N	O	Type1	This pin indicates the driver status. BUSY_N= "0": Driver is busy, data/VCOM is transforming. BUSY_N= "1" : non-busy. Host side can send command/data to driver.
BS	I	Type 5	Input interface setting. Select 3 wire/ 4 wire SPI interface L: 4-wire IF H:3-wire IF(Default)
TSCL	O	Type1	I^2C clock for external temperature sensor
TSDA	I/O	Type 4	I^2C data for external temperature sensor
MS	I	Type 5	Master/Slave selection for cascade mode Low: Slave High: Master In single-chip mode, MS should be connect to VDD
Output Driver			
S[0,319]	O	-	Source driver output signals.
G[0,299]	O	-	Gate driver output signals..
Border			
BDR_L, BDR_R	O	-	Border output pins. It outputs black WF.
VCOM GENERATOR			
VCOM_PASSR / VCOM_PASSL	I /O		VCOM Internal Pass Line
VCOM	O	Type 1	VCOM output. VCOM has follow four voltage state: 1. (VSH-VCM_DC) v 2. (-VCM_DC) v 3. (VSL-VCM_DC) v. 4. Floating
Power Circuit			
GDR	O	-	This pin is N-MOS gate control.
RESE	P	-	Current sense input for control loop.
FB	P	-	Keep open
VGH	P	Type 4	Positive gate voltage
VGL	P	Type 4	Negative gate voltage.

Pin Name	Pin Type	I/O Structure	Description
VSH	P	Type 4	Positive source voltage
VSL	P	Type 4	Negative source voltage.
VSHR	P	Type 4	Positive source voltage for Red
VSLR	P	Type 4	negative source voltage for Red
Power Supply			
VSSP	P	-	DCDC Ground
VDDP	P	-	DCDC power input
VDD	P	-	Digital/Analog power.
VSS	P	-	Digital ground
VSSA	P		Analog Ground
VDDIO	P	-	IO voltage supply
VDD_18V	P	-	1.8V voltage input &output
VOTP	P	-	OTP program power (7.5V)
VSSGS	P		Driver Ground
Reserved Pins			
TP[66:0]	I/O	-	Leave it floating
MS_LR	I	Type 5	Cascade direction 0 : Master(right side output) -> Slave(left side input) 1 : Slave(right side input) <- master(left side output)
VSYNC_R	I/O	Type 4	Cascade right side Vsync
VSYNC_L	I/O	Type 4	Cascade left side Vsync
SYNCM_R	I/O	Type 4	Cascade master right side state sync
SYNCM_L	I/O	Type 4	Cascade master left side state sync
SYNCS_R	I/O	Type 4	Cascade slave right side state sync
SYNCS_L	I/O	Type 4	Cascade slave left side state sync
CLK_L	I/O	Type 4	Cascade left side reference clock pin
CLK_R	I/O	Type 4	Cascade right side reference clock pin
HSYNC_L	I/O	Type 4	Cascade left side system clock pin
HSYNC_R	I/O	Type 4	Cascade right side system clock pin
EN_L	I/O	Type 4	Cascade left side enable pin
EN_R	I/O	Type 4	Cascade right side enable pin
DT_L	I/O	Type 4	Cascade left side data pin for temperature data
DT_R	I/O	Type 4	Cascade right side data pin for temperature data

Note: I: Input, O: Output, P: Power, D: Dummy, S: Shorted line, M: Mark, PI: Power input, PO: Power output, I/O: Input / Output. PS: Power Setting, C: Capacitor pin.

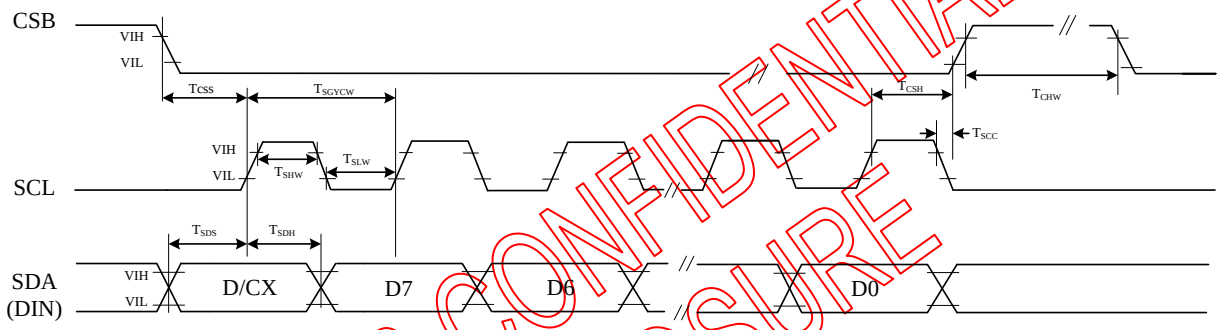
5. SPI COMMAND DESCRIPTION

5.1 “3-Wire” Serial Port Interface

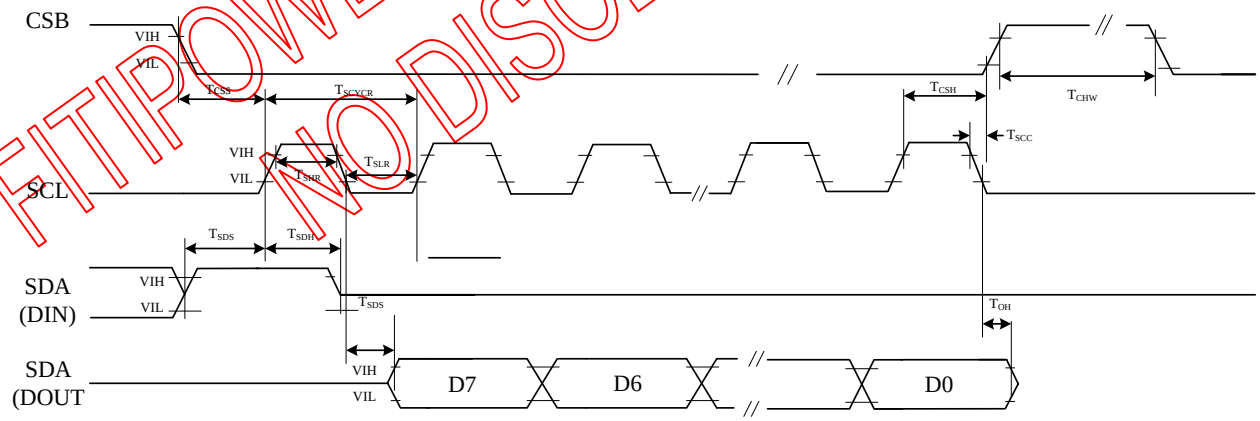
EK79652 use the 3-wire serial port as communication interface for all the function and command setting.

3-Wire communication can be bi-directional controlled by the “R/W” bit in address field. EK79652 3-Wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-Wire bus itself.

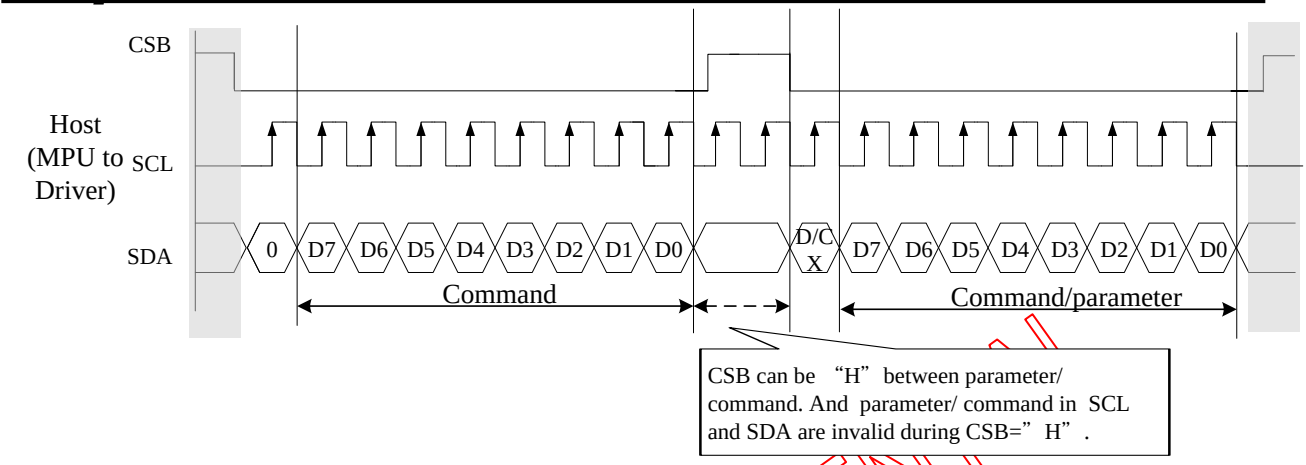
Under read mode, 3-Wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.



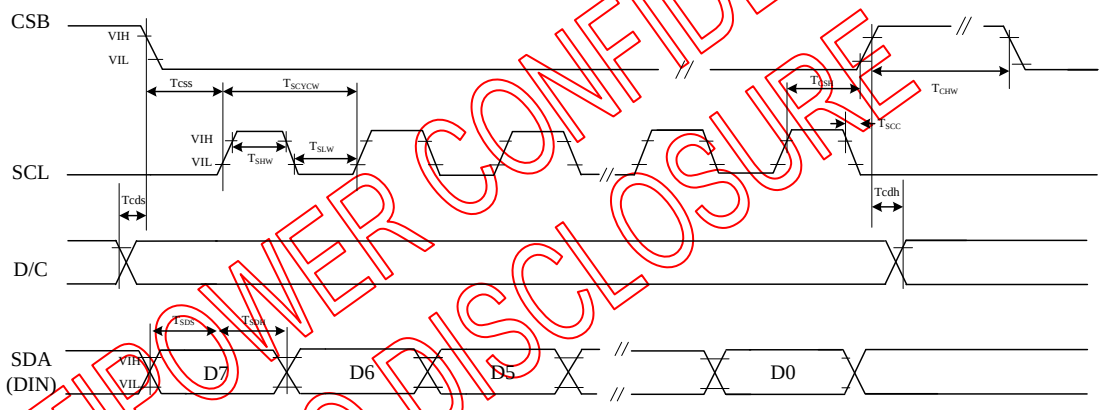
3 pin serial interface characteristics (write mode)



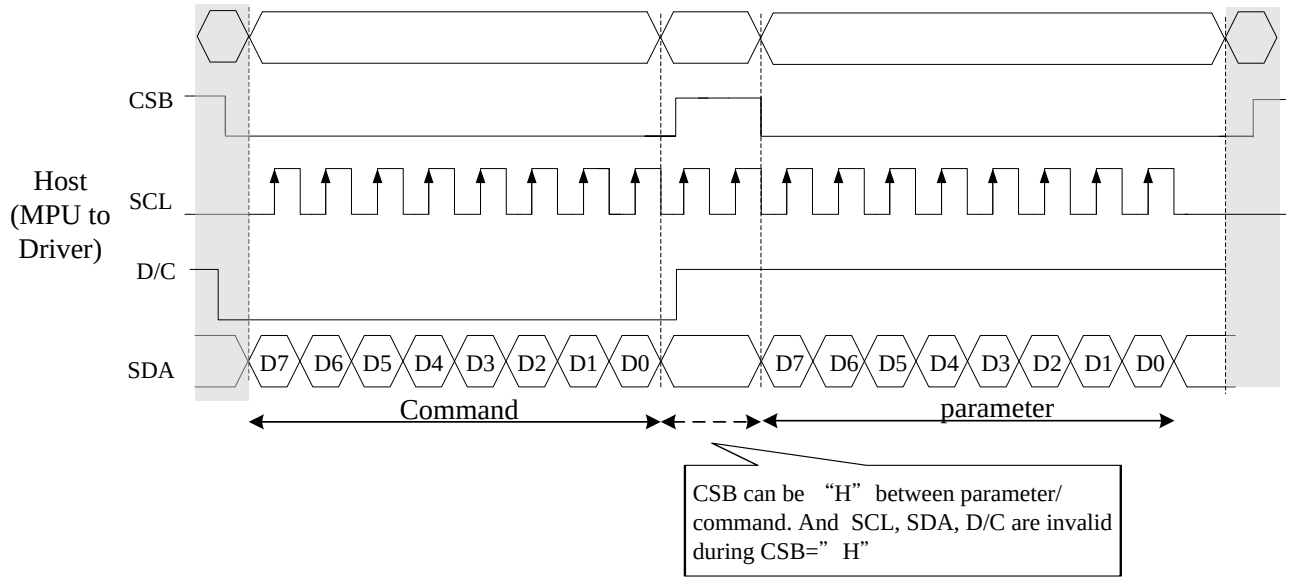
3 pin serial interface characteristics (read mode)



5.2 "4-Wire" Serial Port Interface



4 pin serial interface characteristics



6. SPI CONTROL REGISTERS:

6.1 Register Table

Following table list all the SPI control registers and bit name definition for EK79652. Refer to the next section for detail register function description.

Address	command	Bit										
		R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
R00H	Panel setting (PSR)	W	0	0	0	0	0	0	0	0	0	00H
		W	1	RES[1]	RES[0]	REG_EN	BWR	UD	SHL	SHD_N	RST_N	07h
R01H	Power setting (PWR)	W	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03h
		W	1			-	-	-	VCOM_HV	VGHL_LV [1]	VGHL_LV [0]	00h
		W	1			VSH [5]	VSH [4]	VSH [3]	VSH [2]	VSH [1]	VSH [0]	26h
		W	1			VSL [5]	VSL [4]	VSL [3]	VSL [2]	VSL [1]	VSL [0]	26h
		W	1		VSHR [6]	VSHR [5]	VSHR [4]	VSHR [3]	VSHR [2]	VSHR [1]	VSHR [0]	03h
R02H	Power OFF(POF)	W	0	0	0	0	0	0	0	1	0	02H
R03H	Power off Sequence Setting(PFS)	W	0	0	0	0	0	0	0	1	1	03H
		W	1	-	-	T_VDS_OFF [1]	T_VDS_OFF[0]					00h
R04H	Power ON (PON)	W	0	0	0	0	0	0	1	0	0	04H
R05H	Power ON Measure (PMES)	W	0	0	0	0	0	0	1	0	1	05H
R06H	Booster Soft Start (BTST)	W	0	0	0	0	0	0	0	1	1	06H
		W	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0	03h
		W	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0	00h
		W	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0	26h
R07H	Deep Sleep(DSLP)	W	0	0	0	0	0	0	1	1	1	07H
		W	1	1	0	1	0	0	1	0	1	A5h
R10H	Data Start transmission1 (DTM1)	W	0	0	0	0	1	0	0	0	0	10H
		W	1	#	#	#	#	#	#	#	#	00H
R11H	Data Stop (DSP)	W	0	0	0	0	1	0	0	0	1	11H
		R	1	Data_flag	-	-	-	-	-	-	-	00h
R12H	Display Refresh (DRF)	W	0	0	0	0	1	0	0	0	1	12H
R13H	Data Start transmission 2(DTM2)	W	0	0	0	0	1	0	0	0	0	13H
		W	1	#	#	#	#	#	#	#	#	00H
R30H	OSC control (OSC)	W	0	0	0	1	1	0	0	0	0	30H
		W	1	-	SEL_DIV[1:0]		SEL_F[4:0]					3Ch
R40H	Temperature Sensor Command (TSC)	W	0	0	1	0	0	0	0	0	0	40H
		R	1	D10/TS[7]	D9/TS[6]	D8/TS[5]	D7/TS[4]	D6/TS[3]	D5/TS[2]	D4/TS[1]	D3/TS[0]	
		R	1	D2	D1	D0	-	-	-	-	-	
R41H	Temperature Sensor Calibration (TSE)	W	0	0	1	0	0	0	0	0	1	41H
		W	1	TSE	-	-	-	TO[3]	TO[2]	TO[1]	TO0]	
R42H	Temperature Sensor Write (TSW)	W	0	0	1	0	0	0	0	1	0	42H
		W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
		W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
		W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h
R43H	Temperature Sensor Read (TSR)	W	0	0	1	0	0	0	0	0	1	43H
		W	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	
		W	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	
R50H	VCOM and DATA interval setting (CDI)	W	0	0	1	0	1	0	0	0	0	50H
		W	1	VBD[1]	VBD[0]	DDX[1]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	D7h
R51H	Lower Power Detection (LPD)	W	0	0	1	0	1	0	0	0	1	51H
		R	1	-	-	-	-	-	-	-	LPD	

R60H	TCON setting (TCON)	W	0	0	1	1	0	0	0	0	0	60H
		W	1	S2G[3]	S2G[2]	S2G[1]-	S2G[0]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	22h
R61H	Resolution setting(TRES)	W	0	0	1	1	0	0	0	0	1	61H
		W	1								HRES(8)	00h
		W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	HRES(1)	-	00h
		W	1								VRES(8)	00h
		W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	
R62H	Source & gate start setting	W	0	0	1	1	0	0	0	1	0	
		W	1								S_start [8]	
		W	1	S_start (7)	S_start (6)	S_start (5)	S_start (4)	S_start (3)	S_start (2)	S_start (1)	S_start (0)	
		W	1				gscan				G_start [8]	
		W	1	G_start (7)	G_start (6)	G_start (6)	G_start (4)	G_start (3)	G_start (2)	G_start (1)	G_start (0)	
R70H	REVISION (REV)	W	0	0	1	1	1	0	0	0	0	70H
		R	1	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]	00h
R71H	Status register(FLG)	W	0	0	1	1	1	0	0	0	1	71H
		R	1	-	PTL_flag	I^2C_ERR	I^2C_ BUSYN	Data_flag	PON	POF	BUSY_N	02h
R80H	Auto Measure Vcom (AMV)	W	0	1	0	0	0	0	0	0	0	80 H
		W	1	-	-	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	10h
R81H	Vcom Value (VV)	W	0	1	0	0	0	0	0	0	1	81H
		R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	00h
R82H	Vcom_DC Setting register(VDCS)	W	0	1	0	0	0	0	0	1	0	82H
		W	1	-	VCDS[6]	VCDS[5]	VCDS [4]	VCDS [3]	VCDS [2]	VCDS [1]	VCDS [0]	00h
RE0H	CASCADE setting (CCSET)	W	0	1	1	1	0	0	0	0	0	E0H
		W	1	-	-	-	-	cce_sel	cce_lr	TSFIX	CCEIN	00h
RE5H	Force Temperature	W	0	1	1	1	0	0	1	0	1	E5H
		W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[0]	00h

7. ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Unit
Logic supply voltage	VDD, AVDD,VDDIO, VDD1,VPP	-0.3	+6.0	V
Digital input voltage	VI	-0.3	TBD	V
Supply range	VGH-VGL	VGL-0.3	VGH+0.3	V
Analog supply	VSH	+2.4	+11	V
Analog supply	VSL	-11	-2.4	V
Analog supply	VSHR	-11	+11	
Supply voltage	VGH	-	+16	V
Supply voltage	VGL	-15	-	V
Storage temperature	T_{STG}	-55	125	℃

Note:
Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied.
Exposing device to the absolute maximum ratings in a long period of time may degrade the device and affect its reliability.

7.2 Digital DC Characteristic

DC electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
IO Supply Voltage	VDDIO	2.3	3.3	3.6	V	
Digital/Analog supply voltage	VDD	2.3	3.3	3.6	V	
DCDC power input voltage	AVDD	2.3	3.3	3.6	V	
1.8V output voltage	VDDDO	1.62	1.8	1.98		
1.8V input voltage	VDDD	1.62	1.8	1.98		
OTP program power	VPP	7.25	7.5	7.75		
Digital ground	VSS		0			
DCDC ground	AVSS		0			
Low Level Input Voltage	Vil	GND	-	0.3xVDD	V	Digital input pins
High Level Input Voltage	Vih	0.7xVIO	-	VIO	V	Digital input pins
High Level Output Voltage	Voh	VIO-0.4	-	-	V	Digital output pins; IOH = 400μA
High Level Output Voltage	Vohd	VDD1-0.4	-	-	V	Digital output pins; IOH = 400μA DRVD, DRVU
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	Digital output pins; IOL = -400μA
Input Leakage Current	Iin	-1.0	-	+1.0	uA	Digital input pins, except pull-up, pull-down pin
Pull-up/down impedance	Rin	-	200K		ohm	
Digital Stand-by Current (power off mode)	IstVDD*	-	0	0.1	uA	All stopped
Digital Operating Current	IVDD*	-	0.5	2.0	mA	
IO Stand-by Current (power off mode)	IstVIO*	-	0.4	1.0	uA	All stopped
IO Operating Current	IVIO*	-	-	0.2	mA	No load
DCDC Stand-by Current (power off mode)	IstVDD1*	-	0	0.01	uA	All stopped
DCDC Operating Current	IVDD1*	-	-	0.05	mA	fdcdc=250kHz, No load
DCDC Operating Current	IVDD1*	-	0.5	1.0	mA	fdcdc=250kHz, External cap: PMOS=415pF, NMOS=340pF
Operating temperature	T_{op}	-30	-	85	℃	

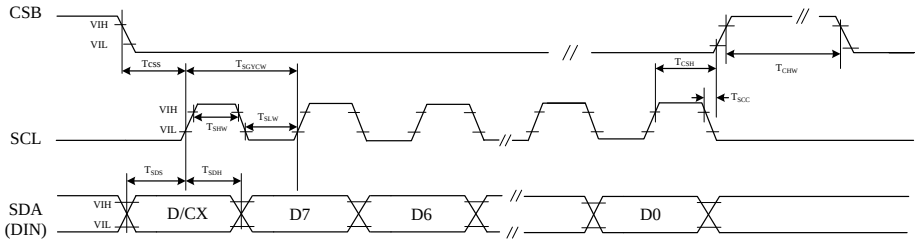
NOTE: typ. and max. values to be confirmed by design

7.3 Analog DC Characteristics

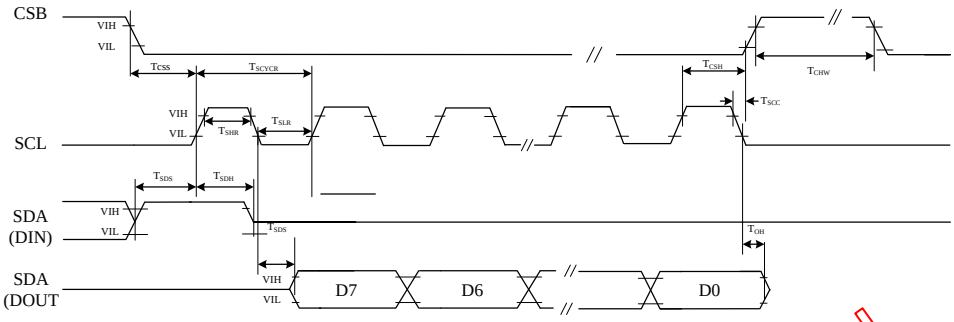
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Positive Source voltage	VSH		10		V	For source driver/VCOM
Positive Source voltage dev	d VSH	-300	0	+300	mV	
Negative Source voltage	VSL		-10		V	For source driver/VCOM
Negative Source voltage dev	d VSL	-300	-	+300	mV	
Positive Source voltage for Red	VSHR					
Negative Source voltage for Red	VSLR					
Analog Operating Current	Idd		TBD		mA	No load,
Voltage Deviation of Outputs	Vvd	-	±20	±35	mV	
Dynamic Range of Output	Vdr	0.1	-	VSH-0.1	V	
Voltage Range of VGH - VGL	VGH-VGL	4.8	-	31	V	
Negative Source voltage	VGL	-15	-	-12	V	For gate driver
Negative Source voltage dev	dVGL	-400	0	+400	mV	
Positive Source voltage	VGH	13		16	V	For gate driver
Positive Source voltage dev	dVGH	-400	0	+400	mA	
Positive HV Stand-by Current (power off mode)	IstVGH*	-	0	0.01	uA	Include VSH power With load
Positive HV Operating Current	IVGH*	-	0.7	1.1	mA	Include VDPS power With load all SD=L VCOM external resistor divider not included
Positive HV Operating Current	IVDPG*	-	0.8	1.2	mA	Include VDPS power With load all SD=H VCOM external resistor divider not included
Negative HV Stand-by Current (power off mode)	IstVDNG*	-	0	0.01	µA	Include VDPNS power With load
Negative HV Operating Current	IVDNG*	-	0.8	1.2	mA	Include VDNS power With load all SD=L
Negative HV Operating Current	IVDNG*	-	0.9-	1.3	mA	Include VDNS power With load all SD=H
VINT1 Stand-by Current (power off mode)	IstVINT1*		0	0.01	µA	
VINT1 Operating Current	IVINT1*			0.3	mA	

7.4 AC Characteristics

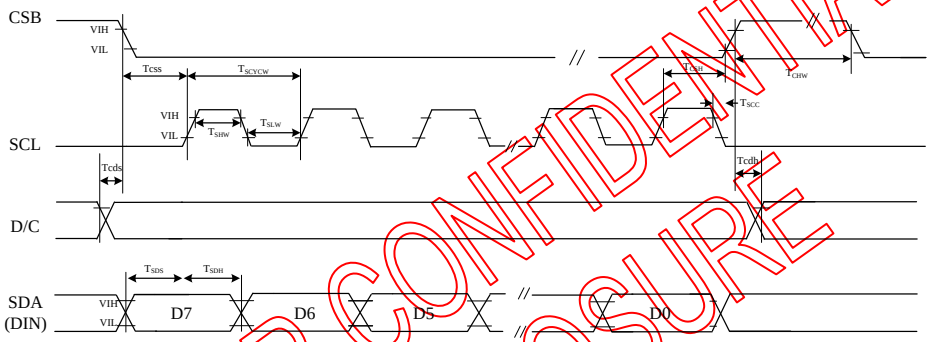
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SERIAL COMMUNICATION						
CSB	tCSS	60			ns	Chip select setup time
	tCSH	65			ns	Chip select hold time
	tSCC	20			ns	Chip select CSB setup time
	tCHW	150			ns	Chip select setup time
SCL	tSCYCW	100			ns	Serial clock cycle (Write)
	TSHW	35	-		ns	SCL “H” pulse width (Write)
	tSLW	35	-		ns	SCL “L” pulse width (Write)
	tSCYCR	150	-		ns	Serial clock cycle (Read)
	TSHR	60			ns	SCL “H” pulse width (Read)
	tSLR	60			ns	SCL “L” pulse width (Read)
SDA (DIN) (DOUT)	tSDS	30			ns	Data setup time
	tSDH	30			ns	Data hold time
	tACC	10			ns	Access time
	tOH	15			ns	Output disable time
D/C	Tcds	20				DC setup time
	Tcdh	20				DC hold time
RC loading						
Source driver output loading	RL_S	-	13.36K		Ω	
	CL_S	-	39.19		pf	
Gate driver output loading	RL_S		12.32K		Ω	
	CL_S		32.09		pf	
VCOM output loading	RL_com		61.26		Ω	
	CL_com		3365.7		pf	
Driver						
Source driver rise time	trS		5		us	99% final value
Source driver fall time	tFS		5		us	
Gate driver rise time	TrG		5		us	99% final value
Gate driver fall time	tFG		5		us	
VCOM rise time	trCOM		1		ms	99% final value
VCOM fall time	tFCOM		1		ms	



3 pin serial interface characteristics (white mode)



3 pin serial interface characteristics (read mode)



4 pin serial interface characteristics

Figure 8: SPI interface timing

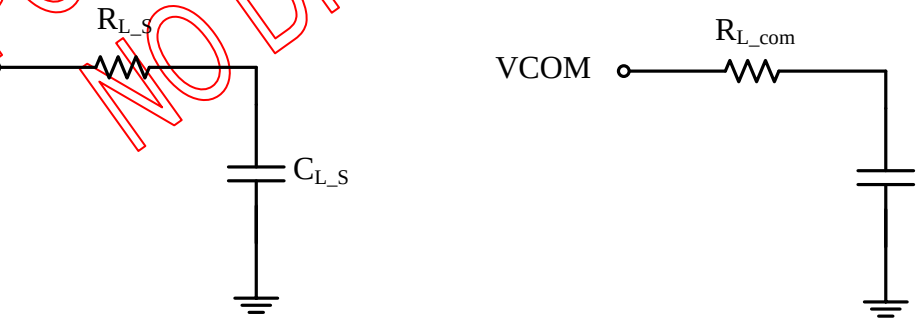


Figure 9: RC loading

8. REVISION HISTORY

Revision	Content	Page	Date
0.1	1.new issue		2015/10/27