



# 11.6 inch E-paper Display Series

**GDEY116Z91**

Dalian Good Display Co., Ltd.

# Product Specifications



<b>Customer</b>	<b>Standard</b>
<b>Description</b>	<b>11.6" E-PAPER DISPLAY</b>
<b>Model Name</b>	<b>GDEY116Z91</b>
<b>Date</b>	<b>2022/12/14</b>
<b>Revision</b>	<b>1.0</b>

	Design Engineering		
	Approval	Check	Design
			

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## 1. Overview

GDEY116Z91 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white, black and red full display capabilities. The 11.60 inch active area contains 960×640 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

## 2.Features

- 960×640 pixels display
- High contrast, high reflectance
- Ultra wide viewing angle, ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform can stored in On-chip OTP or written by MCU
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Sourcedriving voltage
- I<sup>2</sup>C signal master interface to read external temperature sensor
- Built-in temperature sensor

## 3.Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	11.6	Inch	
Display Resolution	960(H)×640(V)	Pixel	Dpi:99
Active Area	244.51×163.01	mm	
Pixel Pitch	0.2547×0.2547	mm	
Pixel Configuration	Rectangle		
Outline Dimension	254.31(H)×176.35(V) ×1.0(D)	mm	
Weight	28.6±0.5	g	

### 4. Mechanical Drawing of EPD module

<i>CUSTOMER'S APPROVED:</i>	<i>DATE:</i>	<i>PAGE:1/1</i>
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NO.	REVISION RECORD	NAME	DATE
4			
3			
2			
1	Initial version	WJZ	2022/04/12

**960\*640 dots**

**Pinout Table:**

PIN NO.	Symbol
1	NC
2	GDR
3	RESE
4	NC
5	VSH2
6	TSCl
7	TSDA
8	BSl
9	BUSY
10	RES#
11	D/C#
12	CS#
13	SCL
14	SDA
15	VDDIO
16	VCl
17	VSS
18	VDD
19	VPP
20	VSH1
21	VGH
22	VSL
23	VGL
24	VCOM

NO.	NAME	DATE
1		
2		
3		
4		

**Dalian Good Display Co., Ltd.**

Unit:mm

Drw  
Chk  
Apv

**REVISION RECORD**

**NAME**

**DATE**

**Display mode** EPD,B/W/R

**Resolution ratio** 11.60",960\*640

**Operating Voltage:** VCl=3.0V

**Operating Temp:** 0°C~40°C

**Storage Temp:** -25°C~70°C

**controller/driver:** SSD1677

**Unspecified tolerance:** ±0.20

**Customer No.:**

**Dimensions with mark "\*" are important**

**RoHS compliant**

## 5. Input /Output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Contro	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	V H2	C	Positive Source driving voltage(Red)	
6	TSCL	O	<sup>2</sup> C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	<sup>2</sup> C Interface to digital temperature sensor Data pin	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES	I	Reset signal input. Active Low.	Note 5-3
11	D/C	I	Data /Command control pin	Note 5-2
12	CS	I	Chip select input pin	Note 5-1
13	SC	I	Serial Clock pin (SPI)	
14	SD	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	V	P	Power Supply for the chip	
17	SS	P	Ground	
18	VD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	PP	P	FOR TEST	
20	VSH1	C	Positive Source driving voltage	
21	VG	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VS	C	Negative Source driving voltage	
23	VG	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output),  
 P = Power Pin, C =Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode.

When the pin is pulled HIGH, the data at SDA will be interpreted as data.

When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when

- Outputting display waveform
- Communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

<b>BS1 State</b>	<b>MCU Interface</b>
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- line serial peripheral interface(SPI) - 9 bits SPI

## 6. Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description						
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting Set A[9:0]=2A7h[POR] ,680MUX Set B[2:0]=000[POR]						
0	1		A7	A6	A5	A4	A3	A2	A1	A0								
0	1		0	0	0	0	0	0	A9	A8								
0	1		0	0	0	0	0	B2	B1	B0								
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage control	SetGate Driving voltage A[4:0]=17h[POR],VGH at 20V[POR] VGH setting from 12V to 20V						
0	1		0	0	0	A4	A3	A2	A1	A0								
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage control	SetSource Driving voltage A[7:0]= 41h[POR],VSH1 at 15V B[7:0]=A8h[POR],VSH2 at 5.0V C[7:0]= 32h[POR], VSL at -15V						
0	1		A7	A6	A5	A4	A3	A2	A1	A0								
0	1		B7	B6	B5	B4	B3	B2	B1	B0								
0	1		C7	C6	C5	C4	C3	C2	C1	C0								
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>A[1:0] :</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>Normal Mode [POR]</td> </tr> <tr> <td>11</td> <td>Enter Deep Sleep Mode</td> </tr> </tbody> </table> After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high.	A[1:0] :	Description	00	Normal Mode [POR]	11	Enter Deep Sleep Mode
A[1:0] :	Description																	
00	Normal Mode [POR]																	
11	Enter Deep Sleep Mode																	
0	1		0	0	0	0	0	0	A <sub>1</sub>	A <sub>0</sub>								
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A [1:0] = ID[1:0]Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.						
0	1		0	0	0	0	0	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>								
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation ,BUSY pad will output high. Note: RAM are unaffected by this command.						



0	0	18	0	0	0	1	1	0	0	0	Temperature Sensor Control	Temperature Sensor Selection A[7:0] = 48h [POR], external temperature sensor A[7:0] = 80h Internal temperature sensor				
0	1		A7	A6	A5	A4	A3	A2	A1	A0						
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[11:0]=7FFh[POR]				
0	1		A11	A10	A9	A8	A7	A6	A5	A4						
0	1		A3	A2	A1	A0	0	0	0	0						
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h User should not interrupt this operation to avoid corruption of panel images.				
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update A[7:0]=00h[POR] A[7:4] Red RAM option 0000 Normal 0100 Bypass RAM content as 0 1000 Inverse RAM content  A[3:0] BW RAM option 0000 Normal 0100 Bypass RAM content as 0 1000 Inverse RAM content				
0	1		A7	A6	A5	A4	A3	A2	A1	A0						
0	0	22	0	0	1	0	0	0	1	0			Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation <b>Setting for LUT from MCU</b> Enable Clock Signal, Then Enable Analog Then PATTERN DISPLAY C7 Then Disable Analog Then Disable OSC <b>Setting for LUT from OTP according to external Temperature Sensor operation</b> Then Enable Analog Then Load LUT 90  Enable Analog Then PATTERN DISPLAY 47 Then Disable Analog Then Disable OSC		
	1		A7	A6	A5	A4	A3	A2	A1	A0						
0	0	24	0	0	1	0	0	1	0	0					Write RAM (BW)	After this command, data entries will be written into the 1RAM until another command is written. Address pointers will advance accordingly. For Write pixel: Content of write RAM(BW)=1 For Black pixel: Content of write RAM(BW)=0
0	1		A7	A6	A5	A4	A3	A2	A1	A0						

0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED)	After this command, data entries will be written into the 2 RAM until another command is written. Address pointers will advance accordingly. For RED pixel: Content of write RAM(RED)=1 For White/Black pixel: Content of write RAM(RED)=0
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Set A[7:0]=50h
0	1		A7	A6	A5	A4	A3	A2	A1	A0	OTP Register Read	Read Register stored in OTP: 1. A[7:0]~ B[7:0]: VCOM Information 2. C[7:0]~G[7:0]:Display mode 3. H[7:0]~K[7:0]: Waveform Version [4bytes]
0	0	2D	0	0	1	0	1	1	0	1		
1	1		A7	A6	A5	A4	A3	A2	A1	A0		
1	1		B7	B6	B5	B4	B3	B2	B1	B0		
1	1		C7	C6	C5	C4	C3	C2	C1	C0		
1	1		D7	D6	D5	D4	D3	D2	D1	D0		
1	1		E7	E6	E5	E4	E3	E2	E1	E0		
1	1		F7	F6	F5	F4	F3	F2	F1	F0		
1	1		G7	G6	G5	G4	G3	G2	G1	G0		
1	1		H7	H6	H5	H4	H3	H2	H1	H0		
1	1		I7	I6	I5	I4	I3	I2	I1	I0		
1	1		J7	J6	J5	J4	J3	J2	J1	J0		
1	1		K7	K6	K5	K4	K3	K2	K1	K0		
0	0	2F	0	0	1	0	1	1	1	1		
1	1		0	0	A5	A4	0	0	A1	A0		
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [105 bytes].
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		B7	B6	B5	B4	B3	B2	B1	B0		
0	1		:	:	:	:	:	:	:	:		
0	1		:	:	:	:	:	:	:	:		
0	1		:	:	:	:	:	:	:	:		

0	0	3A	0	0	1	1	1	0	1	0	Reserved	Reserved																																		
0	0	3B	0	0	1	1	1	0	1	1	Reserved	Reserved																																		
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A [7:0]=C0h[POR],set VBD as HIZ A [7:6] Select VBD option																																		
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	0	0	A <sub>1</sub>	A <sub>0</sub>		<table border="1"> <tr> <td>A[7:6]</td><td>Select VBD as</td></tr> <tr> <td>00</td><td>GS Transition Define A[1:0]</td></tr> <tr> <td>01</td><td>Fix Level Define A [5:4]</td></tr> <tr> <td>10</td><td>VCOM</td></tr> <tr> <td>11[POR]</td><td>HIZ</td></tr> <tr> <td colspan="2">A [5:4] Fix Level Setting for VBD</td></tr> <tr> <td>A[5:4]</td><td>VBD level</td></tr> <tr> <td>00[POR]</td><td>VSS</td></tr> <tr> <td>01</td><td>VSH1</td></tr> <tr> <td>10</td><td>VSL</td></tr> <tr> <td>11</td><td>VSH2</td></tr> <tr> <td colspan="2">A[1:0] BW Transition setting for VBD</td></tr> <tr> <td>A[1:0]</td><td>VBD Transition</td></tr> <tr> <td>00 [POR]</td><td>LUT0</td></tr> <tr> <td>01</td><td>LUT1</td></tr> <tr> <td>10</td><td>LUT2</td></tr> <tr> <td>11</td><td>LUT3</td></tr> </table>	A[7:6]	Select VBD as	00	GS Transition Define A[1:0]	01	Fix Level Define A [5:4]	10	VCOM	11[POR]	HIZ	A [5:4] Fix Level Setting for VBD		A[5:4]	VBD level	00[POR]	VSS	01	VSH1	10	VSL	11	VSH2	A[1:0] BW Transition setting for VBD		A[1:0]	VBD Transition	00 [POR]	LUT0	01	LUT1	10	LUT2	11	LUT3
A[7:6]	Select VBD as																																													
00	GS Transition Define A[1:0]																																													
01	Fix Level Define A [5:4]																																													
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00 [POR]	LUT0																																													
01	LUT1																																													
10	LUT2																																													
11	LUT3																																													
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit A[9:0]: XSA[9:0], X Start, POR = 000h B[9:0]: XEA[9:0], X End, POR = 3BFh																																		
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>																																				
0	1		-	-	-	-	-	-	A <sub>9</sub>	A <sub>8</sub>																																				
0	1		B <sub>7</sub>	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>																																				
0	1		-	-	-	-	-	-	B <sub>9</sub>	B <sub>8</sub>																																				
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y-address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[9:0]: YSA[9:0], Y Start, POR = 000h B[9:0]: YEA[9:0], Y End, POR = 2A7h																																		
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>																																				
0	1		-	-	-	-	-	-	A <sub>9</sub>	A <sub>8</sub>																																				
0	1		B <sub>7</sub>	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>																																				
0	1		-	-	-	-	-	-	B <sub>9</sub>	B <sub>8</sub>																																				
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[9:0]: 000h[POR]																																		
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>																																				
0	1		-	-	-	-	-	-	A <sub>9</sub>	A <sub>8</sub>																																				
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[9:0]: 000h[POR]																																		
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>																																				
0	1		-	-	-	-	-	-	A <sub>9</sub>	A <sub>8</sub>																																				
0	1		A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>																																				

## 7. Electrical Characteristics

### 7.1. Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	V <sub>CI</sub>	-0.5 to +4.0	V
Logic Input voltage	V <sub>IN</sub>	-0.5 to V <sub>DDIO</sub> +0.5	V
Logic Output voltage	V <sub>OUT</sub>	-0.5 to V <sub>DDIO</sub> +0.5	V
Operating Temp range	TOPR	0 to +40	°C
Storage Temp range	TSTG	-25 to +70	°C
Optimal Storage Temp	TSTGo	23±2	°C
Optimal Storage Humidity	HSTGo	55±10	%RH

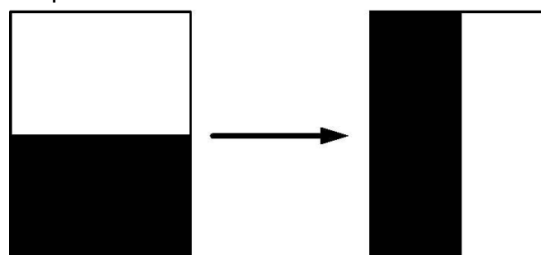
Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section.

### 7.2. Panel DC Characteristics

The following specifications apply for: V<sub>SS</sub>=0V, V<sub>CI</sub>=3.0V, TOPR =25°C

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V <sub>SS</sub>	-		-	0	-	V
Logic supply voltage	V <sub>CI</sub>	-	V <sub>CI</sub>	2.2	3.0	3.3	V
Core logic voltage	V <sub>DD</sub>		V <sub>DD</sub>	1.7	1.8	1.9	V
High level input voltage	V <sub>IH</sub>	-	-	0.8 V <sub>DDIO</sub>	-	-	V
Low level input voltage	V <sub>IL</sub>	-	-	-	-	0.2 V <sub>DDIO</sub>	V
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -100uA	-	0.9 V <sub>DDIO</sub>	-	-	V
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 100uA	-	-	-	0.1V <sub>DDIO</sub>	V
Typical power	P <sub>TYP</sub>	V <sub>CI</sub> =3.0V	-	-	82.5	-	mW
Deep sleep mode	P <sub>STPY</sub>	V <sub>CI</sub> =3.0V	-	-	0.003	-	mW
Typical operating current	I <sub>opr_VCI</sub>	V <sub>CI</sub> =3.0V	-	-	25	-	mA
Image update time	-	25 °C	-	-	28	-	sec
Sleep mode current	I <sub>slp_VCI</sub>	DC/DC off No clock No input load Ram data retain	-	-	25		uA
Deep sleep mode current	I <sub>dsip_VCI</sub>	DC/DC off No clock No input load Ram data not retain	-	-	1	5	uA

Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.



- 2.The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
- 3.The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display.

### 7.3. Panel AC Characteristics

#### 7.3.1. MCU Interface

It support 4-wire or 3-wire serial peripheral MCU interface, which is pin selectable by BS1 pin.The interface pin assignment for different MCU interfaces is shown in Table 7-1.

MCU Interface	Pin Name						
	BS1	RES#	CS#	D/C#	SCL	SDI	SDO
4-wire serial peripheral interface (SPI)	L	RES#	CS#	DC#	SCL	SDA	
3-wire serial peripheral interface (SPI) – 9 bits SPI	H	RES#	CS#	L	SCL	SDA	

**Note:**

- (1) L is connected to V<sub>SS</sub> and H is connected to V<sub>DDIO</sub>
- (2) SDI and SDO are connected to be SDA pin for bi-directional data access

#### 7.3.2. MCU Serial Interface (4-wire SPI)

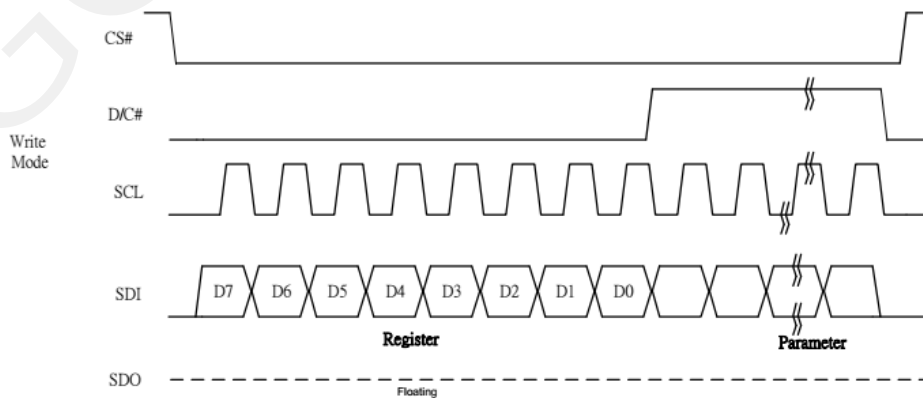
The 4-wire SPI consists of serial clock SCL, serial data input SDI, D/C# and CS#. The control pins status in 4-wire SPI in writing command/data is shown in Table 7-2 and the write procedure in 4-wire SPI is shown in Figure 7-1.

Function	SCL pin	SDI pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

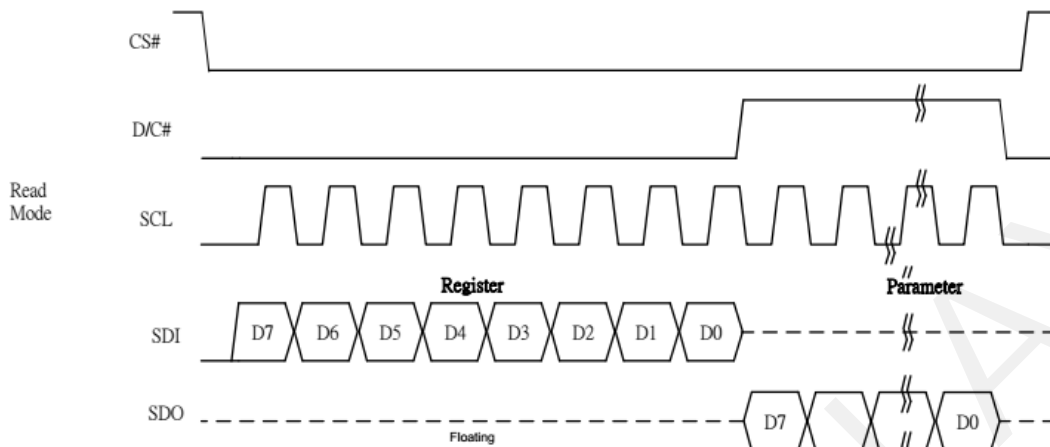
**Note:**

- (1) L is connected to V<sub>SS</sub> and H is connected to V<sub>DDIO</sub>
- (2) ↑ stands for rising edge of signal

SDI is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.



In the read operation, after CS# is pulled low, the first byte sent is command byte, D/C# is pulled low. After command byte sent, the following byte(s) read are data byte(s), so D/C# bit is then pulled high. An 8-bit data will be shifted out on every clock falling edge. The serial data output SDO bit shifting sequence is D7, D6, to D0 bit. Figure shows the read procedure in 4-wire SPI.



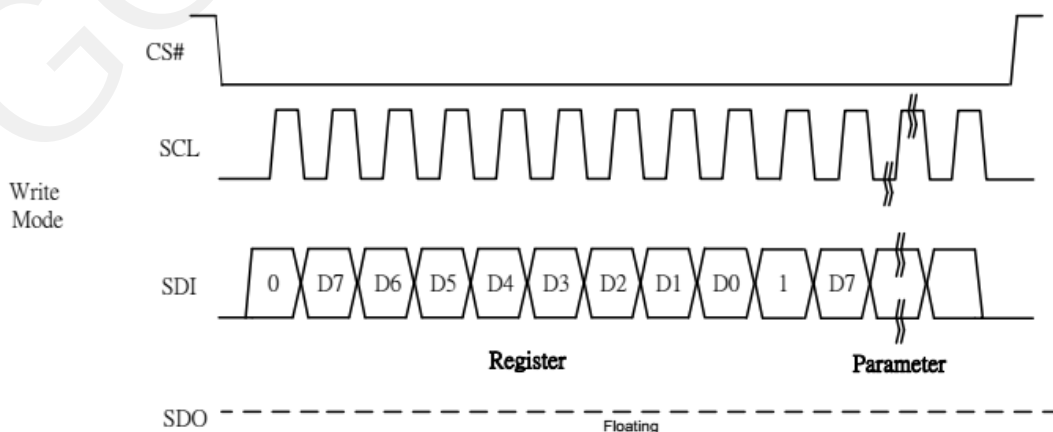
### 7.3.3. MCU Serial Interface(3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data input SDI, and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 7-3. In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Table 7-3 shows the write procedure in 3-wire SPI

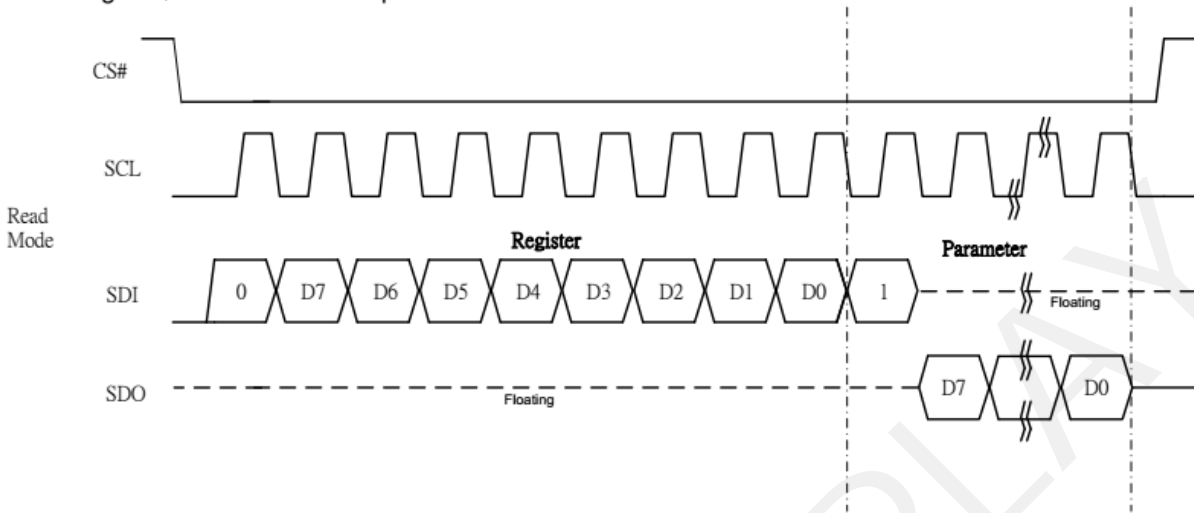
Function	SCL pin	SDI pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

**Note:**

- (1) L is connected to V<sub>SS</sub> and H is connected to V<sub>DDIO</sub>
- (2) ↑ stands for rising edge of signal



In the read operation, serial data are transferred in the unit of 9 bits. After CS# pull low, the first byte is command byte, the D/C# bit is as 0 and following with the register byte. After command byte send, the following byte(s) are data byte(s), with D/C# bit is 1. After D/C# bit sending from MCU, an 8-bit data will be shifted out on every clock falling edge. The serial data output SDO bit shifting sequence is D7, D6, to D0 bit. Figure 7-4 shows the read procedure in 3-wire SPI.



### 7.3.4. Interface Timing

The following specifications apply for: VDDIO - VSS = 2.2V to 3.7V, CL=30pF

#### Serial Peripheral Interface Timing Characteristics

##### Write mode

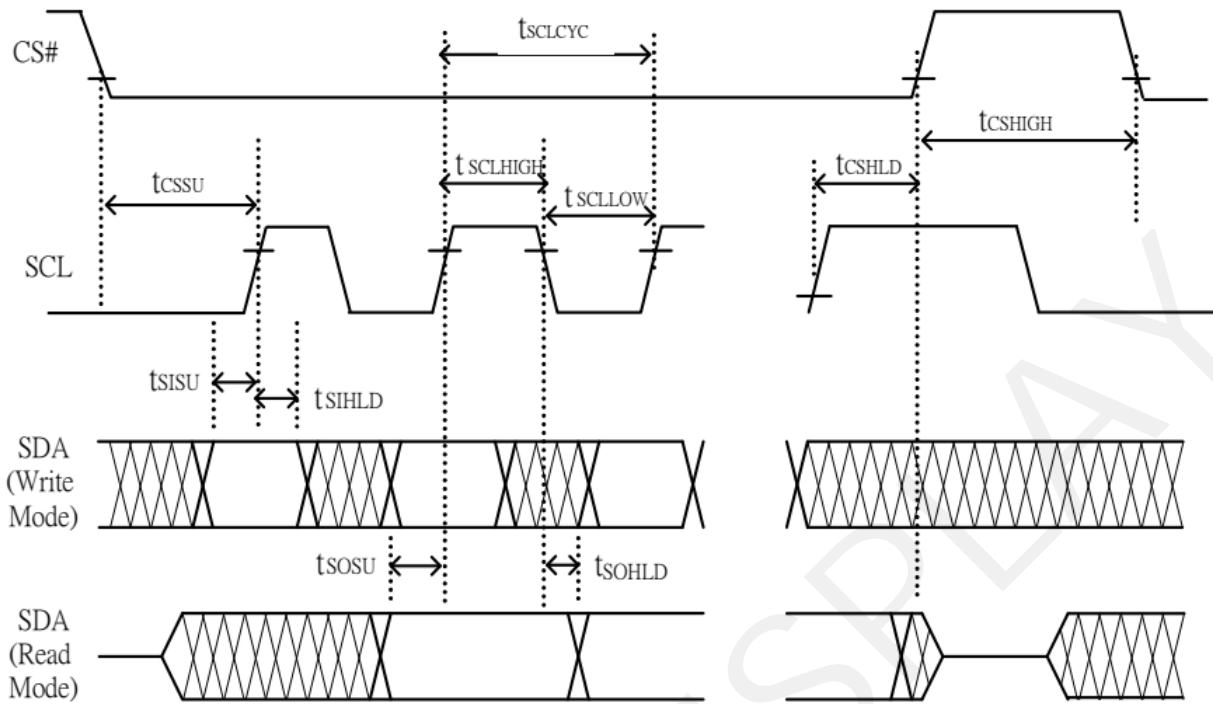
Symbol	Parameter	Min	Typ	Max	Unit
f <sub>SCL</sub>	SCL frequency (Write Mode)			20	MHz
t <sub>CSSU</sub>	Time CS# has to be low before the first rising edge of SCLK	20			ns
t <sub>CSHLD</sub>	Time CS# has to remain low after the last falling edge of SCLK	20			ns
t <sub>CSHIGH</sub>	Time CS# has to remain high between two transfers	100			ns
t <sub>SCLCYC</sub>	SCL cycle time	50			ns
t <sub>SCLHIGH</sub>	Part of the clock period where SCL has to remain high	25			ns
t <sub>SCLLOW</sub>	Part of the clock period where SCL has to remain low	25			ns
t <sub>SISU</sub>	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
t <sub>SIHLD</sub>	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

##### Read mode

Symbol	Parameter	Min	Typ	Max	Unit
f <sub>SCL</sub>	SCL frequency (Read Mode)			2.5	MHz
t <sub>CSSU</sub>	Time CS# has to be low before the first rising edge of SCLK	100			ns
t <sub>CSHLD</sub>	Time CS# has to remain low after the last falling edge of SCLK	50			ns
t <sub>CSHIGH</sub>	Time CS# has to remain high between two transfers	250			ns
t <sub>SCLHIGH</sub>	Part of the clock period where SCL has to remain high	180			ns
t <sub>SCLLOW</sub>	Part of the clock period where SCL has to remain low	180			ns
t <sub>SOSU</sub>	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
t <sub>SOHLD</sub>	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

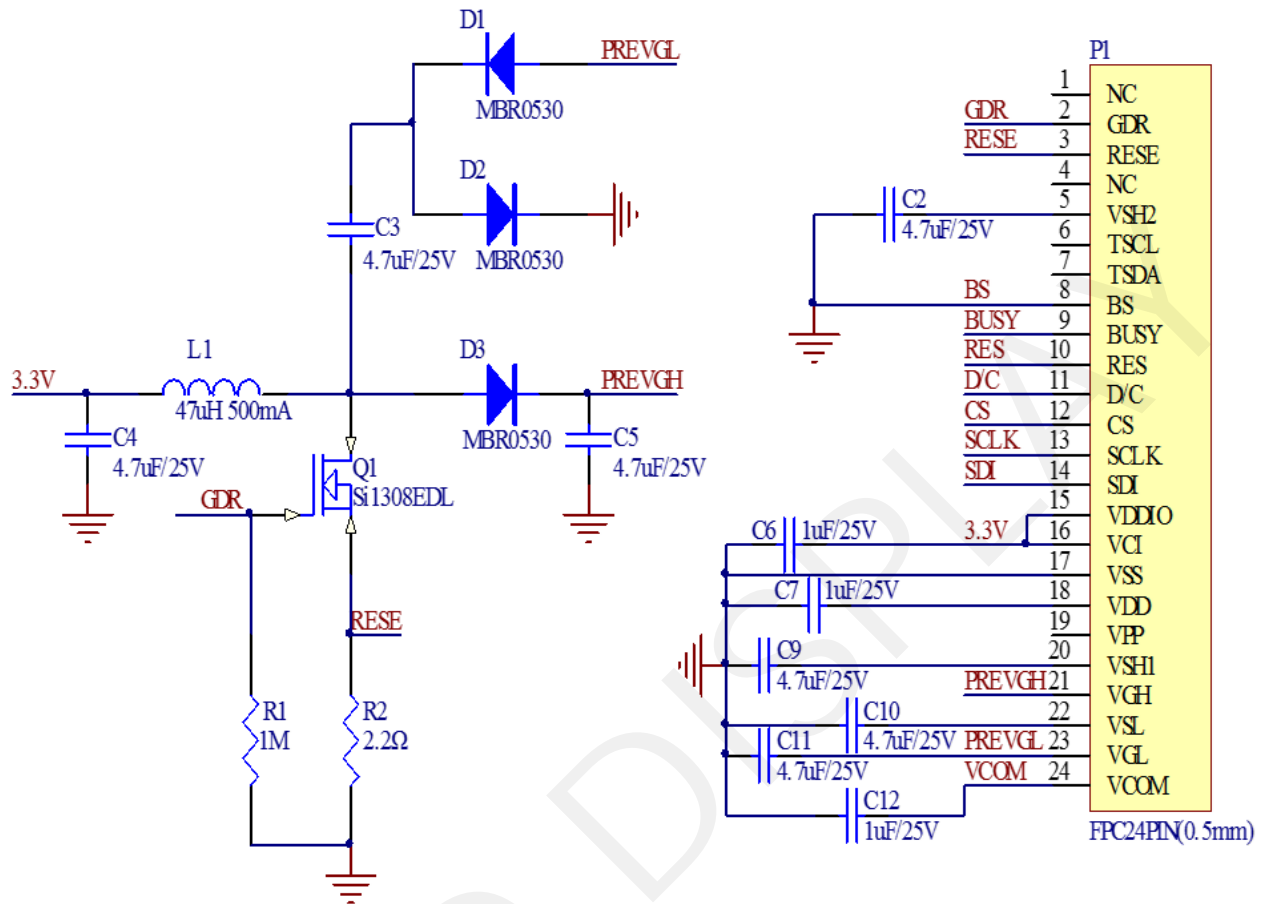
Note: All timings are based on 20% to 80% of VDDIO-VSS

SPI timing diagram





### 7.4 Reference Circuit



## 8. Optical Specifications

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contras Ratio	Indoor	8:1		-		8-2
GN	2Gr Level	-		$DS+(WS-DS)*n(m-1)$			8-3
T update	Image update time	at 25 °C		28	-	sec	
Life		Topr		1000000times or 5years			

Notes:

8-1. Luminance meter: Eye-One Pro Spectrophotometer.

8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

8-3. WS: White state, DS: Dark state

## 9. Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display and three-color (black, white and red/Yellow) Good Display 's E-paper Display. And it is also added the functions of USB serial port, Raspberry Pi and LED indicator light ect.

DESPI Development Kit consists of the development board and the pinboard.

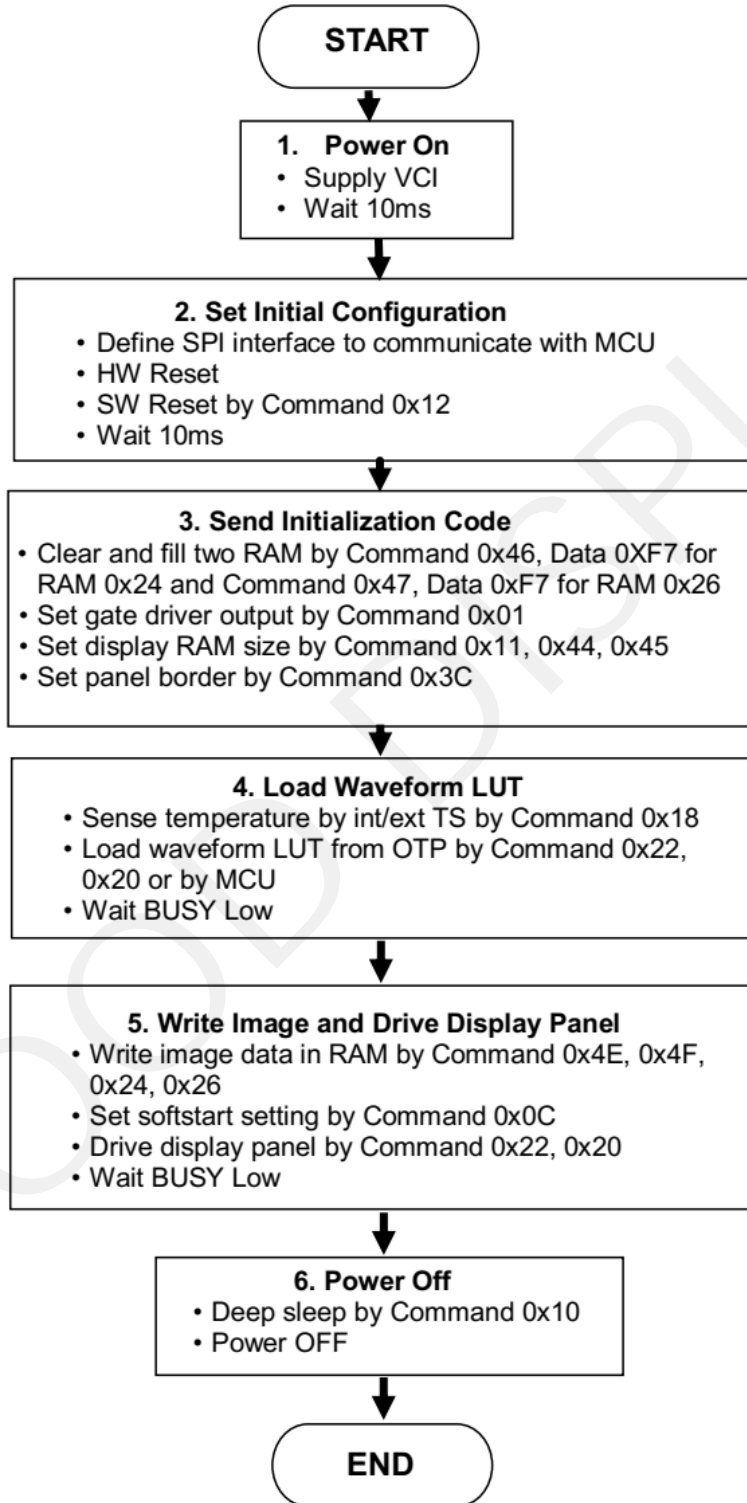
More details about the Development Kit, please click to the following link:

<https://www.good-display.com/product/53/>

GOOD DISPLAY

## 10. Typical Operating Sequence

### 10.1 Normal Operation Flow



## 11. Reliability Test

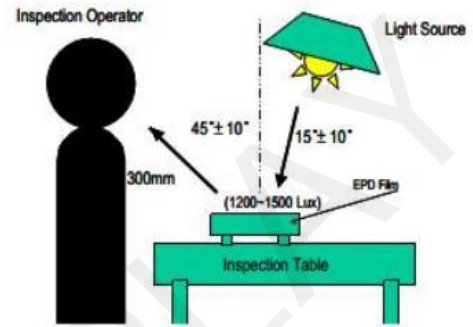
NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=70°C, RH=40%, 240h Test in white pattern
3	High-Temperature Operation	T=40°C, RH=35%, 240h
4	Low-Temperature Operation	0°C, 240h
5	High-Temperature, High-Humidity Operation	T=40°C, RH=80%, 168h
6	High Temperature, High Humidity Storage	T=50°C, RH=80%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min]→[+70 °C 30 min] : 50 cycles Test in white pattern
8	UV exposure Resistance	765W/m <sup>2</sup> for 168hrs,40 °C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell,not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display,no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display,including IC and FPC area)

Note: Put in normal temperature for 1hour after test finished, display performance is ok.

## 12. Inspection method and condition

### 12.1. Inspection condition

Item	Condition
Illuminance	$\geq 1000$ lux
Temperature	$22^{\circ}\text{C} \pm 3^{\circ}\text{C}$
Humidity	45-65 % RoHS
Distance	$\geq 30\text{cm}$
Angle	$\pm 45^{\circ}$
Inspection method	By eyes

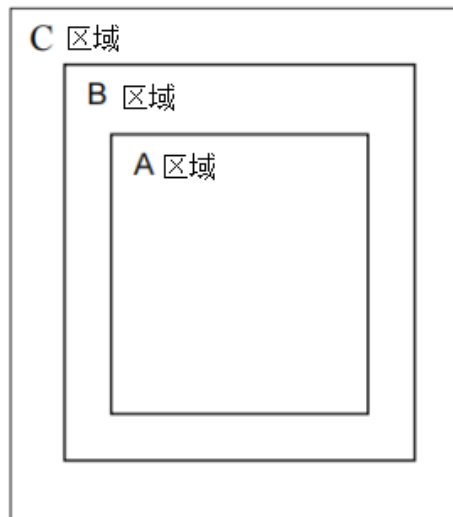


### 12.2 Display area

#### 12.2.1 Zone definition:

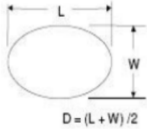
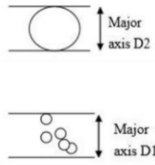
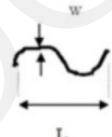
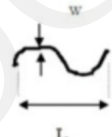
- A Zone: Active area
- B Zone: Border zone
- C Zone: From B zone edge to panel edge

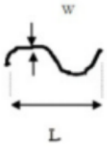
基板边缘

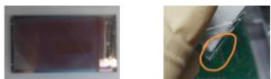

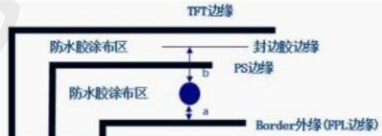


## 12.3 General inspection standards for products

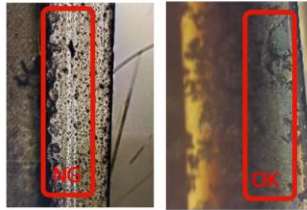


### 12.3.1 Appearance inspection standard

Inspection item		Figure		A zone inspection standard	B/C zone	Inspection method	MAJ/ MIN
Spot defects	Spot defects such as dot, foreign matter, air bubble, and dent etc.	Diameter $D=(L+W)/2$ (L-length, W-width) Measuring method shown in the figure below 	A spec module  The distance between the two spots should not be less than 10mm	7.5"-13.3"Module (Not include 7.5") : $D > 1\text{mm}$ N=0 $0.5 < D \leq 0.8$ $N \leq 4$ $D \leq 0.5$ Ignore $0.8 < D \leq 1$ $N \leq 2$  4.2"-7.5"Module (Not include 4.2") : $D > 0.5$ N=0 $0.4 < D \leq 0.5$ $N \leq 2$ $D \leq 0.25$ Ignore $0.25 < D \leq 0.4$ $N \leq 4$  Module below 4.2": $D > 0.5$ N=0 $0.4 < D \leq 0.5$ $N \leq 1$ $D \leq 0.25$ Ignore $0.25 < D \leq 0.4$ $N \leq 4$ $0.1\text{mm} < D \leq 0.25$ $N \leq 3/\text{cm}^2$	Foreign matter  D≤1mm Pass	Check by eyes  Film gauge	MIN
			B spec module  The distance between the two spots should not be less than 5mm (Outside the AA area, ignore if not serious when checking by eyes)	No affect on display			
Inspection item		Figure		A zone inspection standard	B/C zone	Inspection method	MAJ/ MIN
Line defects	Line defects such as scratch, hair etc.	L-Length, W-Width, $(W/L) < 1/4$ Judged by line,  $(W/L) \geq 1/4$ Judged by dot 	A spec module  The distance between the two lines should not be less than 5mm	7.5"-13.3"Module (Not include 7.5") : $L > 10\text{mm}, N=0$ $W > 0.8\text{mm}, N=0$ $5\text{mm} \leq L \leq 10\text{mm}, 0.5\text{mm} \leq W \leq 0.8\text{mm}$ $N \leq 2$ $L \leq 5\text{mm}, W \leq 0.5\text{mm}$ Ignore  4.2"-7.5"Module (Not include 4.2") : $L > 8\text{mm}, N=0$ $W > 0.2\text{mm}, N=0$ $2\text{mm} \leq L \leq 8\text{mm}, 0.1\text{mm} \leq W \leq 0.2\text{mm}$ $N \leq 4$ $L \leq 2\text{mm}, W \leq 0.1\text{mm}$ Ignore  Module below 4.2": $L > 5\text{mm}, N=0$ $W > 0.2\text{mm}, N=0$ $2\text{mm} \leq L \leq 5\text{mm}, 0.1\text{mm} \leq W \leq 0.2\text{mm}$ $N \leq 4$ $L \leq 2\text{mm}, W \leq 0.1\text{mm}$ Ignore	Ignore	Check by eyes  Film gauge	MIN
			B spec module  The distance between the two lines should not be less than 5mm (Outside the AA area, ignore if not serious when checking by eyes)	No affect on display			

Inspection item		Figure		A zone inspection standard	B/C zone	Inspection method	MAJ/MI/N
Line defects	Line defects such as scratch, hair etc.	L-Length, W-Width, (W/L)<1/4 Judged by line, (W/L)≥1/4 Judged by dot 	A spec module The distance between the two lines should not be less than 5mm	7.5"-13.3"Module (Not include 7.5") : L>10mm,N=0 W>0.8mm, N=0 5mm≤L≤10mm, 0.5mm≤W≤0.8mm N≤2 L≤5mm, W≤0.5mm Ignore 4.2"-7.5"Module (Not include 4.2") : L>8mm,N=0 W>0.2mm, N=0 2mm≤L≤8mm, 0.1mm≤W≤0.2mm N≤4 L≤2mm, W≤0.1mm Ignore Module below 4.2": L>5mm,N=0 W>0.2mm, N=0 2mm≤L≤5mm, 0.1mm≤W≤0.2mm N≤4 L≤2mm, W≤0.1mm Ignore	Ignore	Check by eyes Film gauge	MIN
			B spec module The distance between the two lines should not be less than 5mm (Outside the AA area, ignore if not serious when checking by eyes)	No affect on display			

Inspection item		Figure	Inspection standard	Inspection method	MAJ/MI/N
PS defect	Water proof film		1. Waterproof film damage, wrinkled, open edge, not allowed 2. Exceeding the edge of module(according to the lamination drawing) Not allowed 3. Edge warped exceeds height of technical file, not allowed	Check by eyes	MIN
RTV defect	Adhesive effect		Adhesive height exceeds the display surface, not allowed	Check by eyes	MIN
	Adhesive re-fill		1. Overflow, exceeds the panel side edge, affecting the size, not allowed 2. No adhesive at panel edge≤1mm, no exposure of wiring, allowed 3. No adhesive at edge and corner1*1mm, no exposure of wiring, allowed Protection adhesive, coverage width within W≤1.5mm, no break of adhesive, allowed		
EC defect	Adhesive bubble		1、 Effective edge sealing area of hot melt products ≥1/2 edge sealing area; 2、 Bubble a+b/2≥1/2 effective width, N≤3, spacing≥5mm, allowed No exposure of wiring, allowed	Check by eyes	MIN



Inspection item		Figure	Inspection standard	Inspection method	MAJ/MIN
EC defect	Adhesive effect		1. Overflow, exceeds the panel side edge, affecting the size, not allowed 2. No adhesive at panel edge $\leq 1\text{mm}$ , no exposure of wiring, allowed 3. No adhesive at edge and corner $1*1\text{mm}$ , no exposure of wiring, allowed 4. Adhesive height exceeds the display surface, not allowed	Visual, caliper	MIN
Silver dot adhesive defect	Silver dot adhesive		1. Single silver dot dispensing amount $\geq 1\text{mm}$ , allowed 2. One of the double silver dot dispensing amount is $\geq 1\text{mm}$ and the other has adhesive (no reference to $1\text{mm}$ ) Allowed	Visual	MIN
			Silver dot dispensing residue on the panel $\leq 0.2\text{mm}$ , allowed	Film gauge	MIN
FPC defect	FPC wiring		FPC, TCP damage / gold finger peroxidation, adhesive residue, not allowed	Visual	MIJ
	FPC golden finger		The height of burr edge of TCP punching surface $\cong 0.4\text{mm}$ , not allowed	Caliper	MIN
	FPC damage/cr ease		Damage and breaking, not allowed Crease does not affect the electrical performance display, allowed	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/MIN
Protective film defect	Protective film		Scratch and crease on the surface but no affect to protection function, allowed	Check by eyes	MIN
			Adhesive at edge $L \leq 5\text{mm}$ , $W \leq 0.5\text{mm}$ , $N=2$ , no entering into viewing area	Check by eyes	MIN
Stain defect	Stain		If stain can be normally wiped clean by $> 99\%$ alcohol, allowed	Visual	MIN
Pull tab defect	Pull tab		The position and direction meet the document requirements, and ensure that the protective film can be pulled off.	Check by eyes/ Manual pulling	MIN
Shading tape defect	Shading tape		Tilt $\leq 10^\circ$ , flat without warping, completely covering the IC.	Check by eyes/ Film gauge	MIN
Stiffener	Stiffener		Flat without warping, Exceeding the left and right edges of the FPC is not allowed. Left and right can be less than $0.5\text{mm}$ from FPC edge	Check by eyes	MIN
Label	Label/ Spraying code		The content meets the requirements of the work sheet. The attaching position meets the requirements of the technical documents.	Check by eyes	MIN

Remarks: The definition of other appearance B spec products, no affect to the display, and no entering into the viewing area.

### 13. Handling, Safety and Environmental Requirements

<b>WARNING</b>
<p>The display glass may break when it is dropped or bumped on a hard surface. Handle with care.</p> <p>Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.</p>

<b>CAUTION</b>
<p>The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.</p>
<p>Disassembling the display module can cause permanent damage and invalidate the warranty agreements.</p>

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

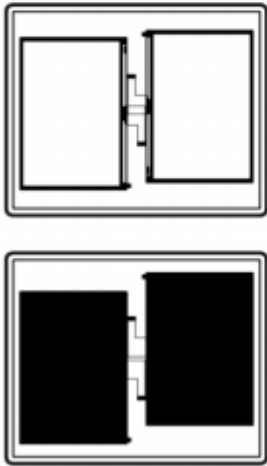
<b>Data sheet status</b>	
Product specification	The data sheet contains final product specifications.
<b>Limiting values</b>	
<p>Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134).</p> <p>Stress above one or more of the limiting values may cause permanent damage to the device.</p> <p>These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.</p>	
<b>Application information</b>	
<p>Where application information is given, it is advisory and does not form part of the specification.</p>	

<b>Product Environmental certification</b>
RoHS

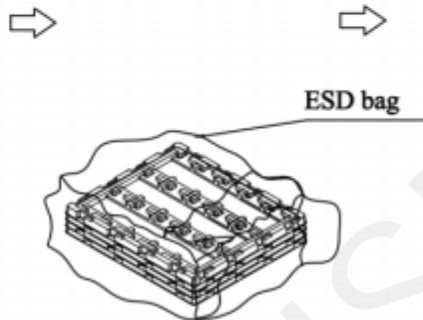
## 14. Packing

### PACKLING ORDER:

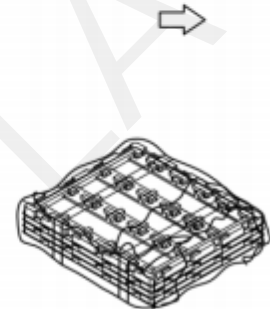
1) Putting 2 pcs Modules on each PET tray. And cover a dedicated EPE film.



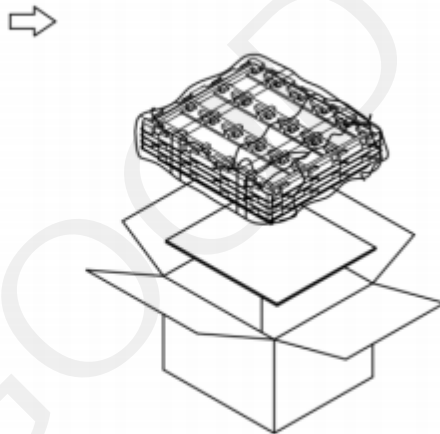
2) Putting 18 pcs PET trays together with 1 empty tray on the top of PET tray. Insert in the ESD bag, add desiccant in the ESD bag.



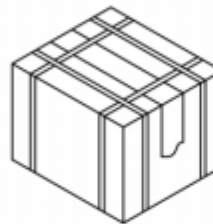
3) the tray together with adhesive tape



4) Putting into one outcarton



5) Packing finished



Note: 2 pcs in a tray, 18 trays in a out carton, so  $2 \times (18 - 1) = 36$  pcs/Outcarton

Dimension (Out carton): 454\*374\*190mm

## 15. Precautions

- (1) Do not apply pressure to the EPD panel in order to prevent damaging it.
- (2) Do not connect or disconnect the interface connector while the EPD panel is in operation.
- (3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.
- (4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.
- (5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue
- (6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.