

## Description

CMPA13SF2 is the P-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

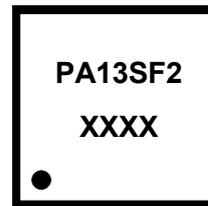
## Features

- $V_{DS}$ : -12V
- $I_D$ : -17A
- $R_{DS(on)}$  (@ $V_{GS}=-4.5V$ ): < 15m $\Omega$
- $R_{DS(on)}$  (@ $V_{GS}=-2.5V$ ): < 24m $\Omega$
- $R_{DS(on)}$  (@ $V_{GS}=-1.8V$ ): < 41m $\Omega$
- High density cell design for extremely low  $R_{DS(on)}$
- Excellent on-resistance and DC current capability

## Applications

- Cellular Handsets and Accessories
- Personal Digital Assistants
- Portable Instrumentation
- Load switch

## Marking Information

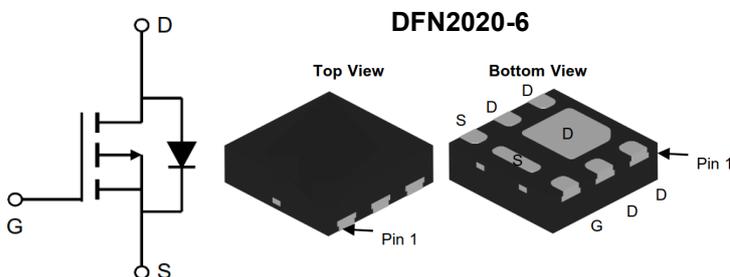


PIN 1

Marking Code = PA13SF2

Date Code = XXXX

## Equivalent Circuit and Pin Configuration



## Ordering Information

Part Number	Packaging	Reel Size
CMPA13SF2	3000/Tape & Reel	7 inch

## Absolute Maximum Ratings (TA=25 °C unless otherwise noted)

Parameter	Symbol	Maximum	Unit	
Drain-source Voltage	$V_{DS}$	-12	V	
Gate-source Voltage	$V_{GS}$	$\pm 10$	V	
Continuous Drain Current	$I_D$	$T_C=25^\circ C$	-17	A
		$T_C=70^\circ C$	-13	A
	$I_D$	$T_A=25^\circ C$	-10	A
		$T_A=70^\circ C$	-7	A
Pulsed Drain Current <sup>(1)</sup>	$I_{DM}$	-67	A	
Total Power Dissipation @ $T_A=25^\circ C$ <sup>(2)</sup>	$P_D$	9.6	W	
Thermal Resistance Junction-to-Case <sup>(2)</sup>	$R_{\theta JC}$	13	$^\circ C/W$	
Thermal Resistance Junction-to-Ambient <sup>(2)</sup>	$R_{\theta JA}$	40	$^\circ C/W$	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ C$	

**Electrical Characteristics (T<sub>J</sub>=25 °C unless otherwise noted)**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-12			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-12V, V <sub>GS</sub> =0V, T <sub>C</sub> =25°C			-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±10V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-0.5		-1.0	V
Static Drain-Source on-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-5A		12	15	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-4A		18	24	
		V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-2A		32	41	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-5A, V <sub>GS</sub> =0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				-17	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-10V, V <sub>GS</sub> =0V, f=1MHz		1400		pF
Output Capacitance	C <sub>oss</sub>			235		
Reverse Transfer Capacitance	C <sub>rss</sub>			210		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =-4.5V, V <sub>DS</sub> =-10V, I <sub>D</sub> =-10A		19.4		nC
Gate Source Charge	Q <sub>gs</sub>			2.2		
Gate Drain Charge	Q <sub>gd</sub>			4.5		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =-4.5V, V <sub>DD</sub> =-10V, I <sub>D</sub> =-1A, R <sub>GEN</sub> =10Ω		22		ns
Turn-on Rise Time	t <sub>r</sub>			14.4		
Turn-off Delay Time	t <sub>D(off)</sub>			168		
Turn-off Fall Time	t <sub>f</sub>			69.2		

Noted: (1) Pulse Test: Pulse Width ≤ 300μs, Duty cycle ≤ 2%.

(2) Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. With 2oz Copper, t ≤ 10s

**Typical Performance Characteristics**

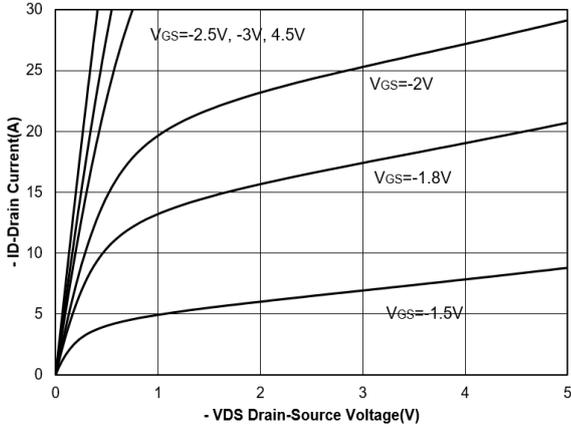


Figure 1. Output Characteristics

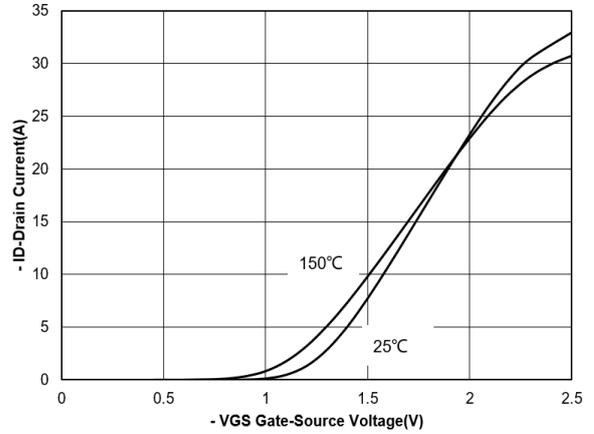


Figure 2. Transfer Characteristics

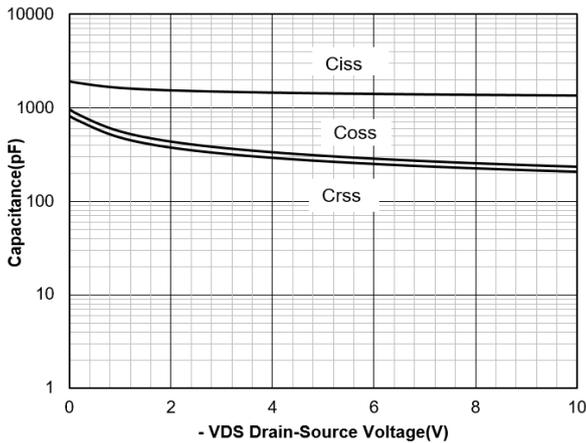


Figure 3. Capacitance Characteristics

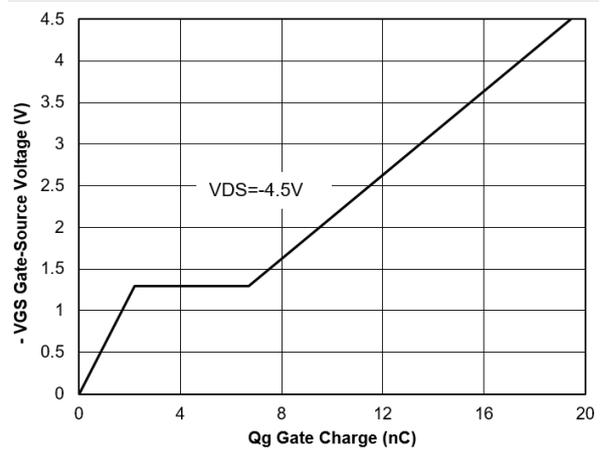


Figure 4. Gate Charge

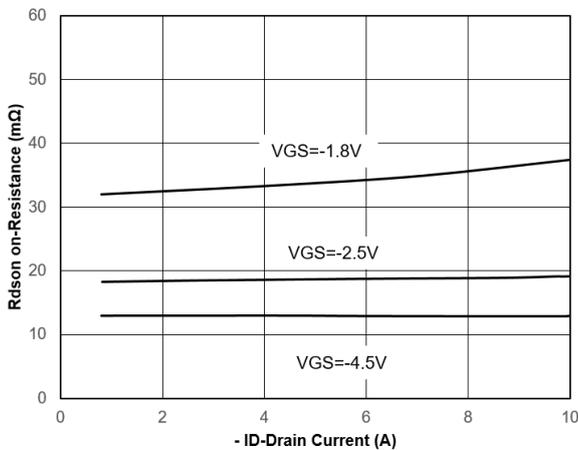


Figure 5. Drain-Source on Resistance

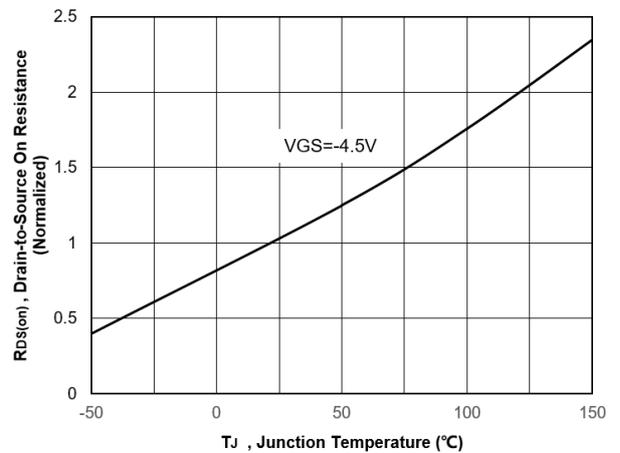


Figure 6. Normalized On-Resistance Vs. Temperature

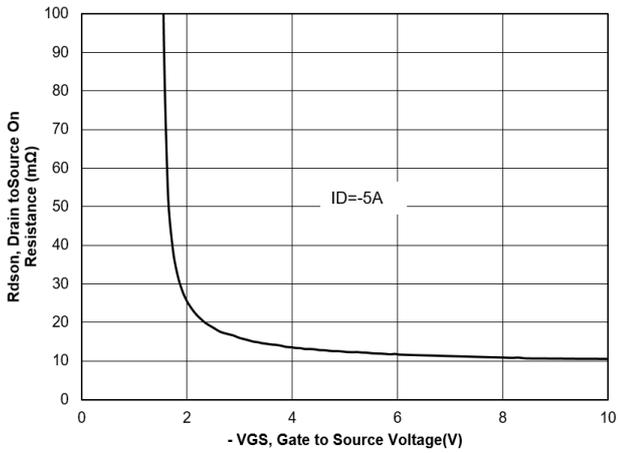


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

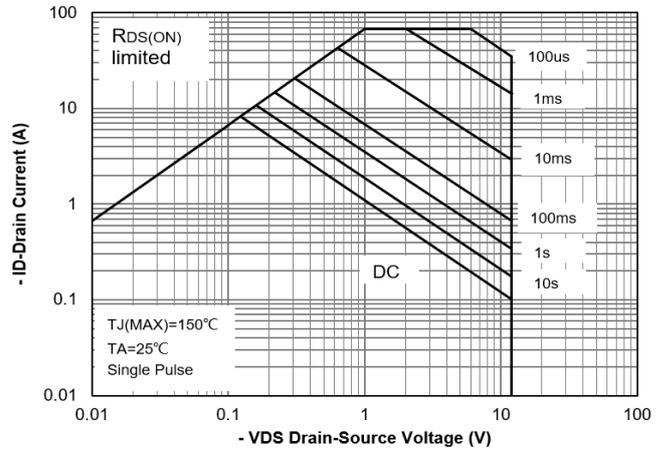


Figure 8. Safe Operation Area

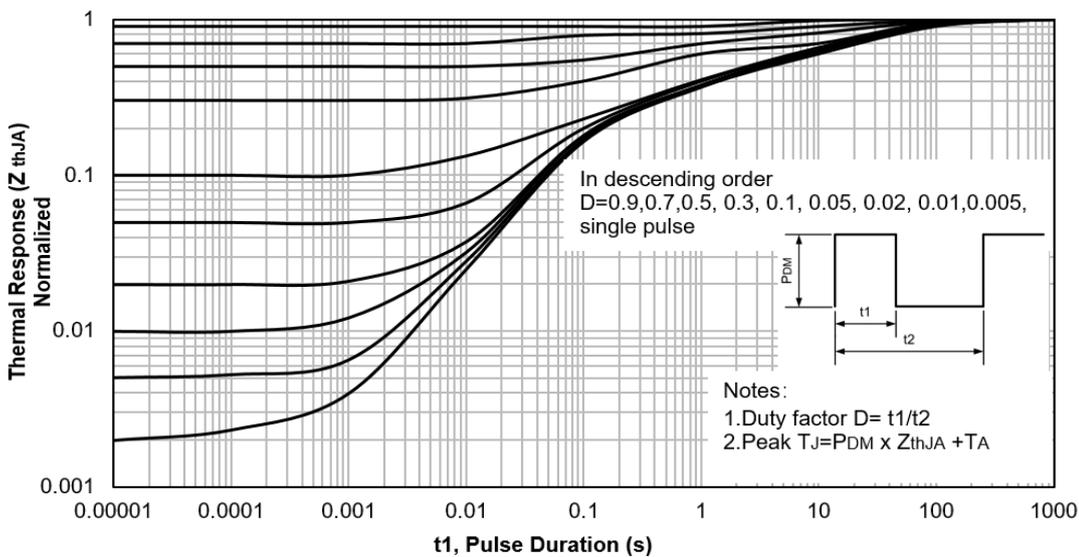


Figure 9. Maximum Effective Transient Thermal Impedance ,Junction-to-Ambient

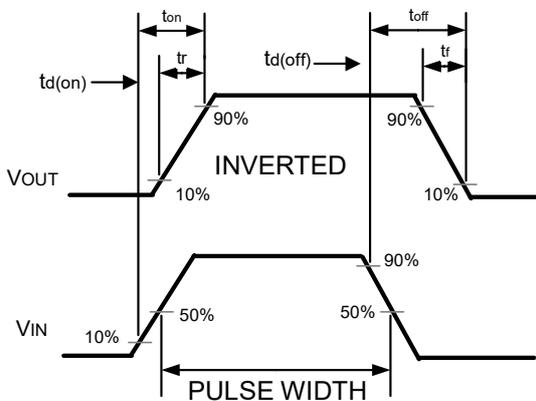
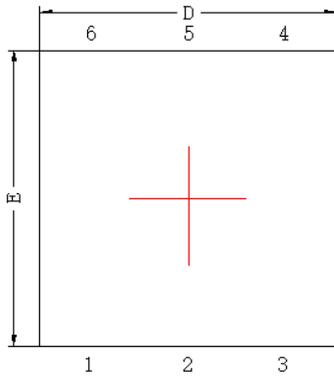


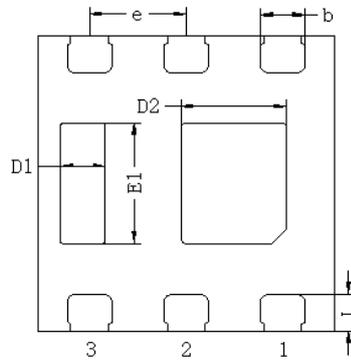
Figure 10. Switching wave

**DFN2020-6 Package Outline Drawing**

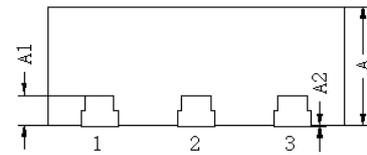
Top View



Bottom View



Side View



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.75	0.80	0.85
A1		0.2 REF	
A2	0.00	0.02	0.05
L	0.15	0.25	0.35
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
e		0.65 BSC	
D1	0.20	0.30	0.40
D2	0.61	0.71	0.81
E1	0.71	0.81	0.91

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