

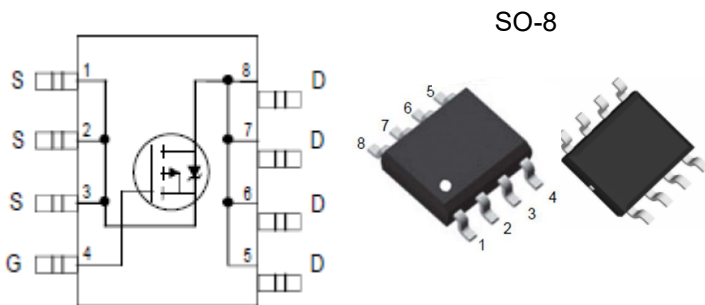
Description

The CMP4411AS8 is the P-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

Features

- V_{DS} : -30V
- I_D : -13.7A
- $R_{DS(on)}$ (@ $V_{GS}=-10V$): < 10.5m Ω
- $R_{DS(on)}$ (@ $V_{GS}=-4.5V$): < 15m Ω
- High density cell design for extremely low $R_{DS(on)}$
- Excellent on-resistance and DC current capability

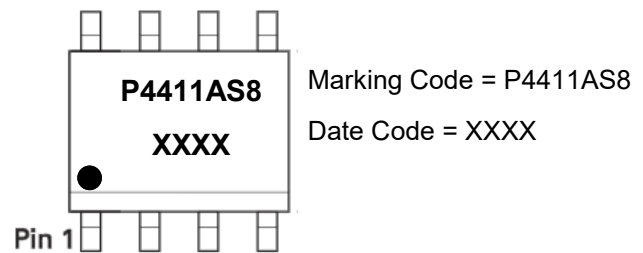
Equivalent Circuit and Pin Configuration



Applications

- Cellular Handsets and Accessories
- Personal Digital Assistants
- Portable Instrumentation
- Load switch

Marking Information



Ordering Information

Part Number	Packaging	Reel Size
CMP4411AS8	4000/Tape & Reel	13 inch

Absolute Maximum Ratings (TA=25 °C unless otherwise noted)

Parameter	Symbol	Maximum	Unit	
Drain-source Voltage	V_{DS}	-30	V	
Gate-source Voltage	V_{GS}	± 20	V	
Continuous Drain Current	I_D	$T_A=25^\circ C$	-13.7	A
		$T_A=70^\circ C$	-10.5	A
Pulsed Drain Current ⁽¹⁾	I_{DM}	-55	A	
Total Power Dissipation @ $T_A=25^\circ C$ ⁽²⁾	P_D	3.0	W	
Thermal Resistance Junction-to-Ambient ⁽²⁾	$R_{\theta JA}$	42	$^\circ C/W$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$	

Electrical Characteristics (T_J=25 °C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-24V, V _{GS} =0V, T _C =25°C			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1		-2.5	V
Static Drain-Source on-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-14A		8.7	10.5	mΩ
		V _{GS} =-4.5V, I _D =-10A		11.5	15	
Diode Forward Voltage	V _{SD}	I _S =-14A, V _{GS} =0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I _S				-14	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-15V, V _{GS} =0V, f=1MHz		2350		pF
Output Capacitance	C _{oss}			354		
Reverse Transfer Capacitance	C _{rss}			255		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-4.5V, V _{DS} =-15V, I _D =-10A		29		nC
Gate Source Charge	Q _{gs}			6.3		
Gate Drain Charge	Q _{gd}			7.8		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DD} =-15V, I _D =-1A, R _{GEN} =6Ω		12.6		ns
Turn-on Rise Time	t _r			6.4		
Turn-off Delay Time	t _{D(off)}			232		
Turn-off Fall Time	t _f			80		

Noted: (1) Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

(2) Device mounted on FR-4 PCB , 1 inch x 0.85 inch x 0.062 inch with 2oz. Copper , t ≤ 10s.

Typical Performance Characteristics

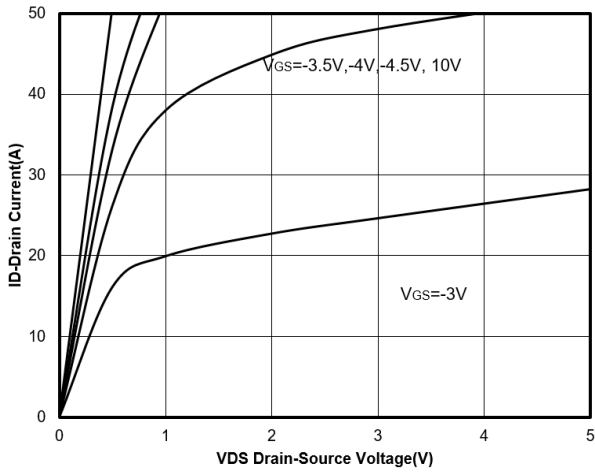


Figure 1. Output Characteristics

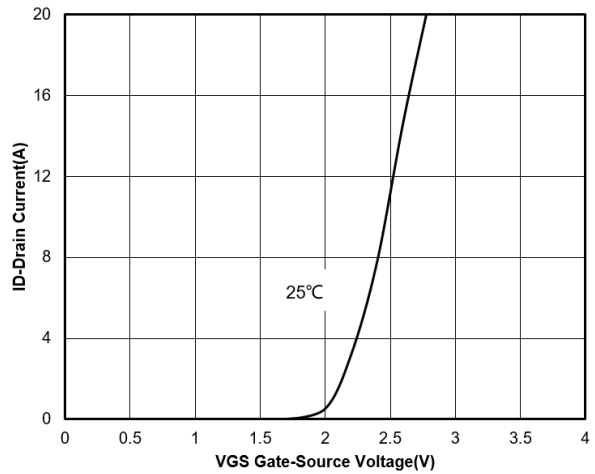


Figure 2. Transfer Characteristics

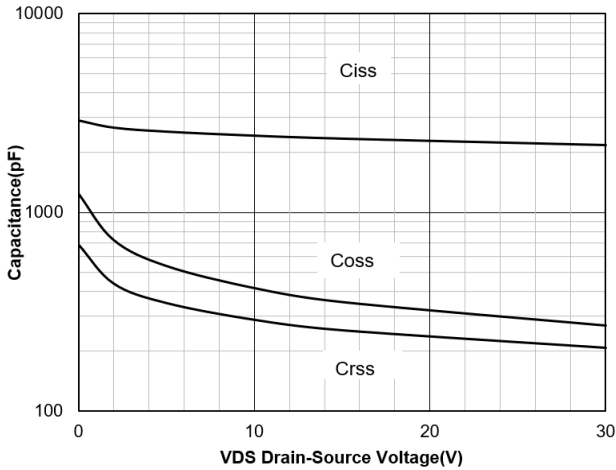


Figure 3. Capacitance Characteristics

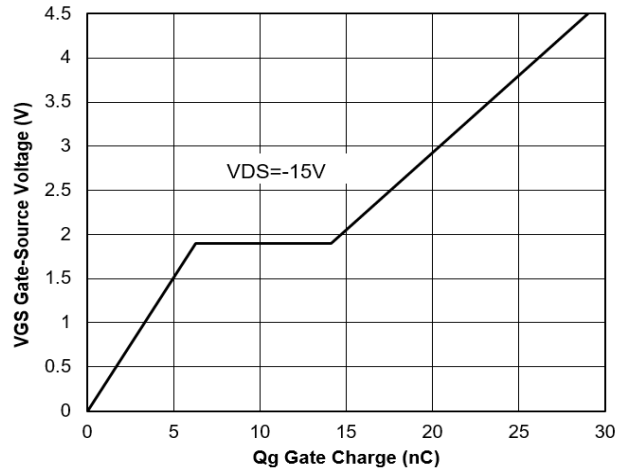


Figure 4. Gate Charge

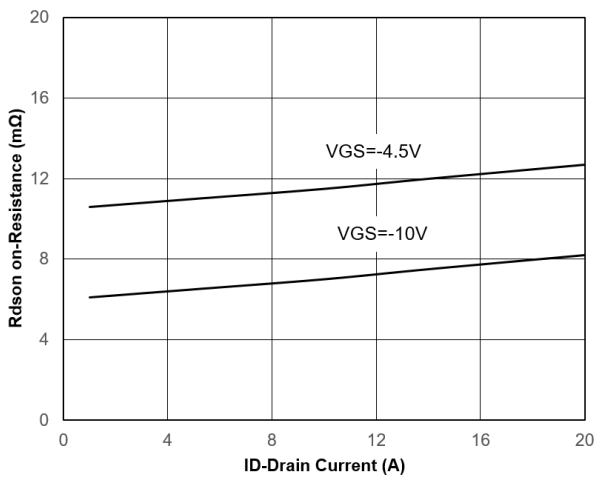


Figure 5. Drain-Source on Resistance

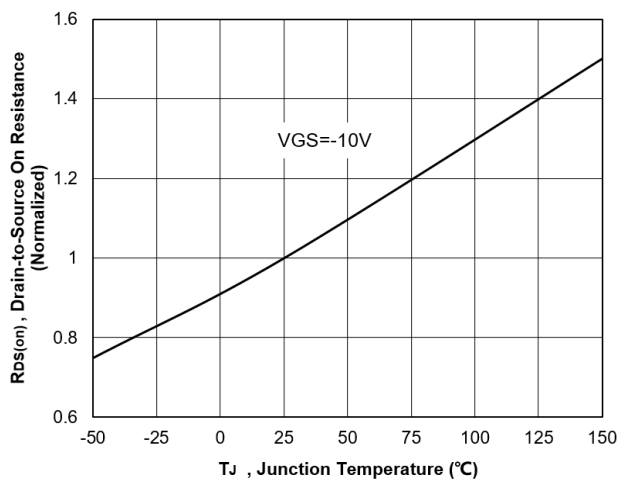


Figure 6. Normalized On-Resistance

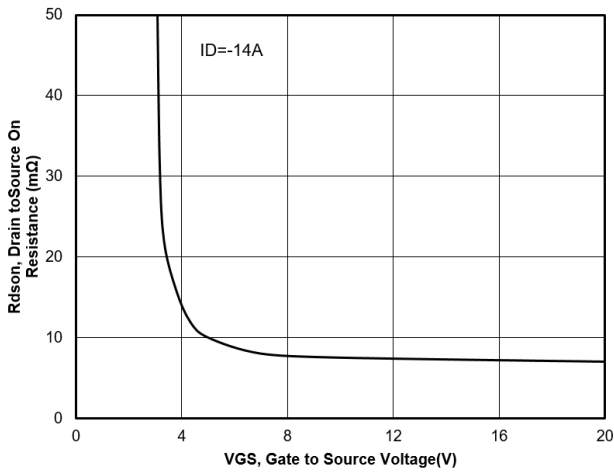


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

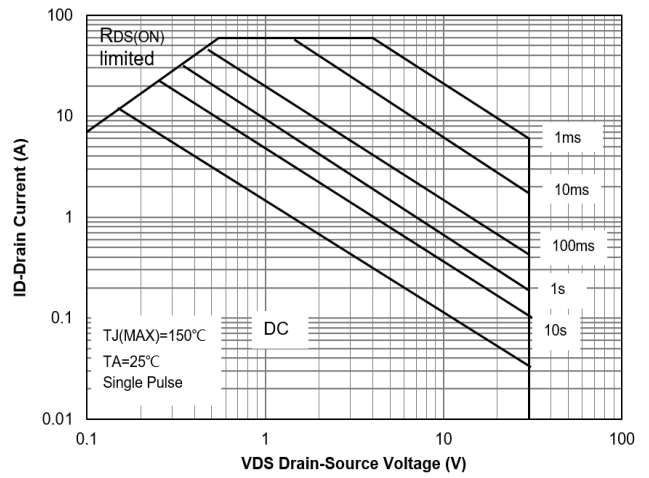


Figure 8. Safe Operation Area

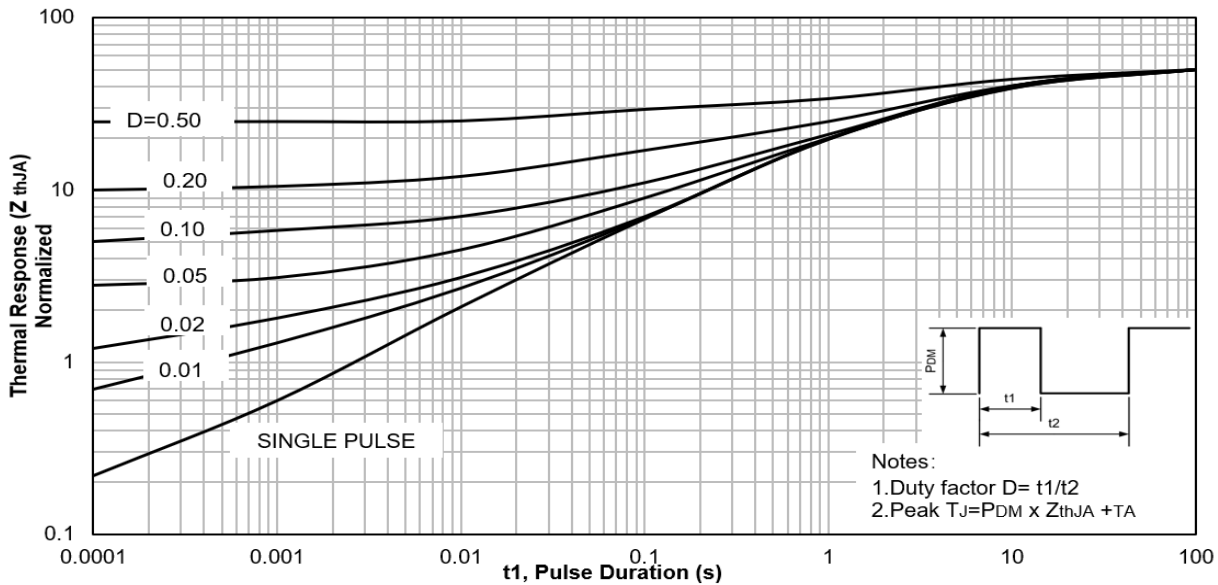


Figure 9. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

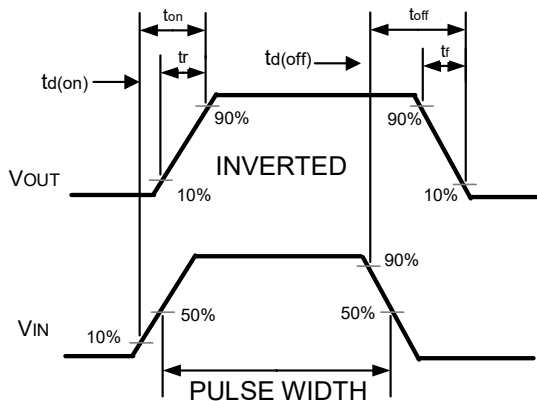
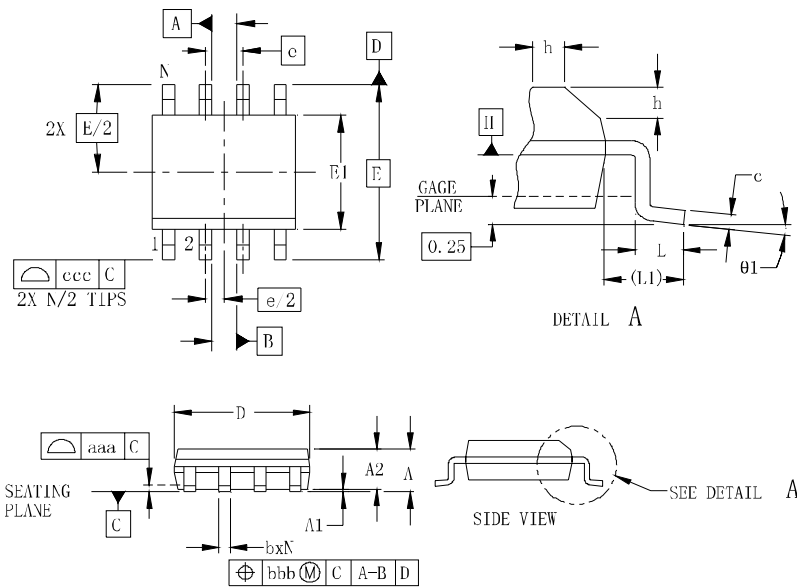


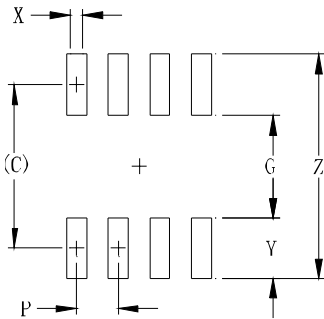
Figure 10. Switching wave

SO-8 Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.25		1.65	0.049		0.065
b	0.31		0.51	0.012		0.020
c	0.17		0.25	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E1	3.80	3.90	4.00	0.150	0.154	0.157
E	6.00 BSC			0.236 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25		0.50	0.010		0.020
L	0.40	0.72	1.04	0.016	0.028	0.041
L1	(1.04)			(0.041)		
N	8			8		
θ_1	0°		8°	0°		8°
aaa	0.10			0.004		
bbb	0.25			0.010		
ccc	0.20			0.008		

Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
C	5.20	0.205
G	3.00	0.118
P	1.27	0.050
X	0.60	0.024
Y	2.20	0.087
Z	7.40	0.291