

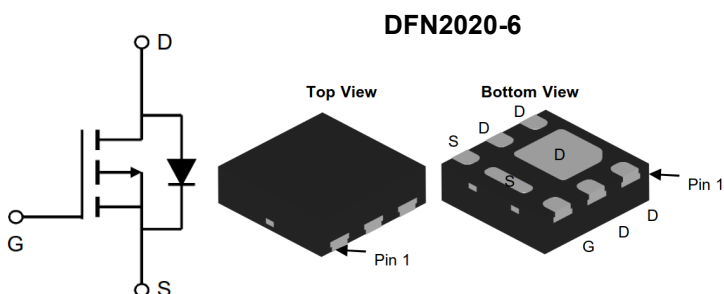
Description

CMP3031F2 is the P-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

Features

- V_{DS} : -30V
- I_D : -9.4A
- $R_{DS(on)}$ (@ $V_{GS}=-10V$): < 25m Ω
- $R_{DS(on)}$ (@ $V_{GS}=-4.5V$): < 35m Ω
- High density cell design for extremely low $R_{DS(on)}$
- Excellent on-resistance and DC current capability

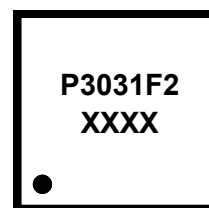
Equivalent Circuit and Pin Configuration



Applications

- Cellular Handsets and Accessories
- Personal Digital Assistants
- Portable Instrumentation
- Load switch

Marking Information



PIN 1

Marking Code = P3031F2
 Date Code = XXXX

Ordering Information

Part Number	Packaging	Reel Size
CMP3031F2	3000/Tape & Reel	7 inch

Absolute Maximum Ratings (TA=25 °C unless otherwise noted)

Parameter	Symbol	Maximum	Unit	
Drain-source Voltage	V_{DS}	-30	V	
Gate-source Voltage	V_{GS}	± 20	V	
Continuous Drain Current	I_D	$T_A=25^\circ C$	-9.4	A
		$T_A=70^\circ C$	-7.5	A
Pulsed Drain Current ⁽¹⁾	I_{DM}	-37.6	A	
Total Power Dissipation @ $T_A=25^\circ C$ ⁽²⁾	P_D	1.4	W	
Thermal Resistance Junction-to-Ambient ⁽²⁾	$R_{\theta JA}$	44	$^\circ C/W$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$	

Electrical Characteristics (T_J=25 °C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V, V _{GS} =0V, T _C =25°C			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0		-3.0	V
Static Drain-Source on-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-8A		19	25	mΩ
		V _{GS} =-4.5V, I _D =-6A		25	35	
Diode Forward Voltage	V _{SD}	I _S =-1A, V _{GS} =0V			-1.2	V
Maximum Body-Diode Continuous Current	I _S				-9.4	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-15V, V _{GS} =0V, f=1MHz		1300		pF
Output Capacitance	C _{oss}			170		
Reverse Transfer Capacitance	C _{rss}			126		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-15V, I _D =-9.4A		30		nC
Gate Source Charge	Q _{gs}			5.3		
Gate Drain Charge	Q _{gd}			7.6		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DD} =-15V, I _D =-6A, R _{GEN} =2.5Ω		14		ns
Turn-on Rise Time	t _r			20		
Turn-off Delay Time	t _{D(off)}			95		
Turn-off Fall Time	t _f			65		

Noted: (1) Pulse Test: Pulse Width ≤ 300μs, Duty cycle ≤ 2%.

(2) Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. With 2oz Copper, t ≤ 10s

Typical Performance Characteristics

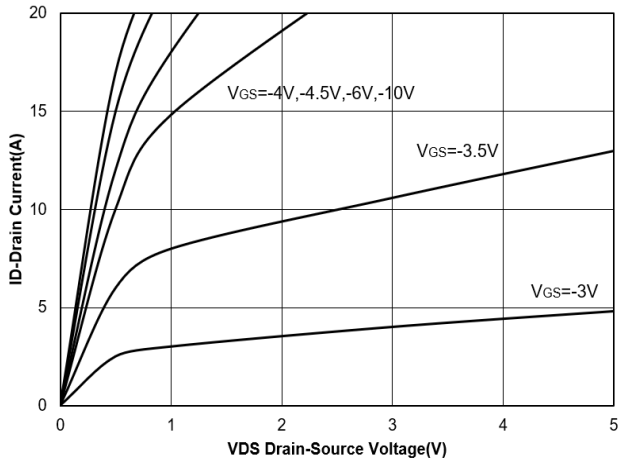


Figure 1. Output Characteristics

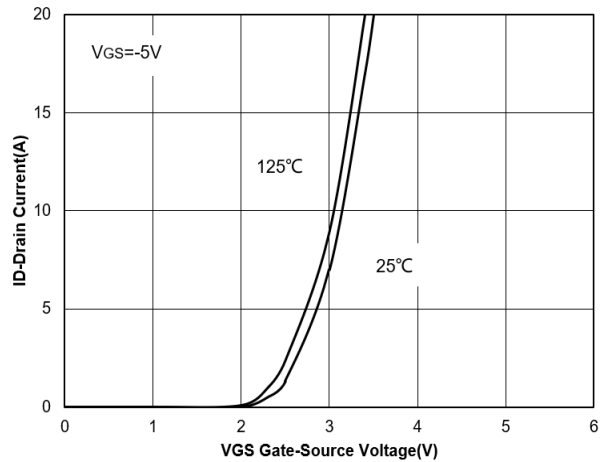


Figure 2. Transfer Characteristics

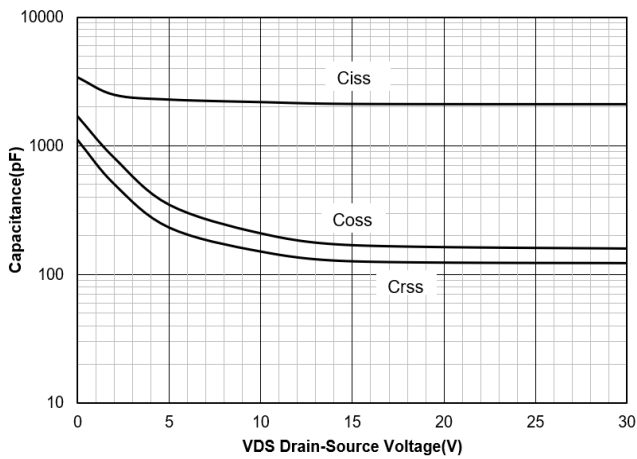


Figure 3. Capacitance Characteristics

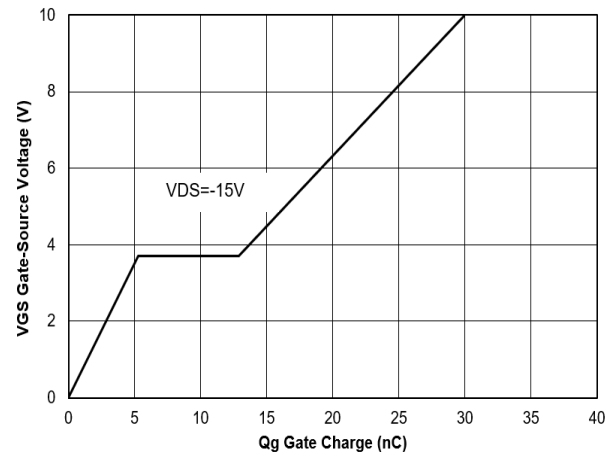


Figure 4. Gate Charge

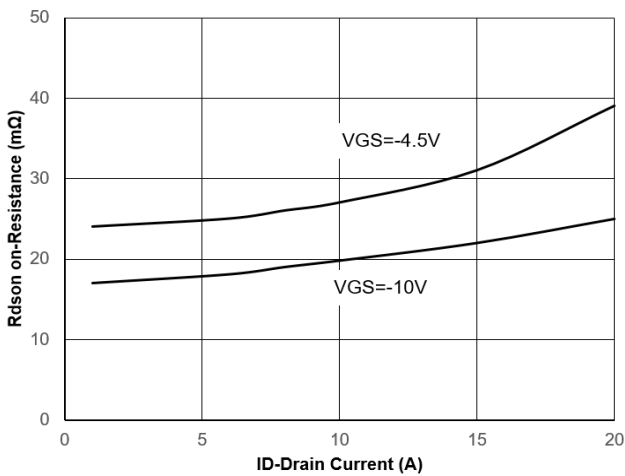


Figure 5. Drain-Source on Resistance

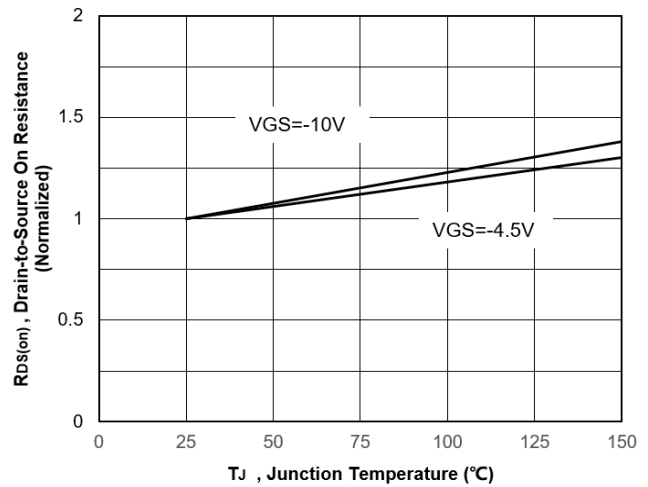


Figure 6. Normalized On-Resistance

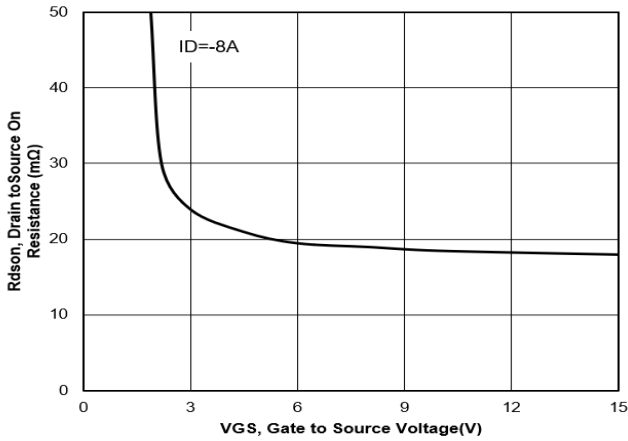


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

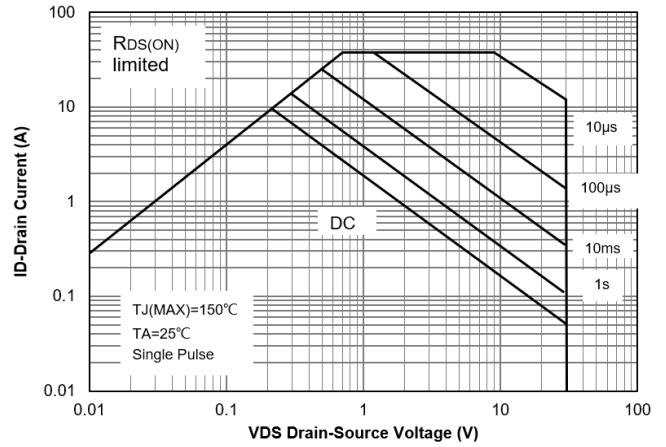


Figure 8. Safe Operation Area

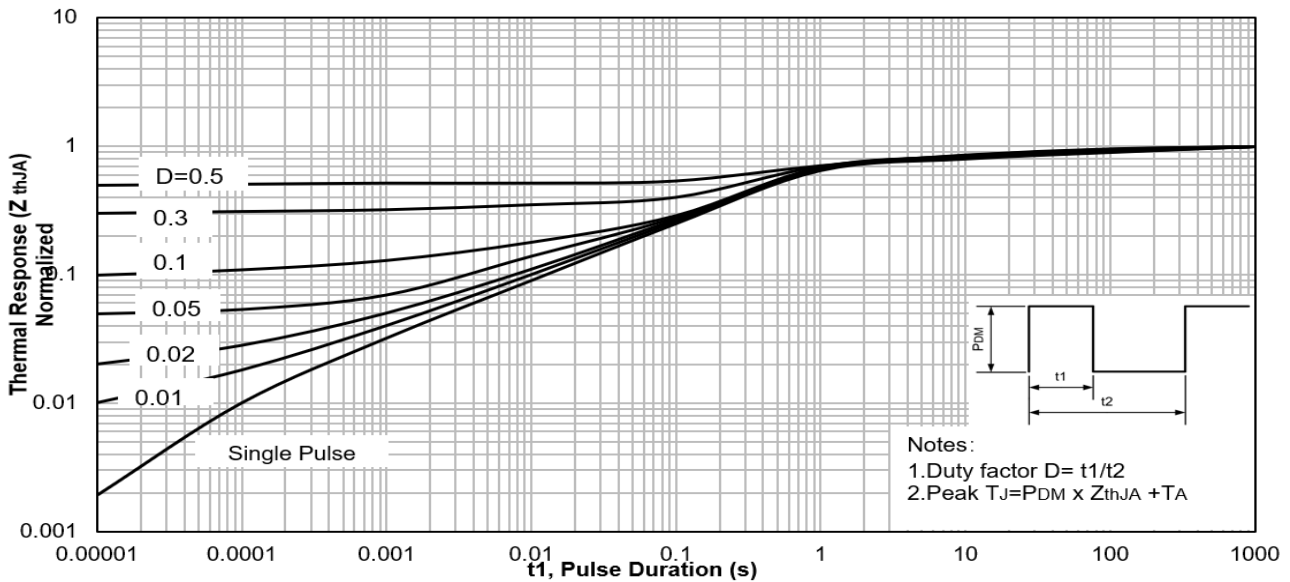


Figure 9. Maximum Effective Transient Thermal Impedance ,Junction-to-Ambient

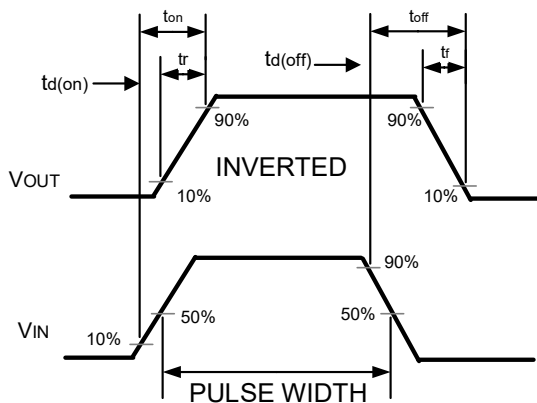
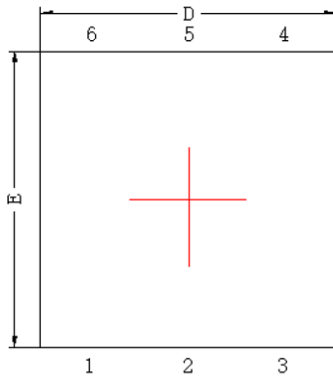


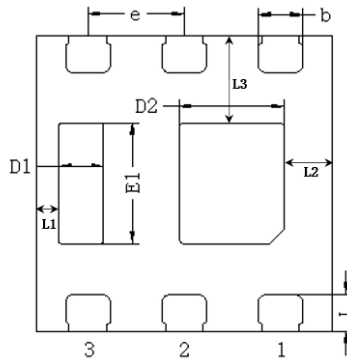
Figure 10. Switching wave

DFN2020-6 Package Outline Drawing

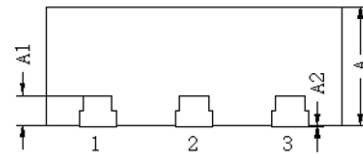
Top View



Bottom View



Side View



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.75	0.80	0.85
A1	0.2 REF		
A2	0.00	0.02	0.05
L	0.15	0.25	0.35
L1	0.156 REF		
L2	0.326 REF		
L3	0.595 REF		
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
e	0.65 BSC		
D1	0.20	0.30	0.40
D2	0.61	0.71	0.81
E1	0.71	0.81	0.91

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