Description

The CMP1080GF5 is the P-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

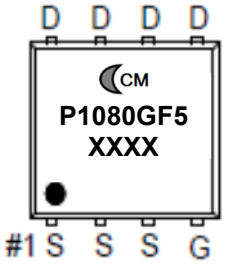
Applications

- Battery management
- Power management
- Load switch

Features

- V_{DS}: -100V
- I_D: -15A
- $R_{DS_{ON}}$ (@V_{GS}=-10V) : < 100mΩ
- $R_{DS_{ON}}$ (@V_{GS}=-4.5V) : < 130mΩ
- High density cell design for extremely low $R_{DS_{ON}}$
- Excellent on-resistance and DC current capability

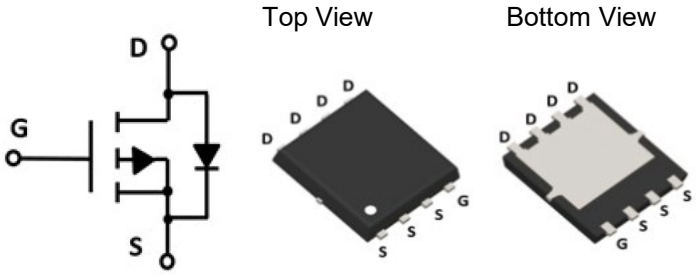
Marking Information



Marking Code =CMP1080GF5

Date Code = XXXX

Equivalent Circuit and Pin Configuration



Ordering Information

Part Number	Packaging	Reel Size
CMP1080GF5	5000/Tape & Reel	13 inch

Absolute Maximum Ratings (T_A=25 ℃ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	-100	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current[1][6]	T_C=25°C	I_D	-15	A
	T_C=100°C		-9.5	A
	T_A=25°C	I_D	-4.4	A
	T_A=100°C		-2.8	A
Pulsed Drain Current[3]		I_{DM}	-60	A
Total Power Dissipation[4]	T_C=25°C	P_D	50	W
	T_A=25°C		4	W
Thermal Resistance Junction-to-Ambient[2][5]		$R_{\theta JA}$	30	°C/W
Thermal Resistance Junction-to-Case		$R_{\theta Jc}$	2.5	°C/W
Junction and Storage Temperature Range		T_J,T_{STG}	-55 to +150	°C

Electrical Characteristics (T_J=25 ℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=-250μA	-100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V,V_{GS}=0V,T_C=25°C			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1.0		-2.5	V
Static Drain-Source on-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-10A		85	110	mΩ
		V_{GS}=-4.5V,I_D=-5A		100	130	
Diode Forward Voltage	V_{SD}	I_S=-15A,V_{GS}=0V			-1.3	V
Maximum Body-Diode Continuous Current	I_S				-15	A
Dynamic Parameters						
Input Capacitance	Ciss	V_{DS}=-50V,V_{GS}=0V,f=1MHz		1020		pF
Output Capacitance	Coss			116		
Reverse Transfer Capacitance	Crss			8		
Switching Parameters						
Total Gate Charge	Qg	V_{GS}=-10V,V_{DS}=-50V,I_D=-5A		20		nC
Gate Source Charge	Qgs			3.8		
Gate Drain Charge	Qgd			4.4		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V,V_{DD}=-50V, R_G=6Ω,R_L=2.5Ω		11		ns
Turn-on Rise Time	tr			29		
Turn-off Delay Time	$t_{D(off)}$			78		
Turn-off Fall Time	tf			80		

Noted: (1) Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

(2) The value of $R_{\theta JA}$ is measured with the device mounted on lin2 FR-4 board with 2oz.Copper,in a still air environment with T_A =25°C.The Power dissipation PDSM is based on $R_{\theta JA}$ t≤10s and the maximum allowed junction temperature of 150°C.The value in any given application depends on the user's specific board design.

(3) Single pulse width limited by junction temperature $T_{J(MAX)}$ = 150°C.

(4) The power dissipation PD is based on $T_{J(MAX)}$ = 150°C,using junction-to-case thermal resistance, and is more useful in setting the upper Dissipation limit for cases where additional heatsinking is used.

(5) The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JA}$ and case to ambient.

(6) The maximum current rating is package limited.

Typical Performance Characteristics

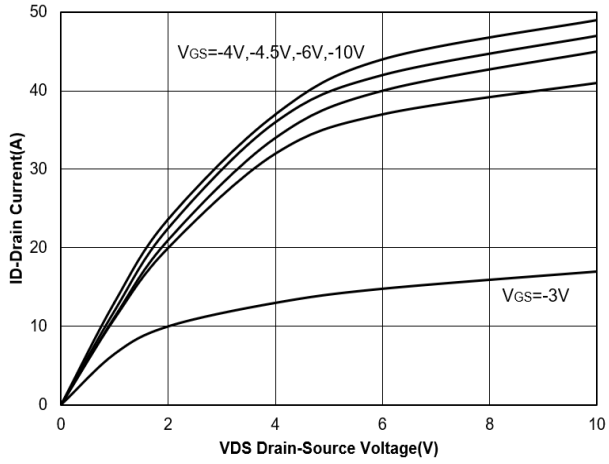


Figure 1. Output Characteristics

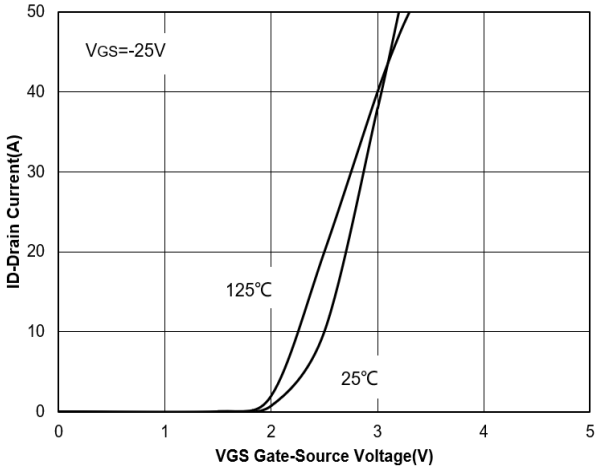


Figure 2. Transfer Characteristics

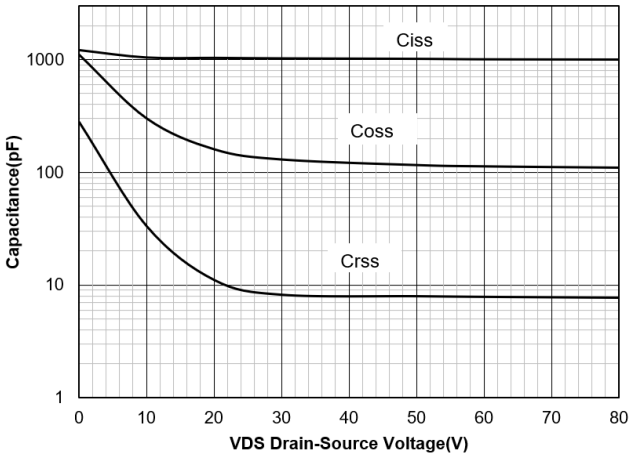


Figure 3. Capacitance Characteristics

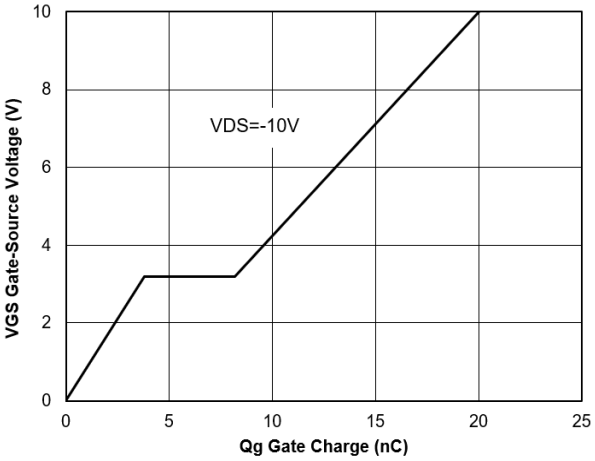


Figure 4. Gate Charge

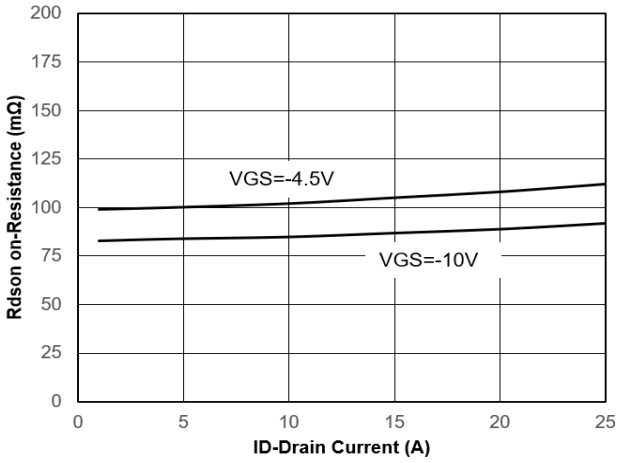


Figure 5. Drain-Source on Resistance

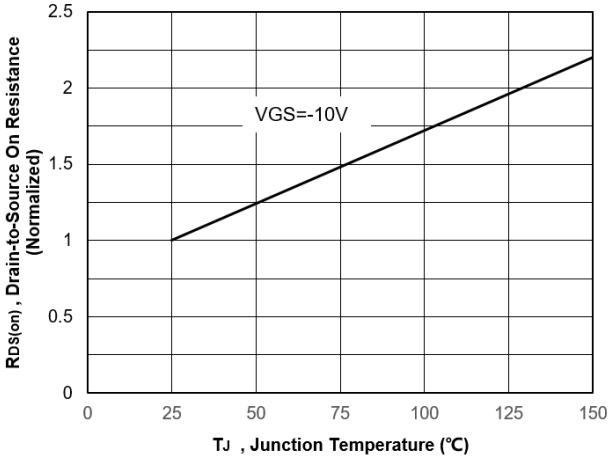


Figure 6. Normalized On-Resistance Vs. Temperature

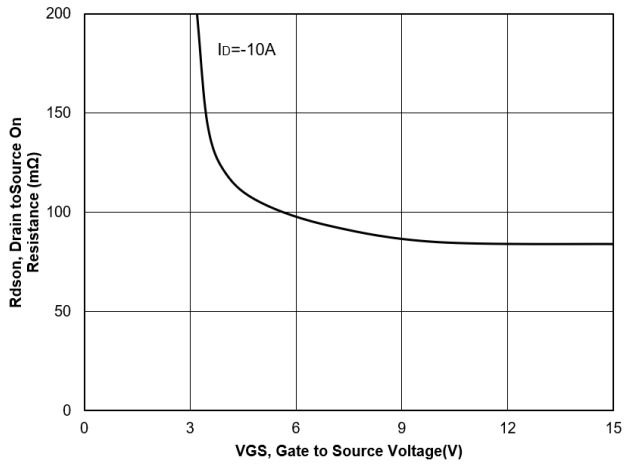


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

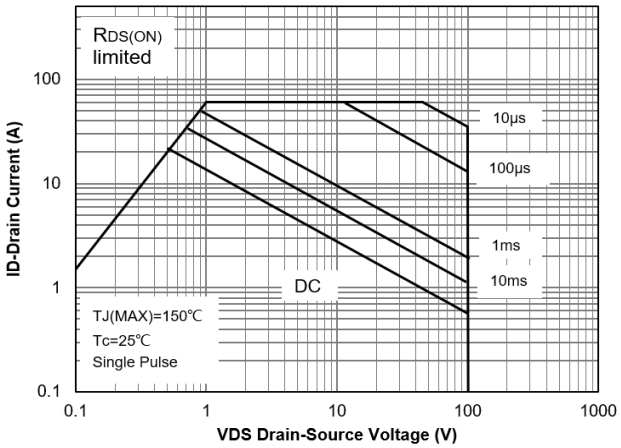


Figure 8. Safe Operation Area

Figure 9. Maximum Effective Transient Thermal Impedance,Junction-to-Case

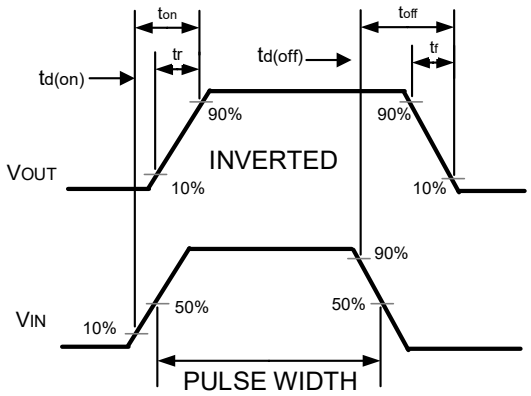
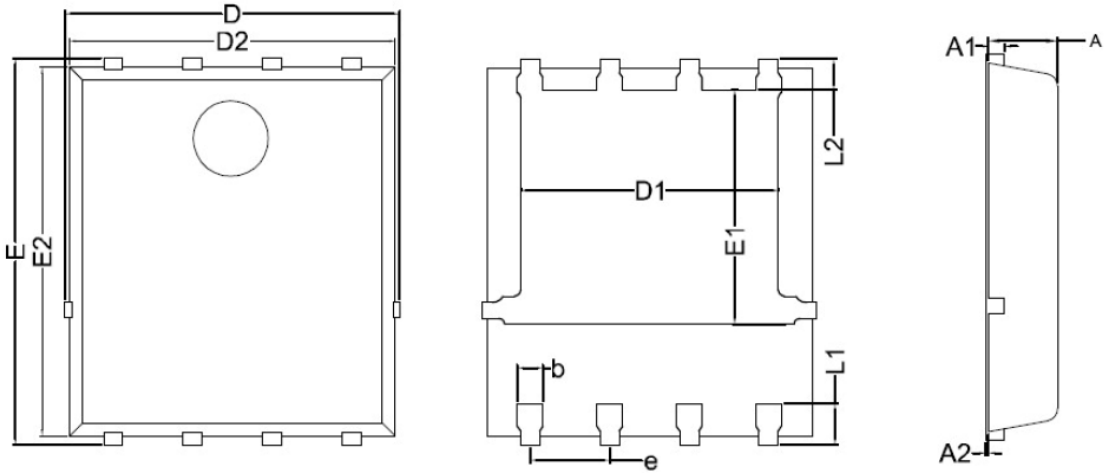
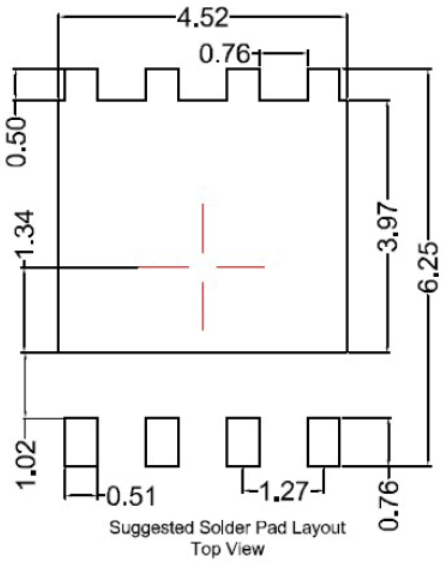


Figure 10. Switching wave

DFN 5X6 Package Outline Drawing



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	



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