CMP100160U

P-Channel 100V (D-S) Power MOSFET

Description

The CMP100160U is the P-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

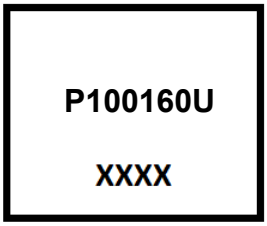
Applications

- Cellular Handsets and Accessories
- Personal Digital Assistants
- Portable Instrumentation
- Load switch

Features

- V_{DS}: -100V
- I_D: -10A
- $R_{DS_{ON}}$(@VGS=-10V) : < 215mΩ
- $R_{DS_{ON}}$ (@V_{GS}=-4.5V) : < 245mΩ
- High density cell design for extremely low $R_{DS_{ON}}$
- Excellent on-resistance and DC current capability

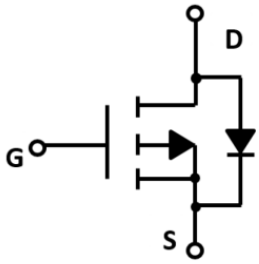
Marking Information



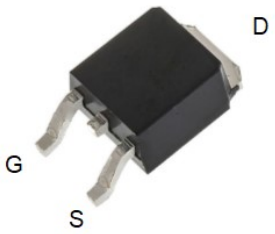
Marking Code = P100160U

Date Code = XXXX

Equivalent Circuit and Pin Configuration



TO-252



Ordering Information

Part Number	Packaging	Remark
CMP100160U	2500/Tape & Reel	ROHS

Absolute Maximum Ratings (T_C=25 ℃ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	-100	V
Gate-source Voltage		V_{GS}	±20	V
Continuous Drain Current[1]	T_C=25°C	I_D	-10	A
	T_C=100°C		-6.4	A
Pulsed Drain Current [2]		I_{DM}	-40	A
Total Power Dissipation [3]		P_D @T_C=25°C	42	W
		Derating Factor above 25°C	0.33	W/°C
Thermal Resistance Junction-to-Case [3]		$R_{\theta JC}$	3	°C/W
Junction and Storage Temperature Range		T_J,T_{STG}	-55 to +150	°C

Electrical Characteristics (Tc=25 ℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=-250μA	-100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-100V,V_{GS}=0V,T_C=25°C			-5	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1.0		-3.0	V
Static Drain-Source on-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-6A		180	215	mΩ
		V_{GS}=-4.5V,I_D=-3A		190	245	
Diode Forward Voltage	V_{SD}	I_S=-10A,V_{GS}=0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I_S				-10	A
Dynamic Parameters						
Input Capacitance	Ciss	VDS=-25V,VGS=0V,f=1MHz		1320		pF
Output Capacitance	Coss			42		
Reverse Transfer Capacitance	Crss			30		
Switching Parameters						
Total Gate Charge	Qg	V_{GS}=-10V,V_{DS}=-50V,I_D=-8A		19		nC
Gate Source Charge	Qgs			0.8		
Gate Drain Charge	Qgd			1.2		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V,V_{DD}=-50V, I_D=-8A ,R_{GEN}=2.2Ω		6.6		ns
Turn-on Rise Time	tr			4.1		
Turn-off Delay Time	$t_{D(off)}$			90		
Turn-off Fall Time	tf			21.6		

Noted: (1) Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

(2) The test with different tester may be preformed differently.

(3) Device mounted on FR-4 PCB , 1 inch x 0.85 inch x 0.062 inch with 2oz. Copper , t≤10s.

Typical Performance Characteristics

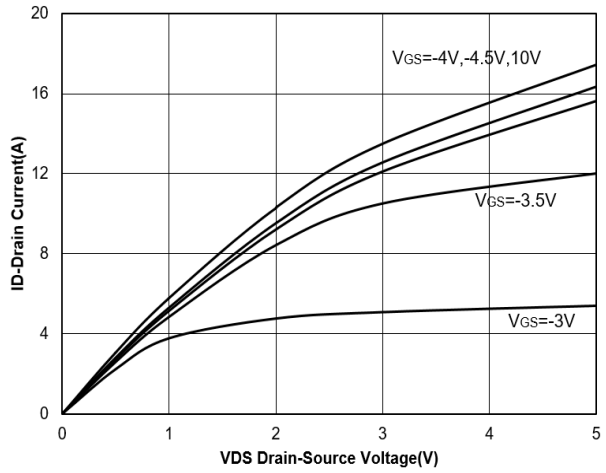


Figure 1. Output Characteristics

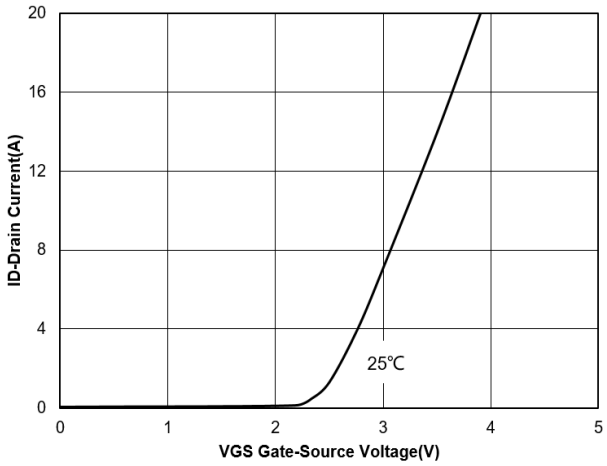


Figure 2. Transfer Characteristics

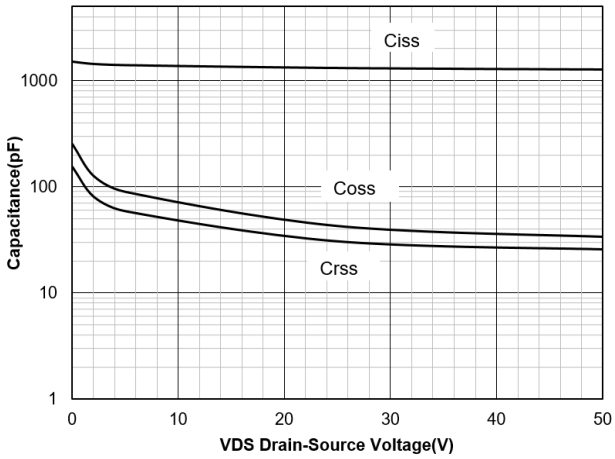


Figure 3. Capacitance Characteristics

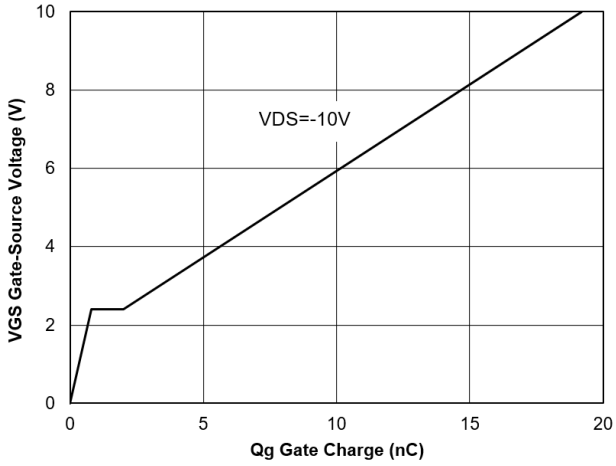


Figure 4. Gate Charge

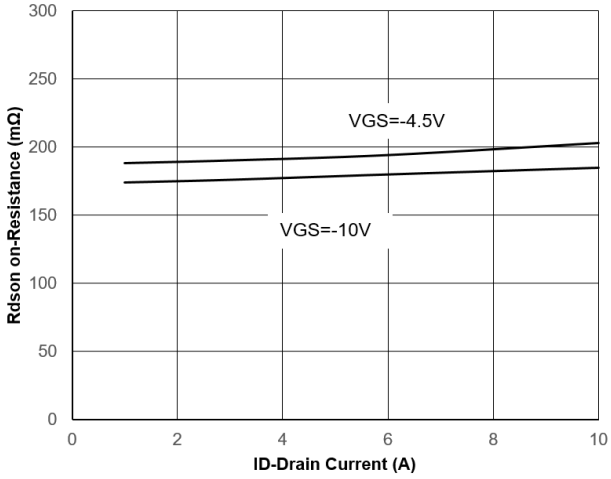


Figure 5. Drain-Source on Resistance

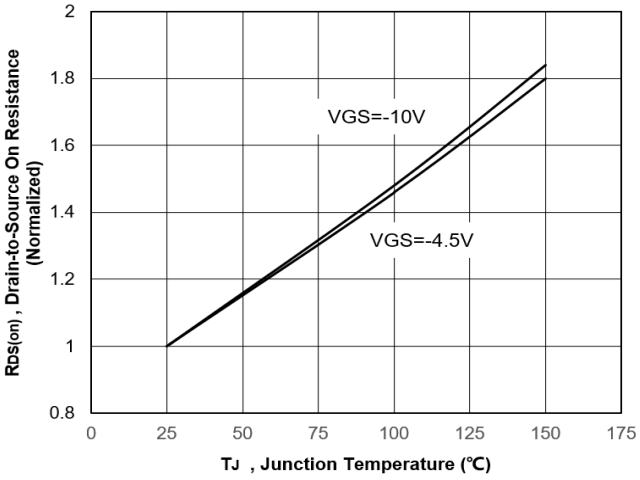


Figure 6. Normalized On-Resistance

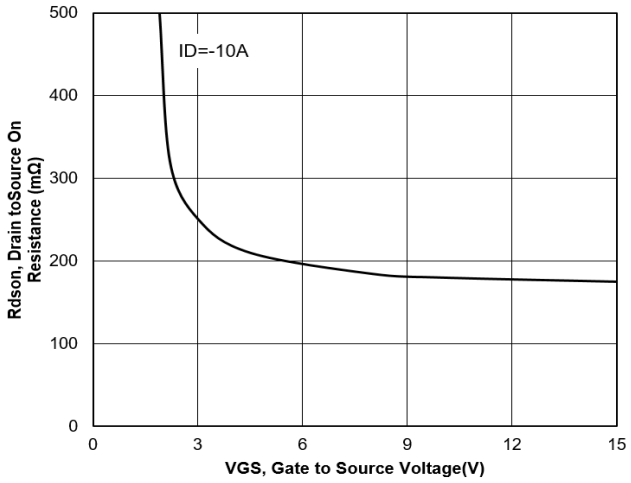


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

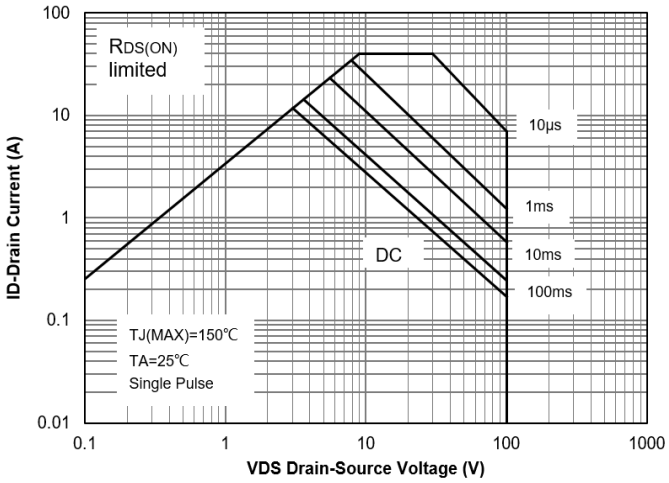


Figure 8. Safe Operation Area

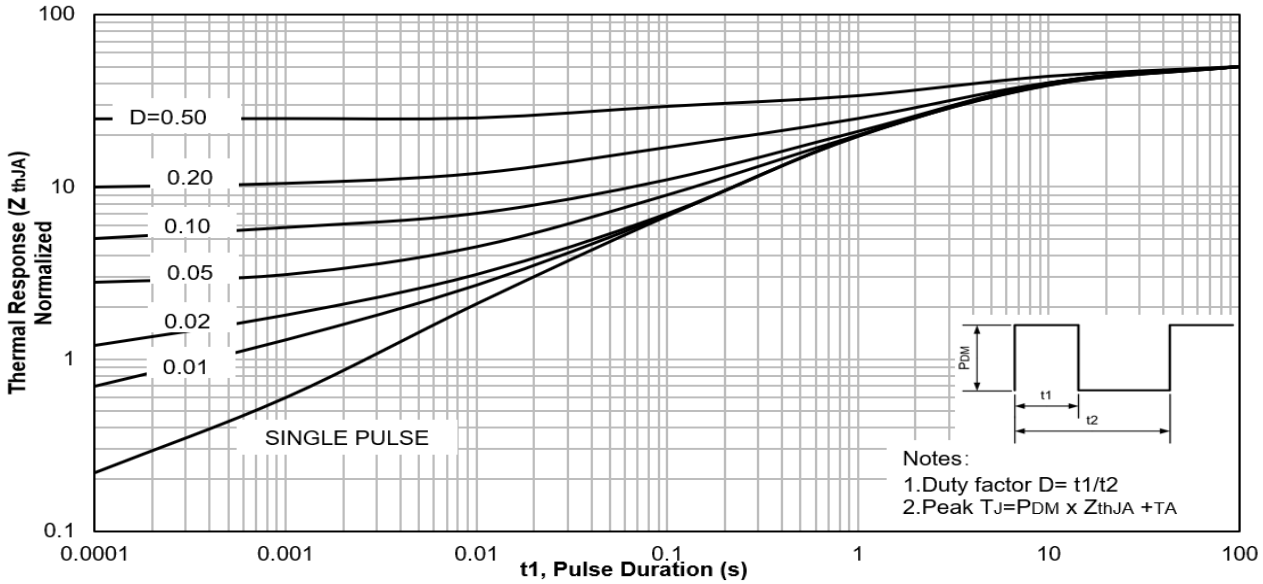


Figure 9. Maximum Effective Transient Thermal Impedance,Junction-to-Ambient

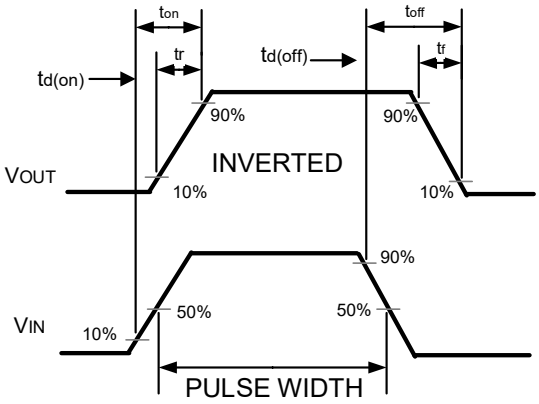
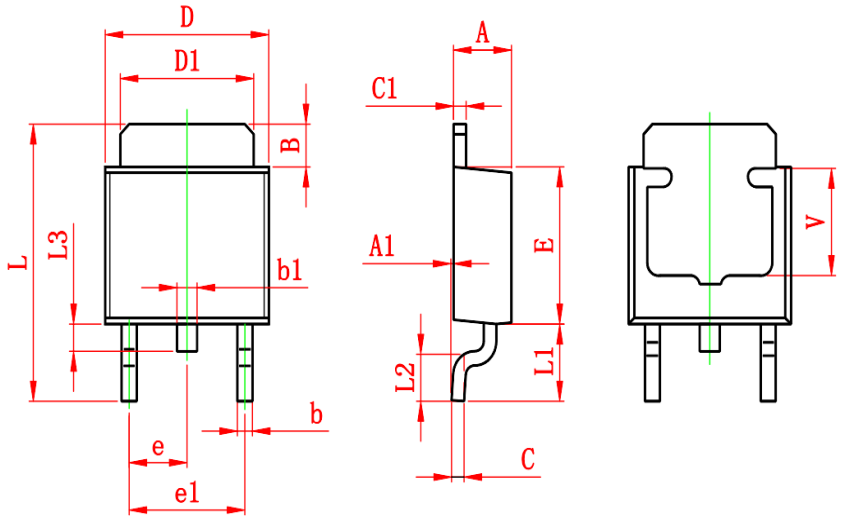


Figure 10. Switching wave

TO-252 Package Outline Drawing



Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP.		0.091 TYP.	
e1	4.500	4.700	0.177	0.185
L	9.500	9.900	0.374	0.390
L1	2.550	2.900	0.100	0.114
L2	1.400	1.780	0.055	0.070
L3	0.600	0.900	0.024	0.035
V	3.800 REF.		0.150 REF.	

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