

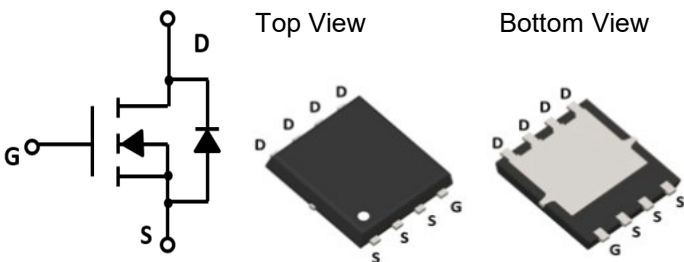
Description

The CMN6002GF5 is the N-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

Features

- V_{DS} : 60V
- I_D : 95A
- $R_{DS(on)}$ (@ $V_{GS}=10V$): < 2.5m Ω
- $R_{DS(on)}$ (@ $V_{GS}=4.5V$): < 3.4m Ω
- High density cell design for extremely low $R_{DS(on)}$
- Excellent on-resistance and DC current capability

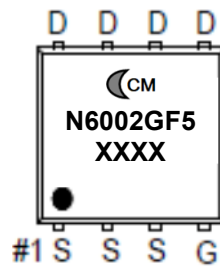
Equivalent Circuit and Pin Configuration



Applications

- Battery management
- Power management
- Load switch

Marking Information



Marking Code = CMN6002GF5

Date Code = XXXX

Ordering Information

Part Number	Packaging	Reel Size
CMN6002GF5	5000/Tape & Reel	13 inch

Absolute Maximum Ratings (TA=25 °C unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current ⁽¹⁾⁽⁶⁾	$T_C=25^\circ C$	I_D	95	A
	$T_C=100^\circ C$		60	A
	$T_A=25^\circ C$	I_D	16	A
	$T_A=100^\circ C$		10	A
Pulsed Drain Current ⁽³⁾		I_{DM}	380	A
Total Power Dissipation ⁽⁴⁾	$T_C=25^\circ C$	PD	50	W
	$T_A=25^\circ C$		6.25	W
Thermal Resistance Junction-to-Ambient ⁽²⁾⁽⁵⁾		$R_{\theta JA}$	20	$^\circ C/W$
Thermal Resistance Junction-to-Case		$R_{\theta Jc}$	2.5	$^\circ C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ C$

Electrical Characteristics (T_J=25 °C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BVDSS	V _{GS} =0V, I _D =250μA	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V, T _C =25°C			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source on-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A		2.1	2.5	mΩ
		V _{GS} =4.5V, I _D =15A		2.7	3.4	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V			1.2	V
Maximum Body-Diode Continuous Current	I _S				95	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=100KHz		5950		pF
Output Capacitance	C _{oss}			1250		
Reverse Transfer Capacitance	C _{rss}			85		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =50A		93		nC
Gate Source Charge	Q _{gs}			17		
Gate Drain Charge	Q _{gd}			14		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =30V, I _D =25A, R _{GEN} =2Ω		23		ns
Turn-on Rise Time	t _r			6.8		
Turn-off Delay Time	t _{D(off)}			80		
Turn-off Fall Time	t _f			27		

Noted: (1) Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

- (2) The value of R_{θJA} is measured with the device mounted on lin2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C. The Power dissipation P_{DSM} is based on R_{θJA}, t ≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
- (3) Single pulse width limited by junction temperature T_{J(MAX)} = 150°C.
- (4) The power dissipation P_D is based on T_{J(MAX)} = 150°C, using junction-to-case thermal resistance, and is more useful in setting the upper Dissipation limit for cases where additional heatsinking is used.
- (5) The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJA} and case to ambient.
- (6) The maximum current rating is package limited.

Typical Performance Characteristics

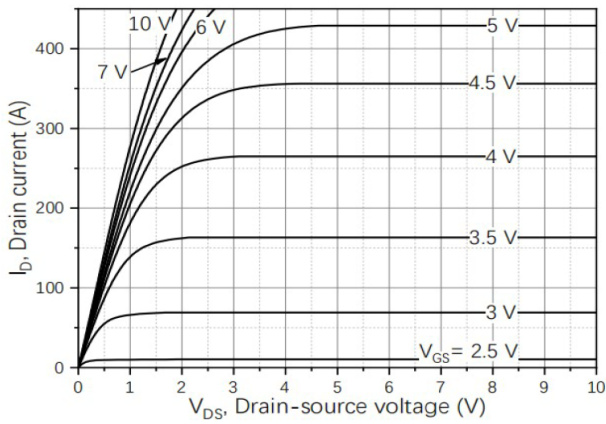


Figure 1. Output Characteristics

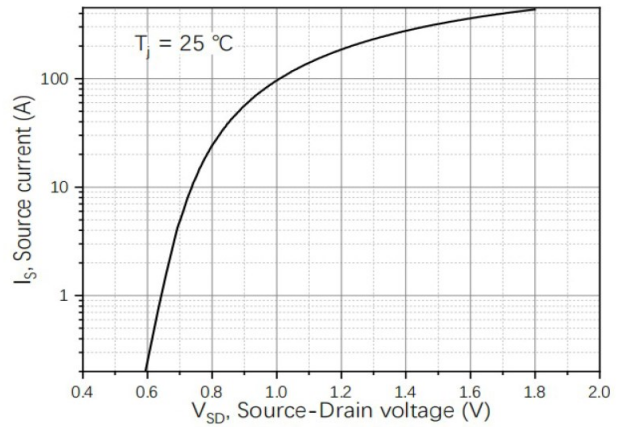


Figure 2. Transfer Characteristics

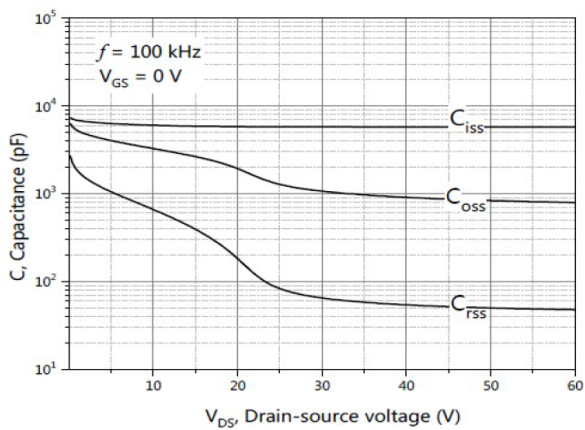


Figure 3. Capacitance Characteristics

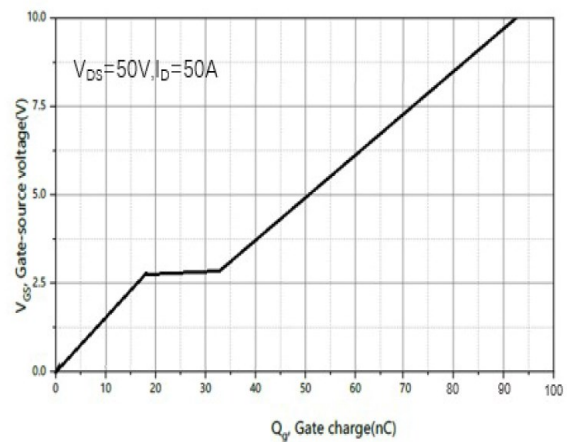


Figure 4. Gate Charge

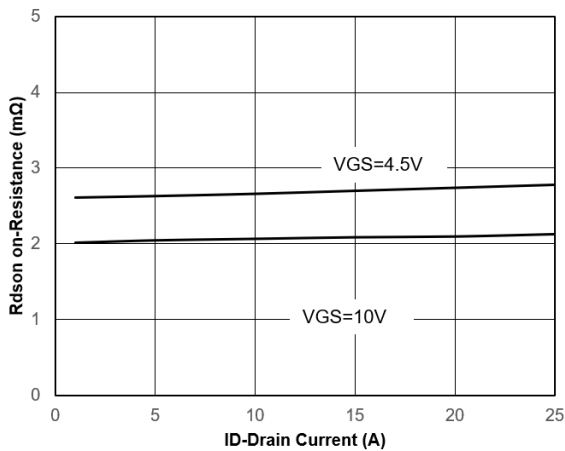


Figure 5. Drain-Source on Resistance

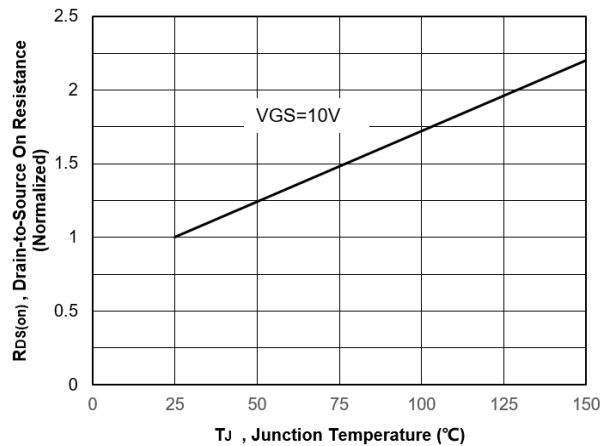


Figure 6. Normalized On-Resistance Vs. Temperature

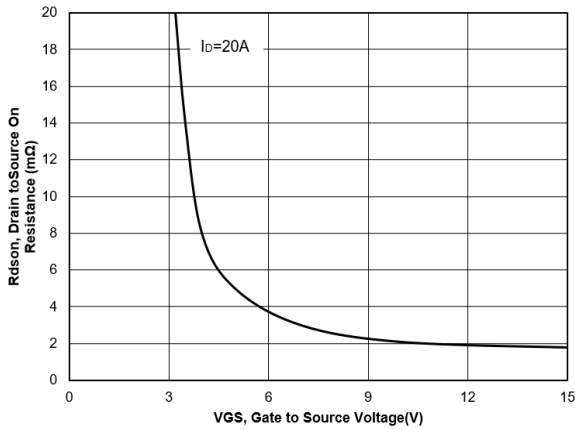


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

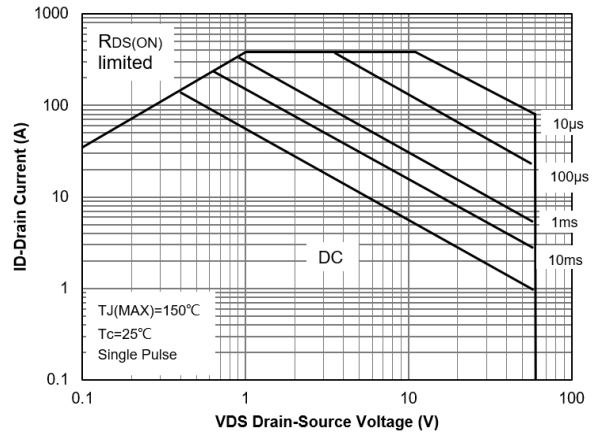


Figure 8. Safe Operation Area

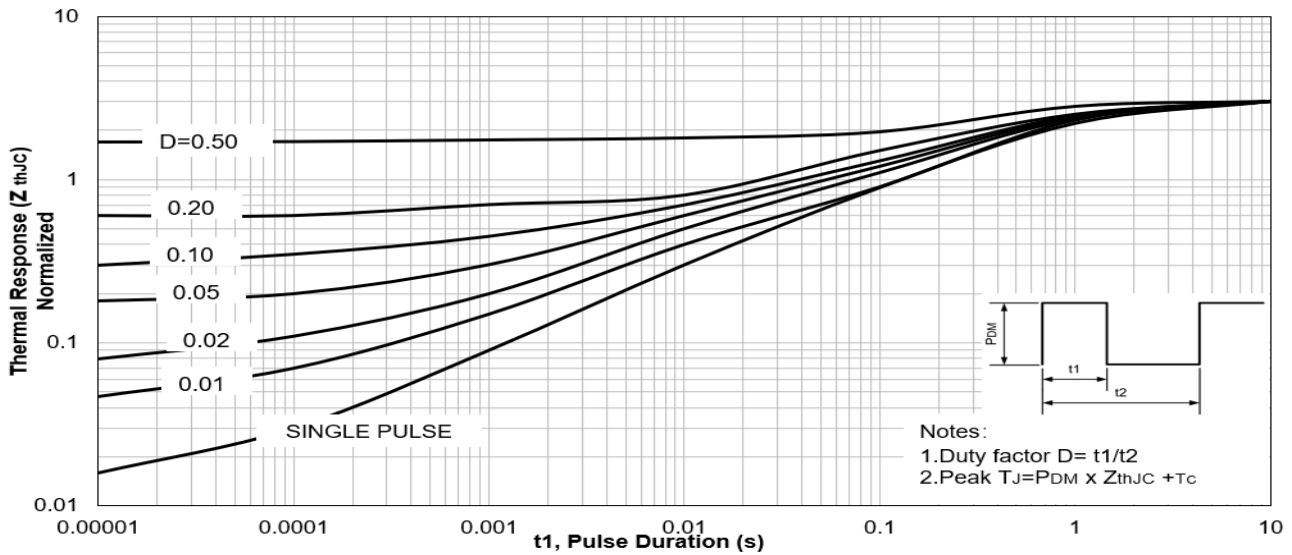


Figure 9. Maximum Effective Transient Thermal Impedance, Junction-to-Case

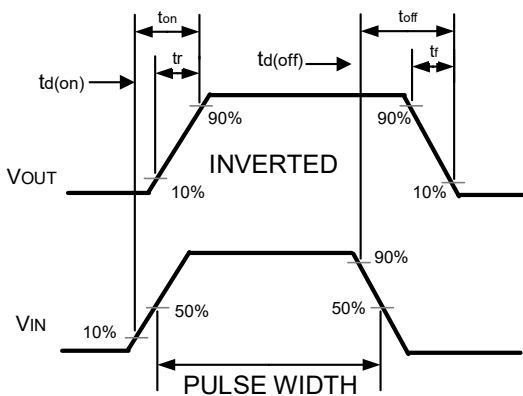
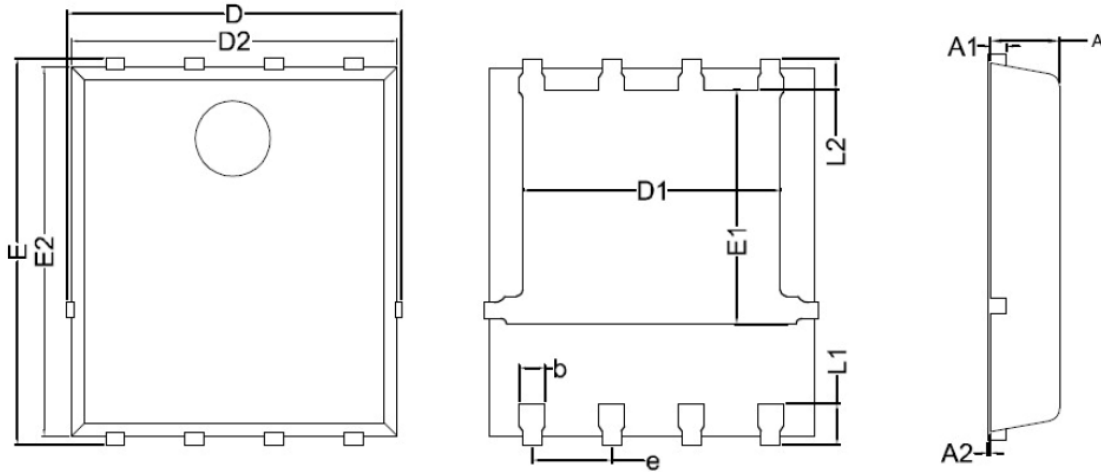
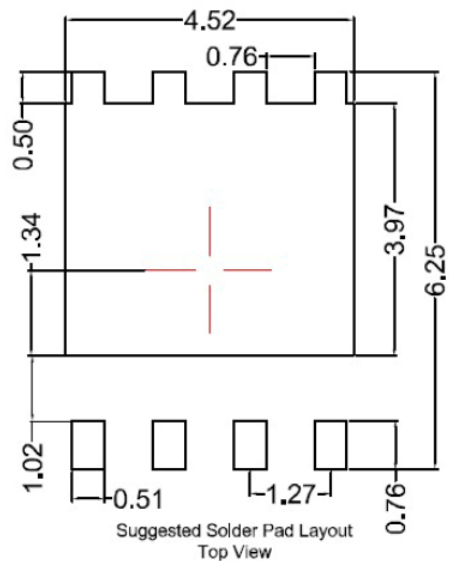


Figure 10. Switching wave

DFN 5X6 Package Outline Drawing



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		



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