CMN401R0F5

N-Channel 40V (D-S) Power MOSFET

Description

The CMN401R0F5 is the N-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

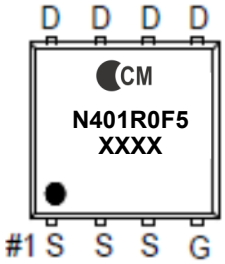
Applications

- Battery management
- Power management
- Load switch

Features

- V_{DS}: 40V
- I_D: 212A
- $R_{DS_{ON}}$ (@V_{GS}=10V) : < 1.4mΩ
- High density cell design for extremely low $R_{DS_{ON}}$
- Excellent on-resistance and DC current capability

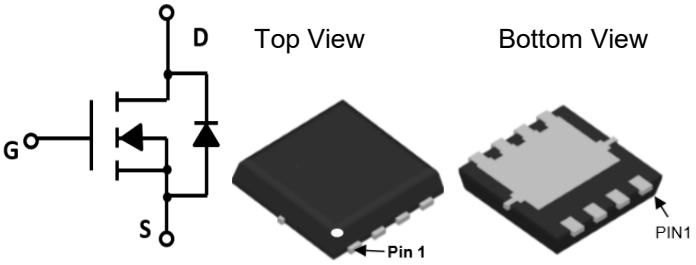
Marking Information



Marking Code = CMN401R0F5

Date Code = XXXX

Equivalent Circuit and Pin Configuration



Ordering Information

Part Number	Packaging	Reel Size
CMN401R0F5	5000/Tape & Reel	13 inch

Absolute Maximum Ratings (T_A=25 ℃ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current[1][6]	T_C=25°C	I_D	212	A
	T_C=100°C		134	A
	T_A=25°C	I_D	29	A
	T_A=100°C		18.5	A
Pulsed Drain Current[3]		I_{DM}	424	A
Total Power Dissipation[4]	T_C=25°C	P_D	113	W
	T_A=25°C		2.2	W
Thermal Resistance Junction-to-Ambient[2][5]		$R_{\theta JA}$	1.1	°C/W
Thermal Resistance Junction-to-Case		$R_{\theta Jc}$	58	°C/W
Junction and Storage Temperature Range		T_J,T_{STG}	-55 to +150	°C

Electrical Characteristics (T_J=25 ℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	40			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V,T_C=25°C			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.0		3.0	V
Static Drain-Source on-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=20A		1.0	1.4	mΩ
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V			1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V,f=100KHz		5840		pF
Output Capacitance	C_{oss}			1920		
Reverse Transfer Capacitance	C_{rss}			90		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=40V,I_D=40A		92		nC
Gate Source Charge	Q_{gs}			17		
Gate Drain Charge	Q_{gd}			18		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=40V, I_D=40A, R_{GEN}=2.0Ω		23.9		ns
Turn-on Rise Time	t_r			17		
Turn-off Delay Time	$t_{D(off)}$			80		
Turn-off Fall Time	t_f			97.5		

Noted: (1) Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

(2) The value of $R_{\theta JA}$ is measured with the device mounted on lin2 FR-4 board with 2oz.Copper,in a still air environment with T_A =25°C.The Power dissipation PDSM is based on $R_{\theta JA}$ t≤10s and the maximum allowed junction temperature of 150°C.The value in any given application depends on the user's specific board design.

(3) Single pulse width limited by junction temperature $T_{J(MAX)}$ = 150°C.

(4) The power dissipation PD is based on $T_{J(MAX)}$ = 150°C,using junction-to-case thermal resistance, and is more useful in setting the upper Dissipation limit for cases where additional heatsinking is used.

(5) The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JA}$ and case to ambient.

(6) The maximum current rating is package limited.

Typical Performance Characteristics

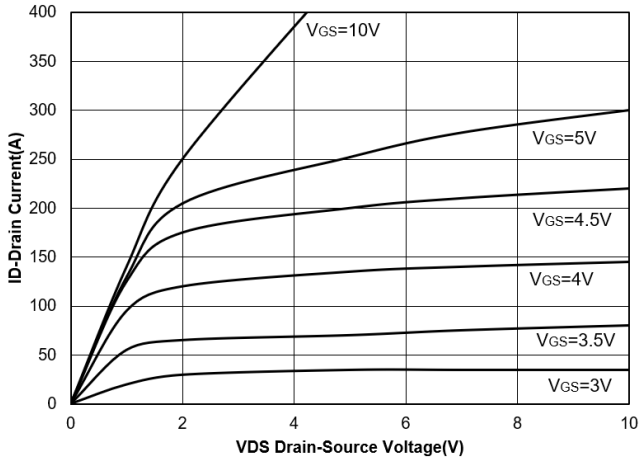


Figure 1. Output Characteristics

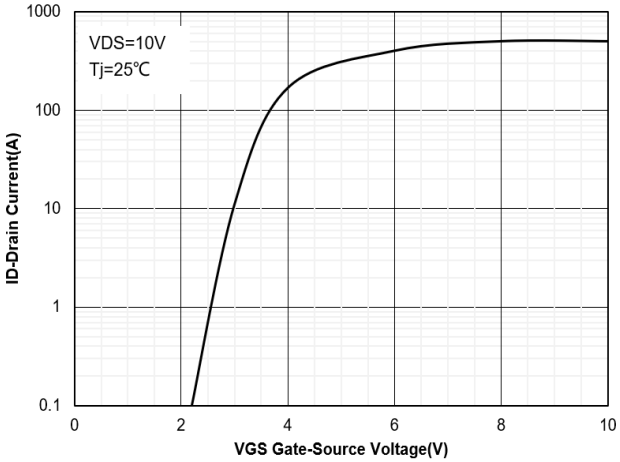


Figure 2. Transfer Characteristics

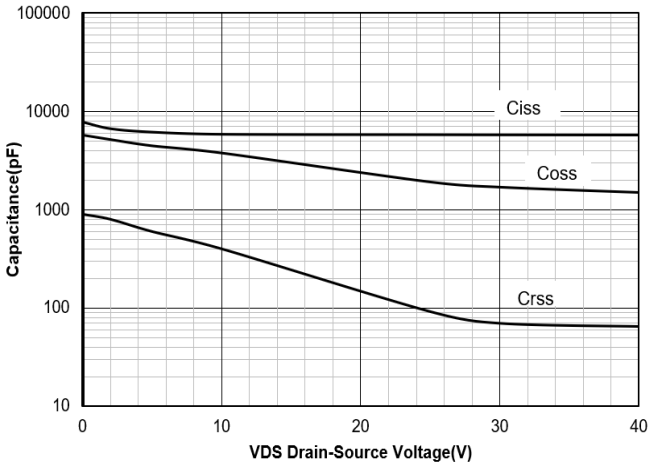


Figure 3. Capacitance Characteristics

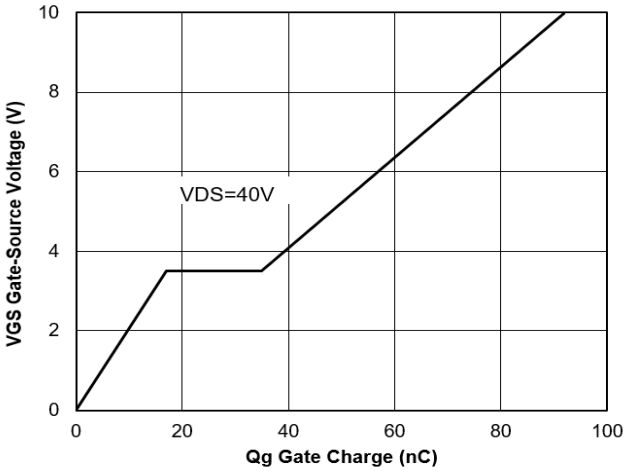


Figure 4. Gate Charge

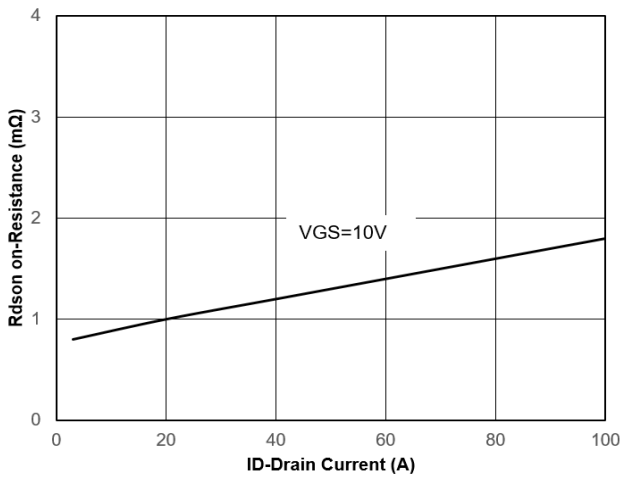


Figure 5. Drain-Source on Resistance

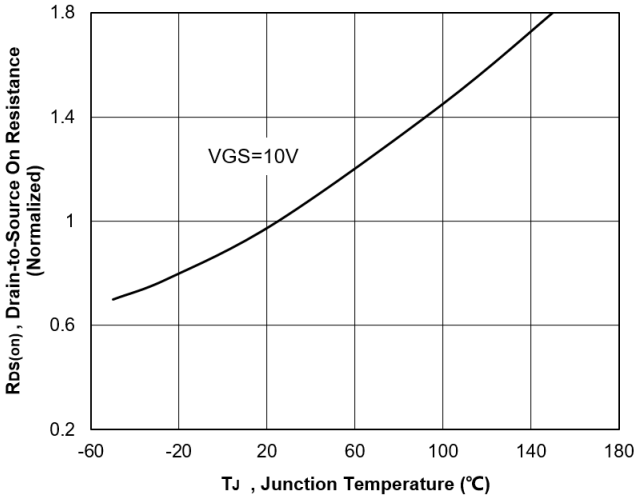


Figure 6. Normalized On-Resistance

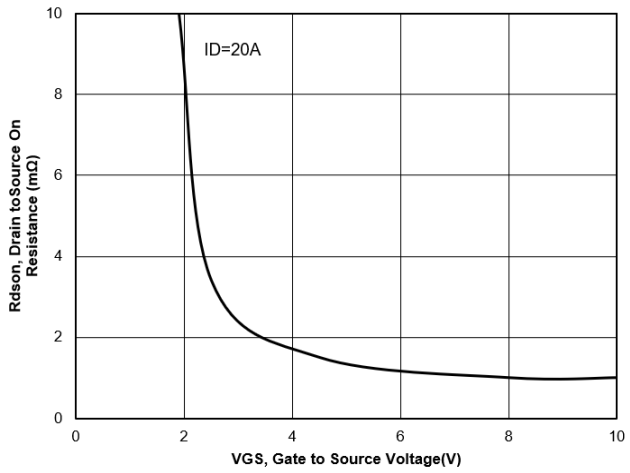


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

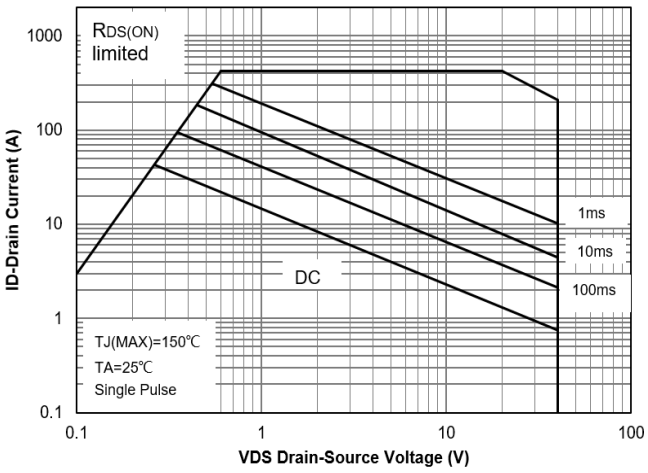


Figure 8. Safe Operation Area

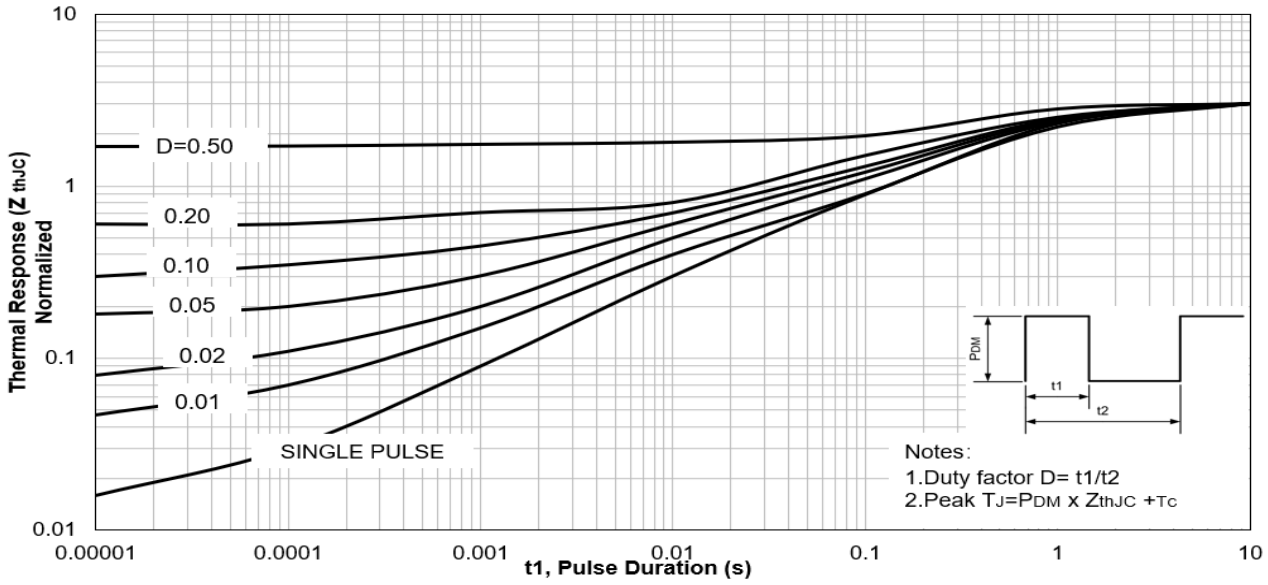


Figure 9. Maximum Effective Transient Thermal Impedance, Junction-to-Case

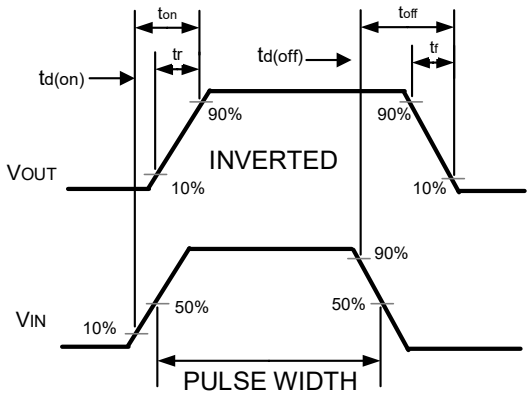
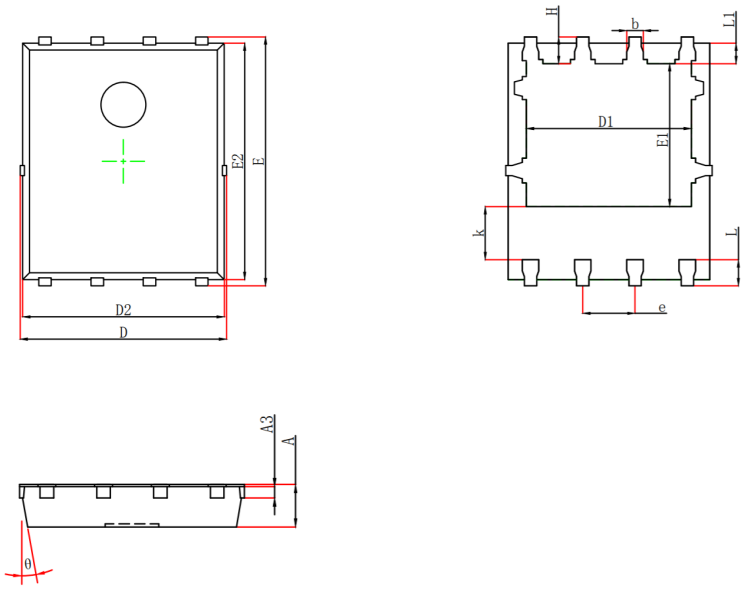


Figure 10. Switching wave

DFN 5X6 Package Outline Drawing



Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0. 900	1.000	0.035	0.039
A3	0.254 REF.		0.010 REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270 TYP.		0.050 TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

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