

## Description

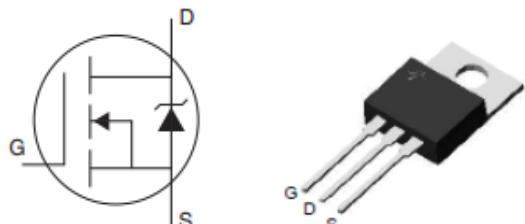
The CMN4004GWP is the N-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

## Features

- V<sub>DS</sub>: 40V
- I<sub>D</sub>: 120A
- R<sub>DS(on)</sub> (@V<sub>GS</sub>=10V) : < 3.3mΩ
- R<sub>DS(on)</sub> (@V<sub>GS</sub>=4.5V) : < 5.2mΩ
- High density cell design for extremely low R<sub>DS(on)</sub>
- Excellent on-resistance and DC current capability

## Equivalent Circuit and Pin Configuration

TO-220



## Applications

- Battery management
- Power management
- Load switch

## Marking Information



Marking Code=N4004GWP

Date Code = XXXX

## Ordering Information

P/N	Package Type	Packaging	Remark
CMN4004GWP	TO-220	Tube	ROHS

## Absolute Maximum Ratings (TA=25 °C unless otherwise noted)

Parameter	Symbol	Maximum	Unit	
Drain-source Voltage	V <sub>DS</sub>	40	V	
Gate-source Voltage	V <sub>GS</sub>	±20	V	
Drain Current <sup>(1)(6)</sup>	T <sub>c</sub> =25°C	269	A	
	T <sub>c</sub> =100°C			
	T <sub>c</sub> =25°C (Package Limit)			
Pulsed Drain Current <sup>(3)</sup>	I <sub>DM</sub>	537	A	
Total Power Dissipation <sup>(4)</sup>	T <sub>c</sub> =25°C	P <sub>D</sub>	417	W
		Derating Factor	2.8	W/°C
Thermal Resistance Junction-to-Case	R <sub>θJC</sub>	0.36	°C/W	
Junction and Storage Temperature Range	T <sub>J,TSTG</sub>	-55 to +175	°C	

**Electrical Characteristics (T<sub>J</sub>=25 °C unless otherwise noted)**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BVDSS	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	40			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V, T <sub>C</sub> =25°C			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.3		2.5	V
Static Drain-Source on-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =30A		2.5	3.3	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		4	5.2	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =30A, V <sub>GS</sub> =0V		0.8	1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				120	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz		2390		pF
Output Capacitance	C <sub>oss</sub>			395		
Reverse Transfer Capacitance	C <sub>rss</sub>			378		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =32V, I <sub>D</sub> =20A		62		nC
Gate Source Charge	Q <sub>gs</sub>			5.8		
Gate Drain Charge	Q <sub>gd</sub>			24.5		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =32V, I <sub>D</sub> =20A, R <sub>GEN</sub> =3Ω		51		ns
Turn-on Rise Time	t <sub>r</sub>			39		
Turn-off Delay Time	t <sub>D(off)</sub>			108		
Turn-off Fall Time	t <sub>f</sub>			52		

Noted: (1) Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

- (2) The value of R<sub>θJA</sub> is measured with the device mounted on lin2 FR-4 board with 2oz.Copper,in a still air environment with T<sub>A</sub> =25°C.The Power dissipation PDSM is based on R<sub>θJA</sub> t≤10s and the maximum allowed junction temperature of 175°C.The value in any given application depends on the user's specific board design.
- (3) Single pulse width limited by junction temperature T<sub>J(MAX)</sub> = 175°C.
- (4) The power dissipation PD is based on T<sub>J(MAX)</sub> = 175°C,using junction-to-case thermal resistance, and is more useful in setting the upper Dissipation limit for cases where additional heatsinking is used.
- (5) The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJA</sub> and case to ambient.
- (6) Drain current limited by maximum junction temperature.

## Typical Performance Characteristics

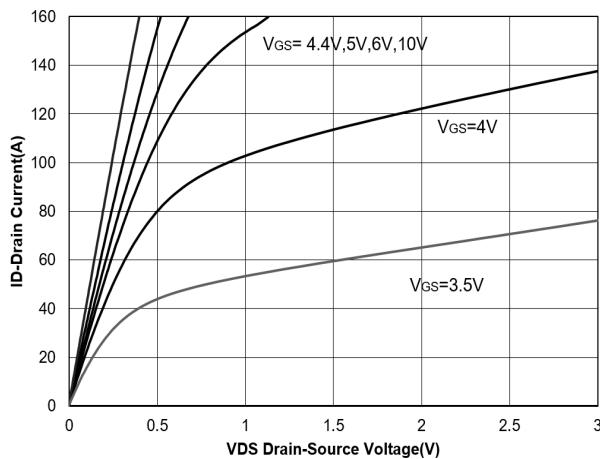


Figure 1. Output Characteristics

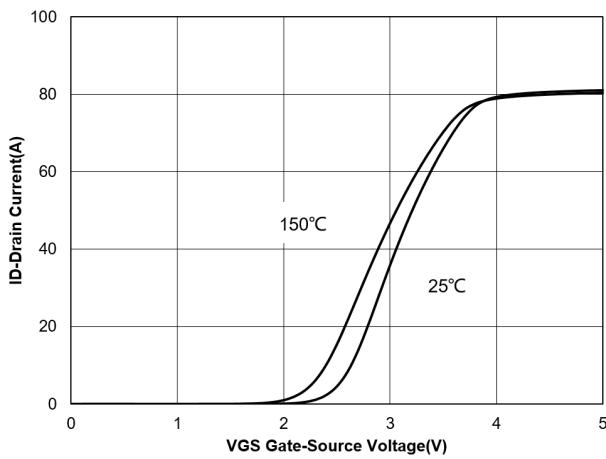


Figure 2. Transfer Characteristics

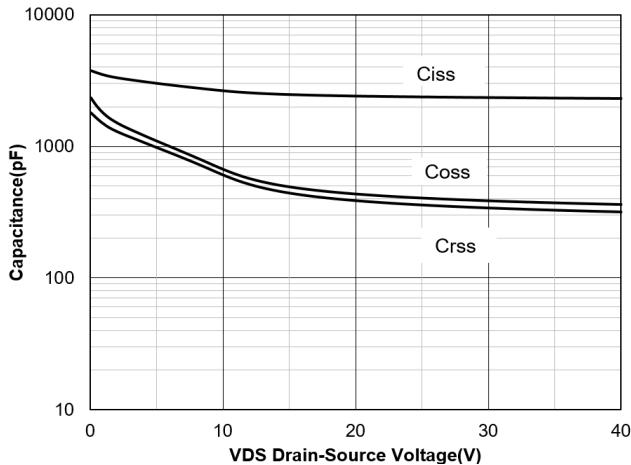


Figure 3. Capacitance Characteristics

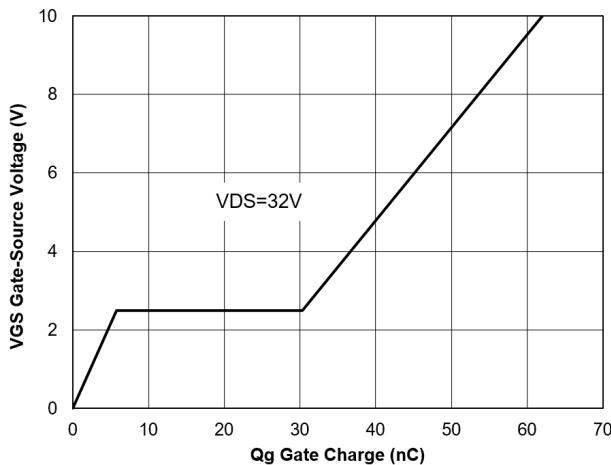


Figure 4. Gate Charge

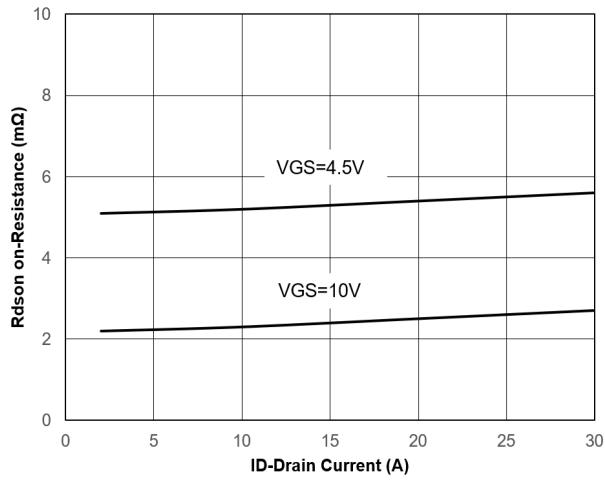


Figure 5. Drain-Source on Resistance

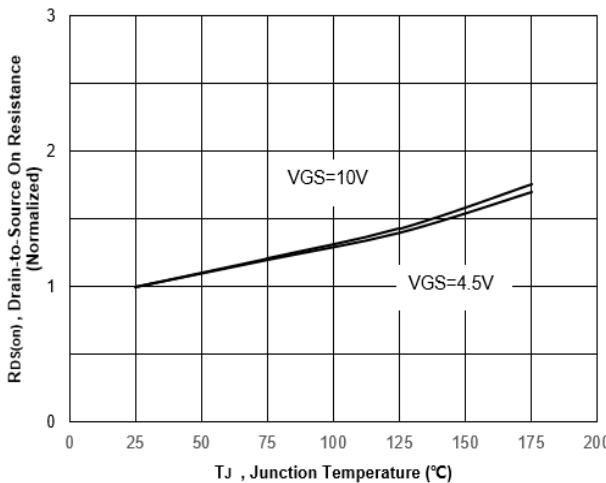


Figure 6. Normalized On-Resistance Vs. Temperature

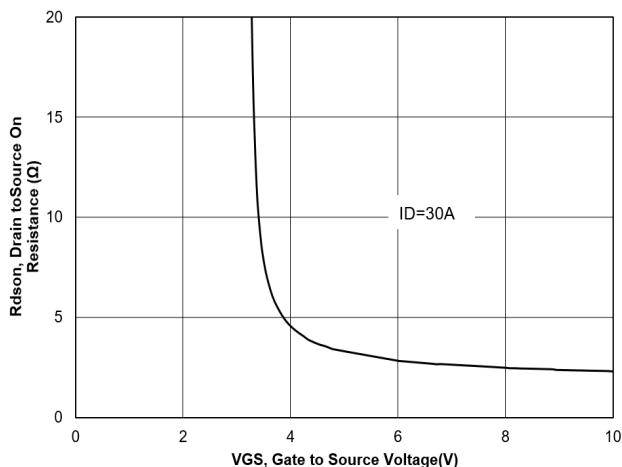


Figure 7. Typical Drain to Source ON Resistance  
VS Gate Voltage and Drain Current

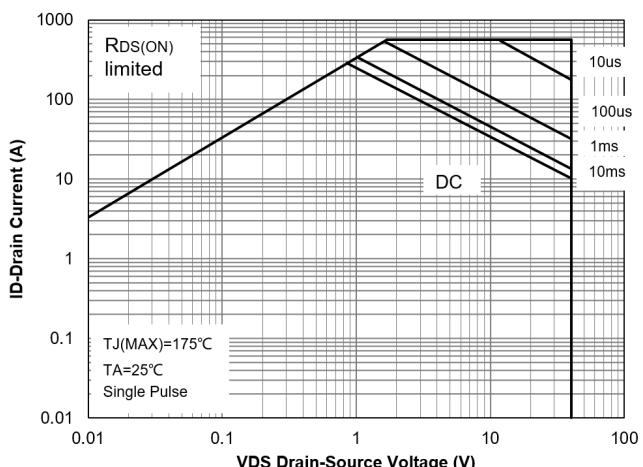


Figure 8. Safe Operation Area

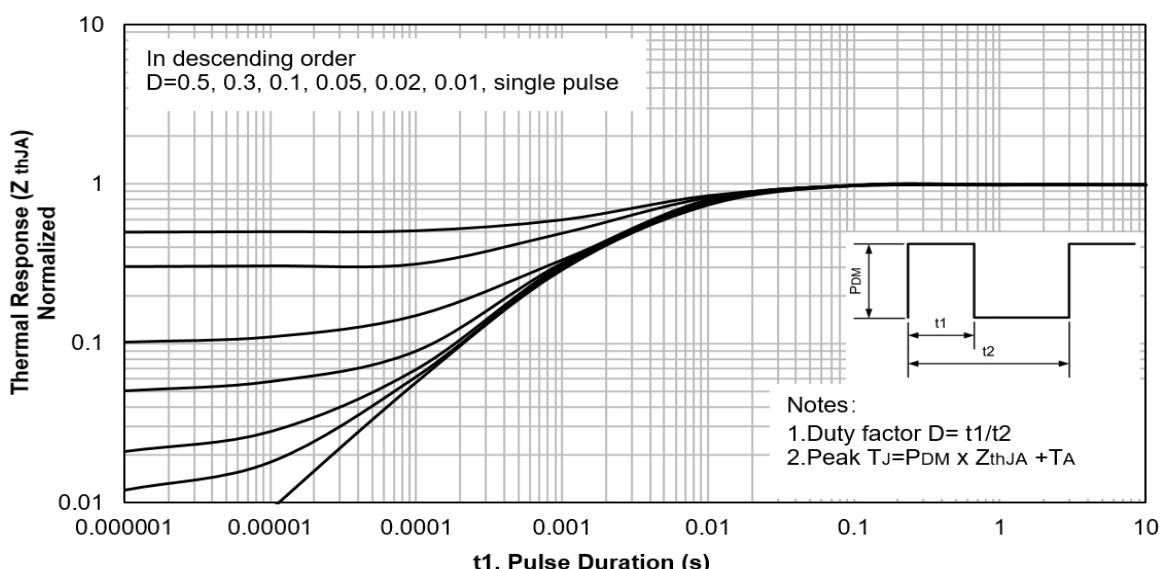


Figure 9. Maximum Effective Transient Thermal Impedance, Junction-to-Case

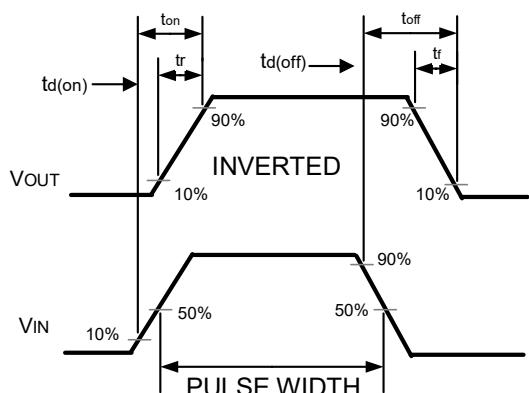
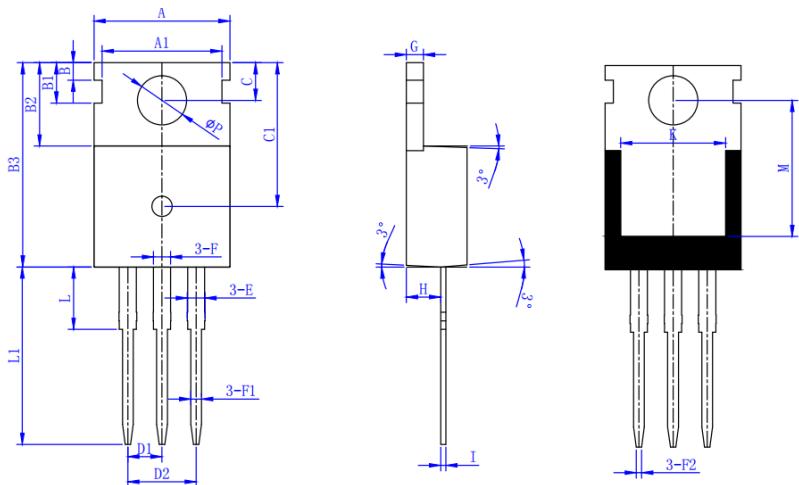


Figure 10. Switching wave

## TO-220 Package Outline Drawing



SYMBOL	MM		
	MIN	NOM	MAX
A	9.90	10.00	10.10
A1		8.70	
B		1.30	
B1		3.00	
B2		6.48	
B3	15.60	15.78	16.00
C		2.80	
C1		11.08	
D1		2.54BSC	
D2		5.08BSC	
E	1.27	1.30	1.35
F	1.15	1.25	1.35
F1	0.70	0.80	0.90
F2	0.30	0.40	0.50
G	1.25	1.30	1.35
H	2.30	2.50	2.70
I	0.45	0.50	0.60
J	4.40	4.50	4.60
K	7.50	7.60	7.70
L	2.68	2.88	3.08
L1	12.95	13.00	13.15
M		10.50	
N	9.40	9.50	9.65
φP	3.60	3.65	3.70

## Contact Information

Applied Power Microelectronics Inc.

Website: <http://www.appliedpowermicro.com>

Email: [sales@appliedpowermicro.com](mailto:sales@appliedpowermicro.com)

Phone: +86 (0519) 8399 3606