Description

The CMN3026S8D is the N-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

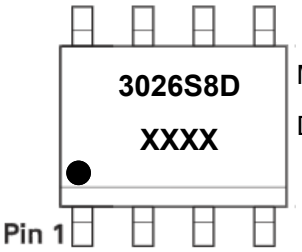
Applications

- Cellular Handsets and Accessories
- Personal Digital Assistants
- Portable Instrumentation
- Load switch

Features

- V_{DS}: 30V
- I_D: 5.8A
- $R_{DS_{ON}}$ (@V_{GS}= 10V) : < 35mΩ
- $R_{DS_{ON}}$ (@V_{GS}= 4.5V) : < 53mΩ
- High density cell design for extremely low $R_{DS_{ON}}$
- Excellent on-resistance and DC current capability

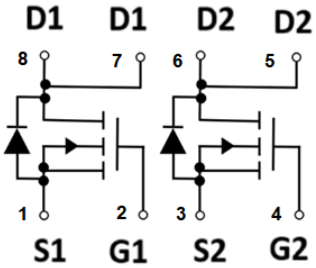
Marking Information



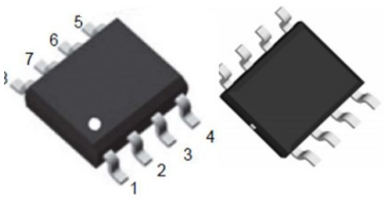
Marking Code = 3026S8D

Date Code = XXXX

Equivalent Circuit and Pin Configuration



SO-8



Ordering Information

Part Number	Packaging	Reel Size
CMN3026S8D	2500/Tape & Reel	13 inch

Absolute Maximum Ratings (T_A=25 ˚C unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A=25°C	I_D	5.8	A
	T_A=70°C		4.6	A
Pulsed Drain Current [1]		I_{DM}	23.2	A
Total Power Dissipation @ T_A=25°C [2]		P_D	2	W
Thermal Resistance Junction-to-Ambient [2]		$R_{\theta JA}$	62.5	°C/W
Junction and Storage Temperature Range		T_J,T_{STG}	-55 to +150	°C

Electrical Characteristics (T_J=25 ℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V,V_{GS}=0V,T_C=25°C			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.0		3.0	V
Static Drain-Source on-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=5.6A		28	35	mΩ
		V_{GS}=4.5V,I_D=5A		41	53	
Diode Forward Voltage	V_{SD}	I_S=5.8A,V_{GS}=0V		0.9	1.2	V
Maximum Body-Diode Continuous Current	I_S				5.8	A
Dynamic Parameters						
Input Capacitance	C_{iss}	VDS=15V,VGS=0V,f=1MHz		290		pF
Output Capacitance	C_{oss}			40		
Reverse Transfer Capacitance	C_{rss}			29		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=15V,I_D=4.7A		6.3		nC
Gate Source Charge	Q_{gs}			0.8		
Gate Drain Charge	Q_{gd}			1.5		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=4.5V,V_{DD}=15V, R_{GEN}=6Ω,R_L=4.7Ω		11		ns
Turn-on Rise Time	t_r			48		
Turn-off Delay Time	$t_{D(off)}$			14		
Turn-off Fall Time	t_f			9		

Noted: (1) Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

(2) Device mounted on FR-4 PCB , 1 inch x 0.85 inch x 0.062 inch with 2oz. Copper , t≤10s.

Typical Performance Characteristics

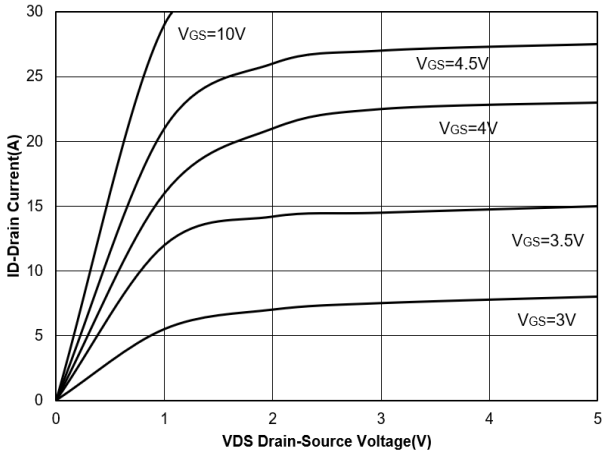


Figure 1. Output Characteristics

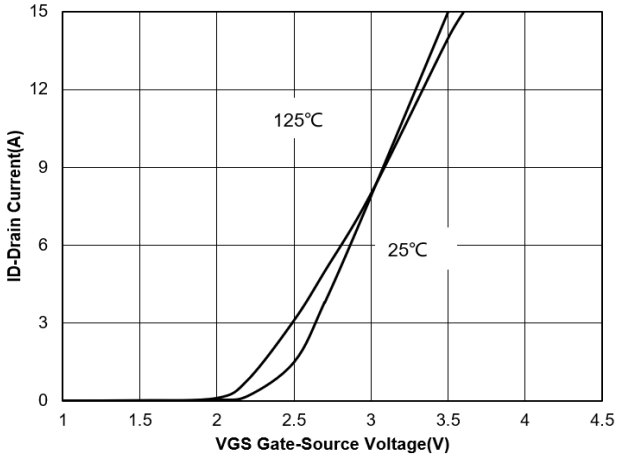


Figure 2. Transfer Characteristics

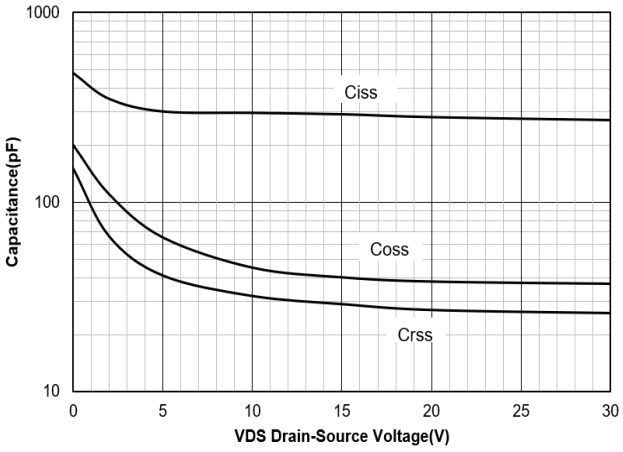


Figure 3. Capacitance Characteristics

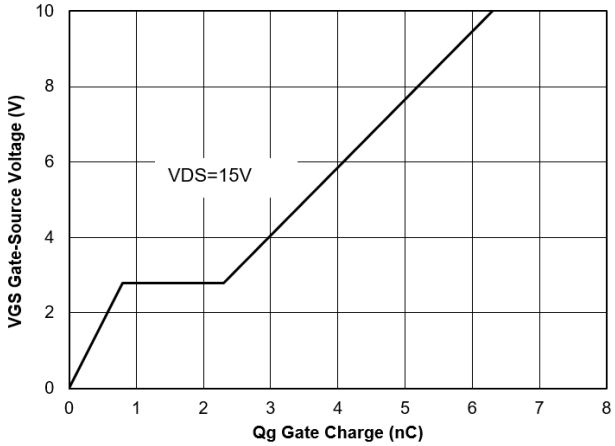


Figure 4. Gate Charge

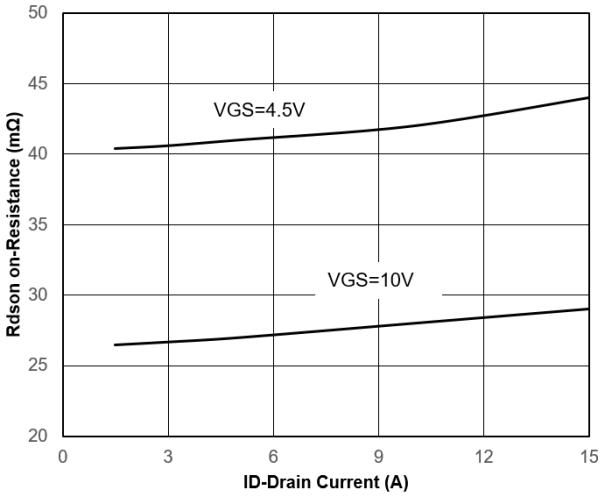


Figure 5. Drain-Source on Resistance

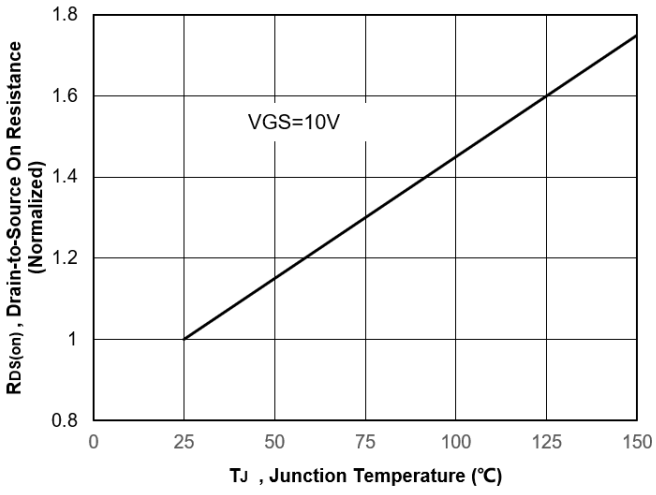


Figure 6. Normalized On-Resistance Vs. Temperature

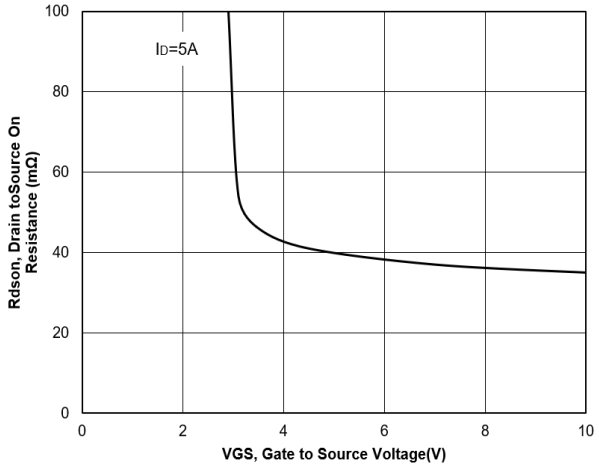


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

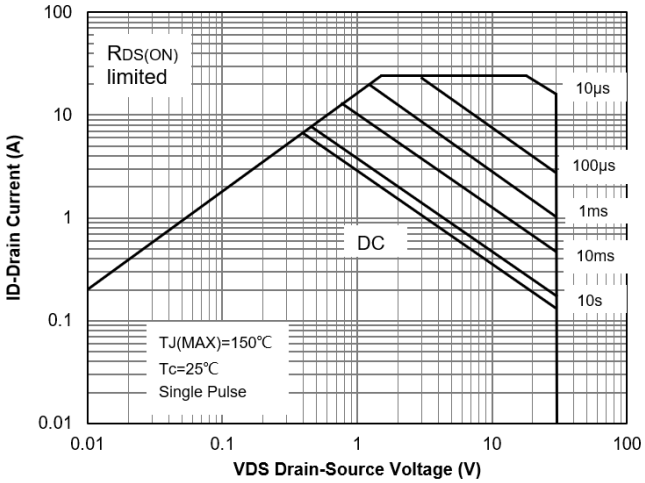


Figure 8. Safe Operation Area

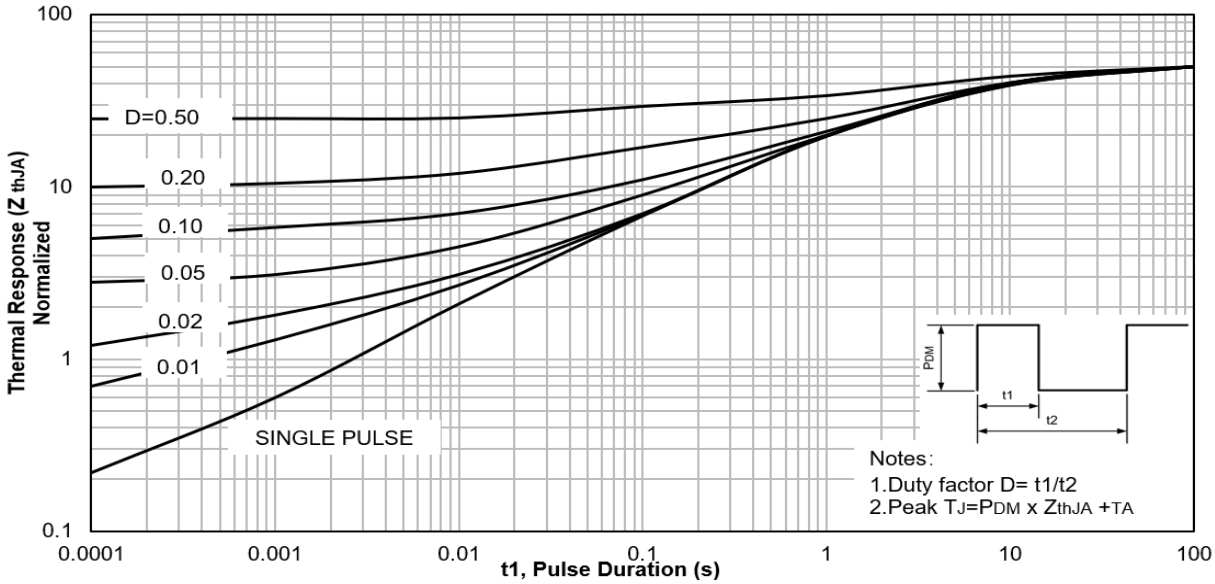


Figure 9. Maximum Effective Transient Thermal Impedance,Junction-to-Ambient

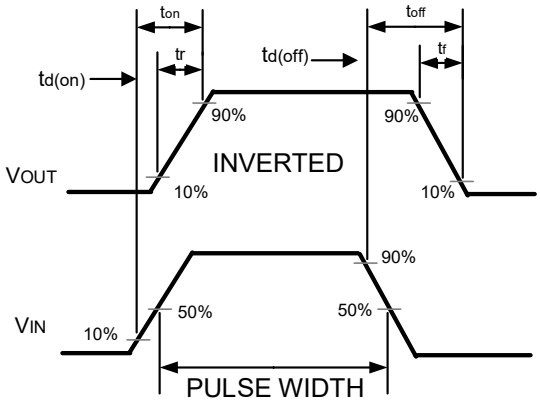
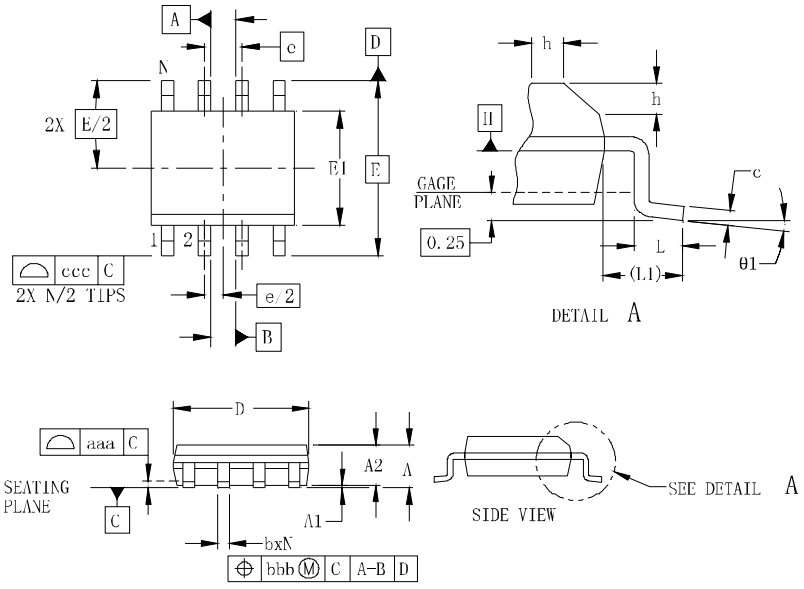


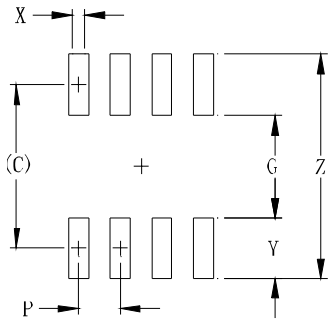
Figure 10. Switching wave

SO-8 Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.25		1.65	0.049		0.065
b	0.31		0.51	0.012		0.020
c	0.17		0.25	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E1	3.80	3.90	4.00	0.150	0.154	0.157
E	6.00 BSC			0.236 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25		0.50	0.010		0.020
L	0.40	0.72	1.04	0.016	0.028	0.041
L1	(1.04)			(0.041)		
N	8			8		
θ1	0°		8°	0°		8°
aaa	0.10			0.004		
bbb	0.25			0.010		
ccc	0.20			0.008		

Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
C	5.20	0.205
G	3.00	0.118
P	1.27	0.050
X	0.60	0.024
Y	2.20	0.087
Z	7.40	0.291