

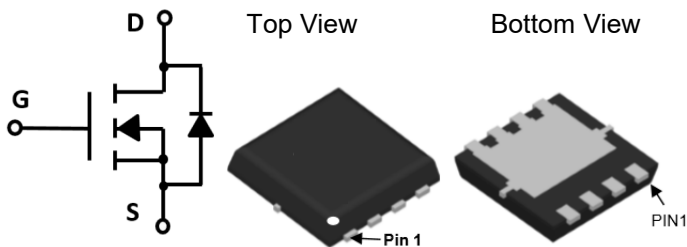
Description

The CMN3005SF5 is the N-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

Features

- V_{DS} : 30V
- I_D : 66A
- $R_{DS(on)}$ (@ $V_{GS}=10V$): < 4.8m Ω
- $R_{DS(on)}$ (@ $V_{GS}=4.5V$): < 7m Ω
- High density cell design for extremely low $R_{DS(on)}$
- Excellent on-resistance and DC current capability

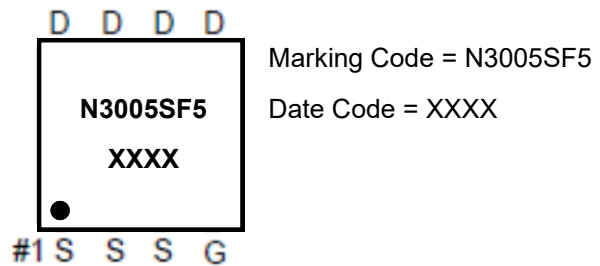
Equivalent Circuit and Pin Configuration



Applications

- Battery management
- Power management
- Load switch

Marking Information



Ordering Information

| Part Number | Packaging | Reel Size |
|-------------|------------------|-----------|
| CMN3005SF5 | 5000/Tape & Reel | 13 inch |

Absolute Maximum Ratings (TA=25 °C unless otherwise noted)

| Parameter | Symbol | Maximum | Unit | |
|--|-----------------|-------------|------|---|
| Drain-source Voltage | V_{DS} | 30 | V | |
| Gate-source Voltage | V_{GS} | ± 20 | V | |
| Drain Current ⁽¹⁾⁽⁶⁾ | I_D | TC=25°C | 66 | A |
| | | TC=100°C | 41 | A |
| | I_D | TA=25°C | 29 | A |
| | | TA=100°C | 13 | A |
| Pulsed Drain Current ⁽³⁾ | I_{DM} | 132 | A | |
| Total Power Dissipation ⁽⁴⁾ | PD | TC=25°C | 31 | W |
| | | TA=25°C | 6.3 | W |
| Thermal Resistance Junction-to-Ambient ⁽²⁾⁽⁵⁾ | $R_{\theta JA}$ | 20 | °C/W | |
| Thermal Resistance Junction-to-Case | $R_{\theta Jc}$ | 4 | °C/W | |
| Junction and Storage Temperature Range | T_J, T_{STG} | -55 to +150 | °C | |

Electrical Characteristics (T_J=25 °C unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---------------------------------------|---------------------|--|-----|------|------|-------|
| Static Parameter | | | | | | |
| Drain-Source Breakdown Voltage | BV _{DSS} | V _{GS} =0V, I _D =250μA | 30 | | | V |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} =30V, V _{GS} =0V, T _C =25°C | | | 1 | μA |
| Gate-Body Leakage Current | I _{GSS} | V _{GS} =±20V, V _{DS} =0V | | | ±100 | nA |
| Gate Threshold Voltage | V _{GS(th)} | V _{DS} =V _{GS} , I _D =250μA | 1.0 | | 2.5 | V |
| Static Drain-Source on-Resistance | R _{DS(on)} | V _{GS} =10V, I _D =20A | | 3.9 | 4.8 | mΩ |
| | | V _{GS} =4.5V, I _D =16A | | 5.4 | 7.0 | |
| Diode Forward Voltage | V _{SD} | I _S =20A, V _{GS} =0V | | 0.9 | 1.2 | V |
| Maximum Body-Diode Continuous Current | I _S | | | | 66 | A |
| Dynamic Parameters | | | | | | |
| Input Capacitance | C _{iss} | V _{DS} =15V, V _{GS} =0V, f=1MHz | | 2040 | | pF |
| Output Capacitance | C _{oss} | | | 249 | | |
| Reverse Transfer Capacitance | C _{rss} | | | 222 | | |
| Switching Parameters | | | | | | |
| Total Gate Charge | Q _g | V _{GS} =10V, V _{DS} =15V, I _D =20A | | 39.6 | | nC |
| Gate Source Charge | Q _{gs} | | | 5.27 | | |
| Gate Drain Charge | Q _{gd} | | | 8.34 | | |
| Turn-on Delay Time | t _{D(on)} | V _{GS} =10V, V _{DD} =15V, R _L =0.75Ω, R _{GEN} =3Ω | | 20 | | ns |
| Turn-on Rise Time | t _r | | | 9.6 | | |
| Turn-off Delay Time | t _{D(off)} | | | 59 | | |
| Turn-off Fall Time | t _f | | | 18.4 | | |

Noted: (1) Pulse Test: Pulse Width ≤ 300μs, Duty cycle ≤ 2%.

- (2) The value of R_{θJA} is measured with the device mounted on lin2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C. The Power dissipation PDSM is based on R_{θJA} t ≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
- (3) Single pulse width limited by junction temperature T_{J(MAX)} = 150°C.
- (4) The power dissipation PD is based on T_{J(MAX)} = 150°C, using junction-to-case thermal resistance, and is more useful in setting the upper Dissipation limit for cases where additional heatsinking is used.
- (5) The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJA} and case to ambient.
- (6) The maximum current rating is package limited.

Typical Performance Characteristics

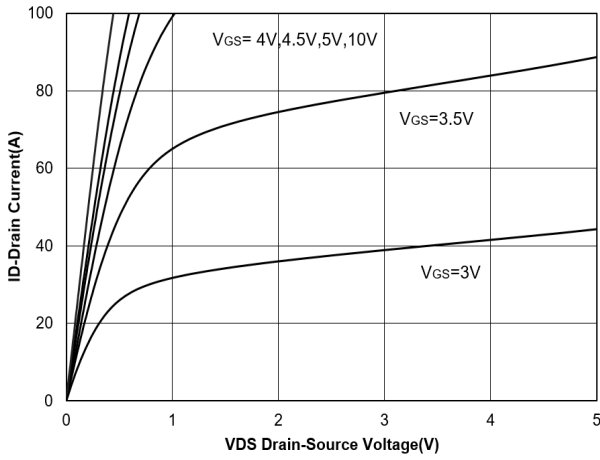


Figure 1. Output Characteristics

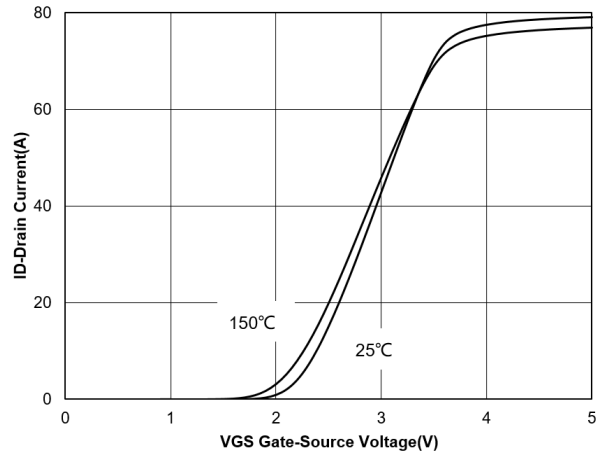


Figure 2. Transfer Characteristics

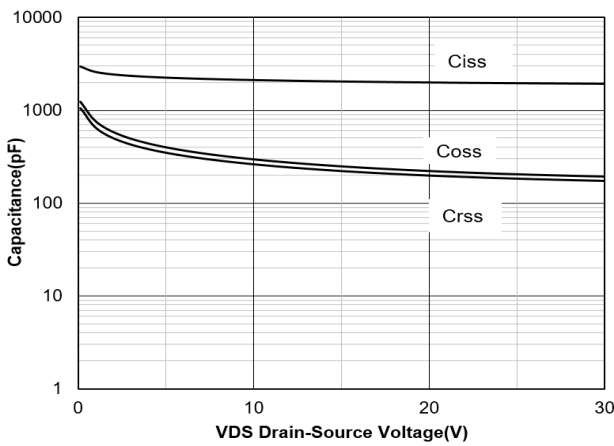


Figure 3. Capacitance Characteristics

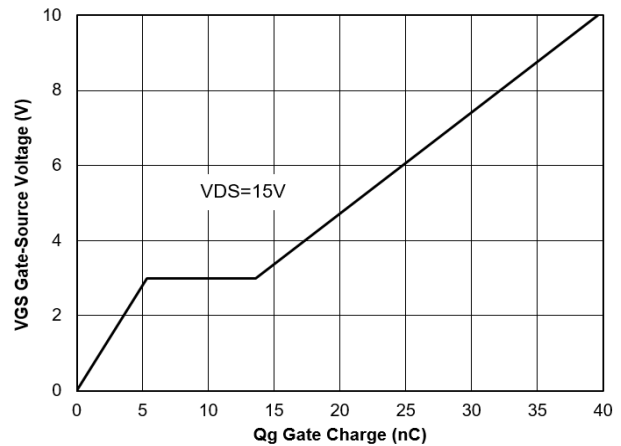


Figure 4. Gate Charge

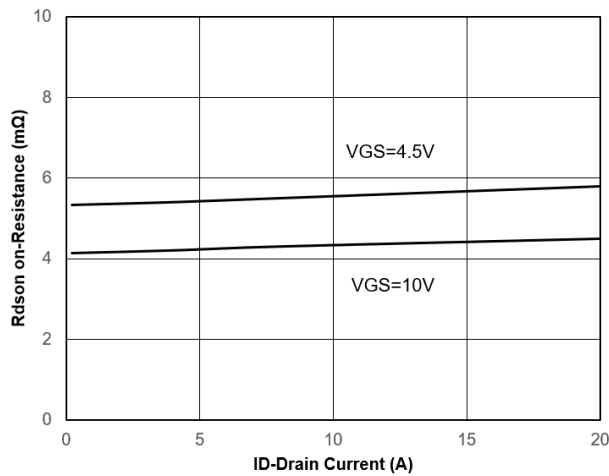


Figure 5. Drain-Source on Resistance

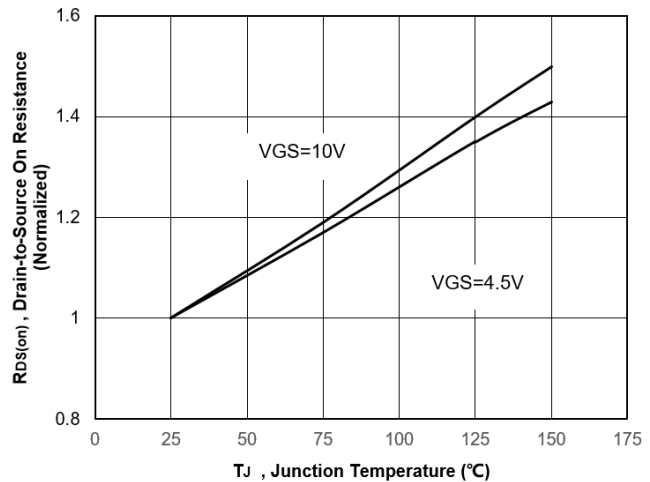


Figure 6. Normalized On-Resistance Vs. Temperature

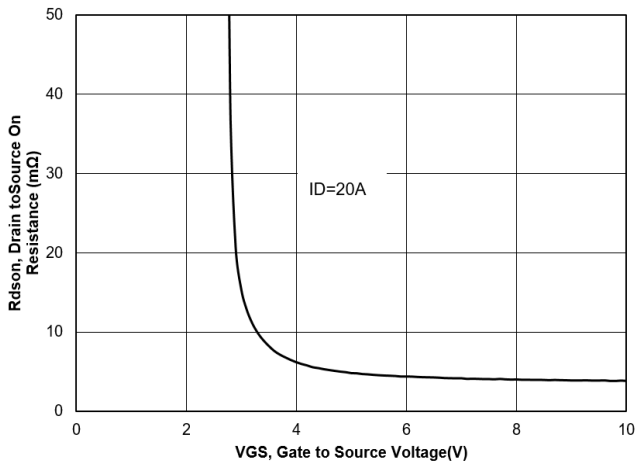


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

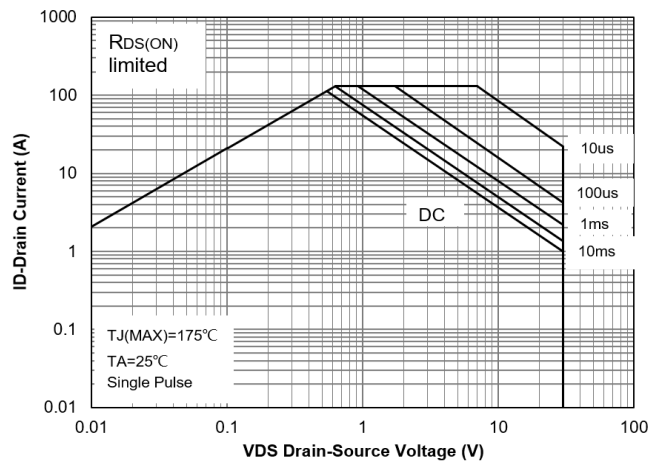


Figure 8. Safe Operation Area

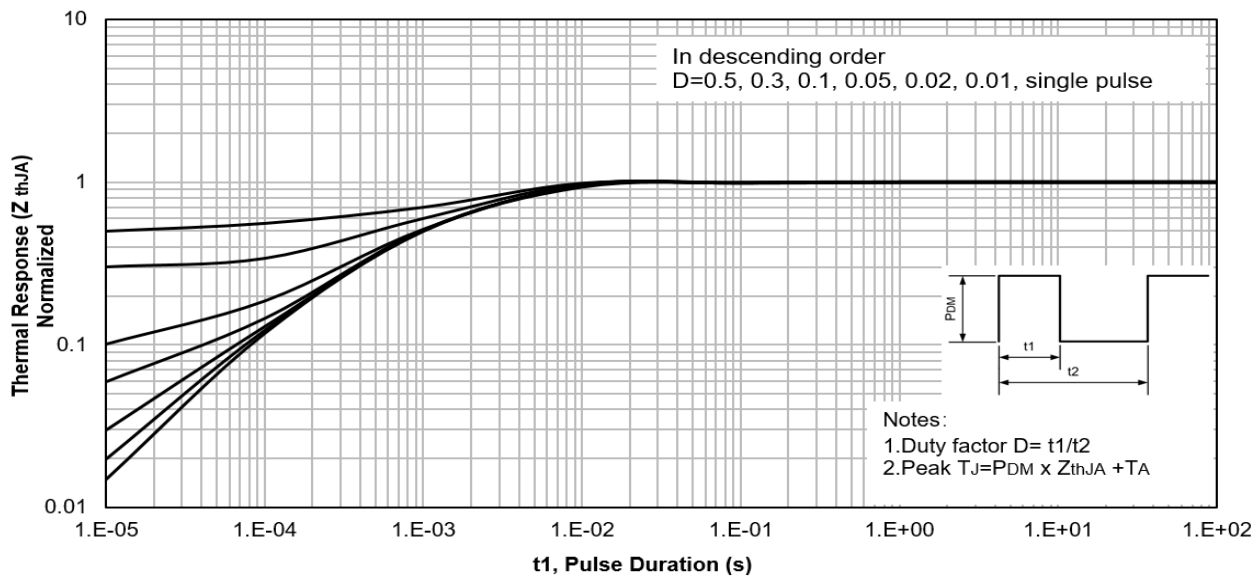


Figure 9. Maximum Effective Transient Thermal Impedance, Junction-to-Case

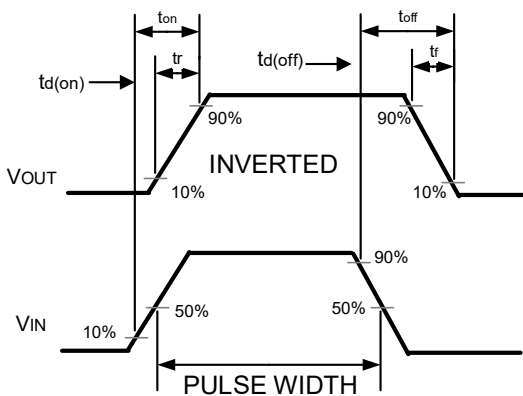
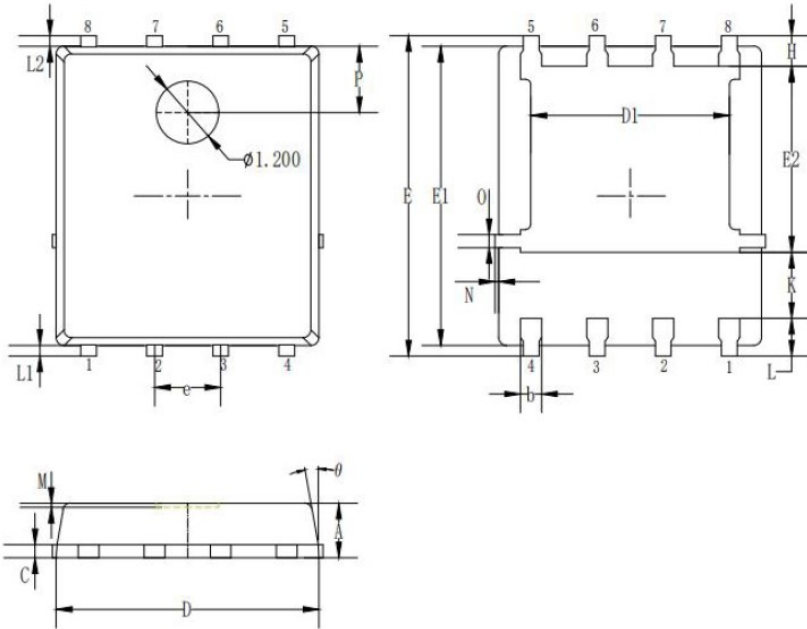


Figure 10. Switching wave

DFN 5x6 Package Outline Drawing



| Symbol | Millimeters | | |
|----------|-------------|------|------|
| | Min. | Nom. | Max. |
| A | 0.90 | 1.05 | 1.20 |
| b | 0.35 | 0.40 | 0.50 |
| c | 0.20 | 0.25 | 0.35 |
| D | 4.90 | 5.05 | 5.20 |
| D1 | 3.72 | 3.82 | 3.92 |
| E | 6.00 | 6.15 | 6.30 |
| E1 | 5.60 | 5.75 | 5.90 |
| E2 | 3.47 | 3.57 | 3.67 |
| e | 1.27 BSC | | |
| H | 0.48 | 0.58 | 0.68 |
| K | 1.17 | 1.27 | 1.37 |
| L | 0.64 | 0.74 | 0.84 |
| L1/L2 | 0.20 REF | | |
| θ | 8° | 10° | 12° |
| M | 0.08 REF | | |
| N | 0 | -- | 0.15 |
| O | 0.25 REF | | |
| P | 1.28 REF | | |

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