

## Description

The CMN3004XF3 is the N-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

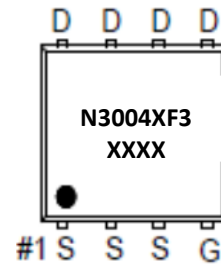
## Features

- $V_{DS}$ : 30V
- $I_D$ : 67A
- $R_{DS(on)}$  (@ $V_{GS}=10V$ ): < 3.7m $\Omega$
- $R_{DS(on)}$  (@ $V_{GS}=4.5V$ ): < 5.0m $\Omega$
- High density cell design for extremely low  $R_{DS(on)}$
- Excellent on-resistance and DC current capability

## Applications

- Battery management
- Power management
- Load switch

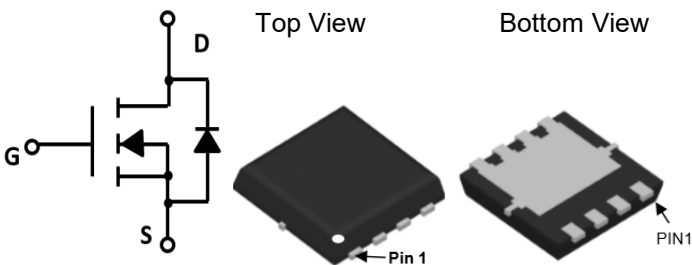
## Marking Information



Marking Code=N3004XF3

Date Code = XXXX

## Equivalent Circuit and Pin Configuration



## Ordering Information

P/N	Package Type	Packaging
CMN3004XF3	5000/Tape & Reel	13 inch

## Absolute Maximum Ratings (TA=25 °C unless otherwise noted)

Parameter	Symbol	Maximum	Unit	
Drain-source Voltage	$V_{DS}$	30	V	
Gate-source Voltage	$V_{GS}$	$\pm 20$	V	
Drain Current <sup>(1)(6)</sup>	$I_D$	TC=25°C	67	A
		TC=100°C	42	A
	$I_D$	TA=25°C	23	A
		TA=100°C	14	A
Pulsed Drain Current <sup>(3)</sup>	$I_{DM}$	133	A	
Total Power Dissipation <sup>(4)</sup>	PD	TC=25°C	27	W
		TA=25°C	3.1	W
Thermal Resistance Junction-to-Ambient <sup>(2)(5)</sup>	$R_{\theta JA}$	40	°C/W	
Thermal Resistance Junction-to-Case	$R_{\theta Jc}$	4.6	°C/W	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	°C	

**Electrical Characteristics (T<sub>J</sub>=25 °C unless otherwise noted)**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BVDSS	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, T <sub>C</sub> =25°C			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0		2.5	V
Static Drain-Source on-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A		3.1	3.7	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =15A		3.8	5.0	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V		0.9	1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				67	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, f=1MHz		3200		pF
Output Capacitance	C <sub>oss</sub>			385		
Reverse Transfer Capacitance	C <sub>rss</sub>			381		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =20V, I <sub>D</sub> =20A		79		nC
Gate Source Charge	Q <sub>gs</sub>			7.6		
Gate Drain Charge	Q <sub>gd</sub>			22		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =20V, I <sub>D</sub> =20A, R <sub>GEN</sub> =3Ω		27.8		ns
Turn-on Rise Time	t <sub>r</sub>			12.8		
Turn-off Delay Time	t <sub>D(off)</sub>			96		
Turn-off Fall Time	t <sub>f</sub>			24		

Noted: (1) Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

- (2) The value of R<sub>θJA</sub> is measured with the device mounted on lin2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> = 25°C. The Power dissipation PDSM is based on R<sub>θJA</sub> t ≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
- (3) Single pulse width limited by junction temperature T<sub>J(MAX)</sub> = 150°C.
- (4) The power dissipation PD is based on T<sub>J(MAX)</sub> = 150°C, using junction-to-case thermal resistance, and is more useful in setting the upper Dissipation limit for cases where additional heatsinking is used.
- (5) The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJA</sub> and case to ambient.
- (6) The maximum current rating is package limited.

**Typical Performance Characteristics**

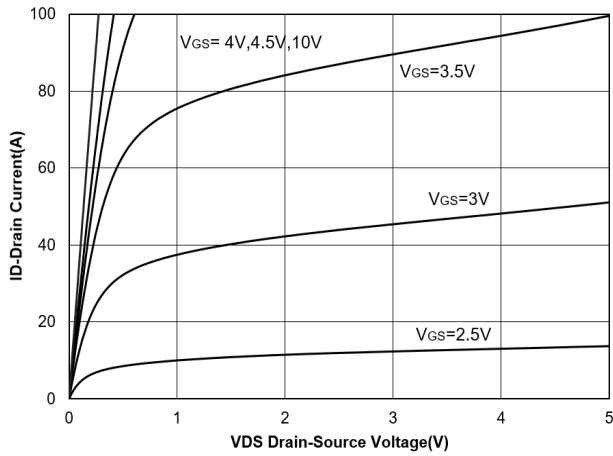


Figure 1. Output Characteristics

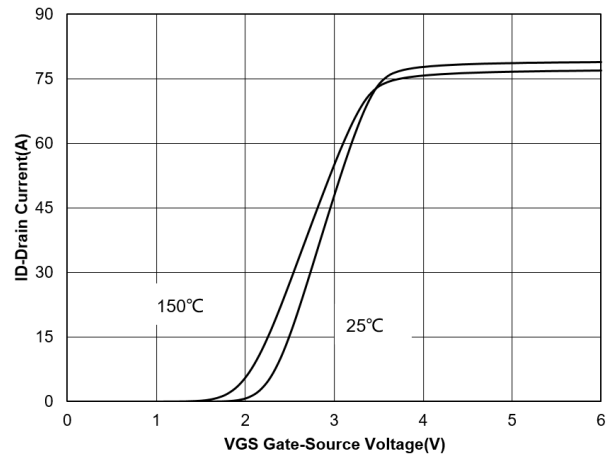


Figure 2. Transfer Characteristics

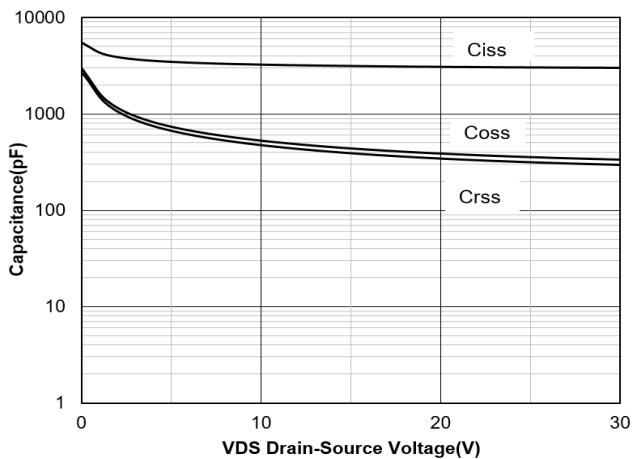


Figure 3. Capacitance Characteristics

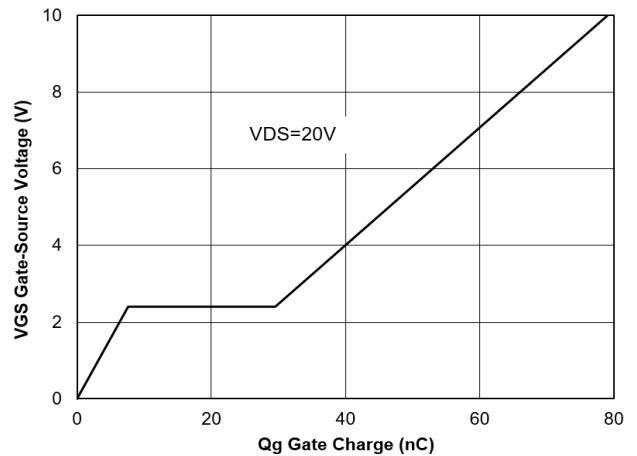


Figure 4. Gate Charge

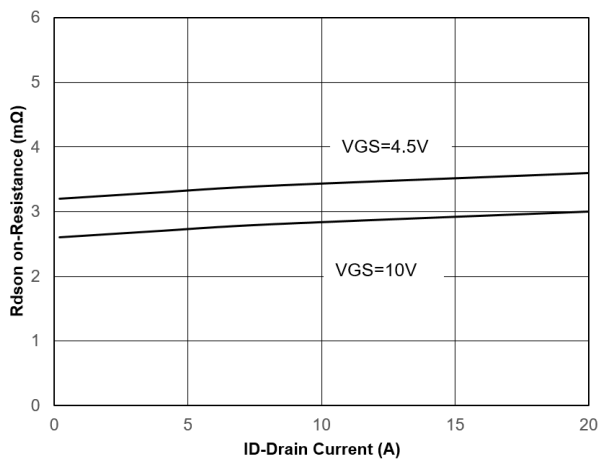


Figure 5. Drain-Source on Resistance

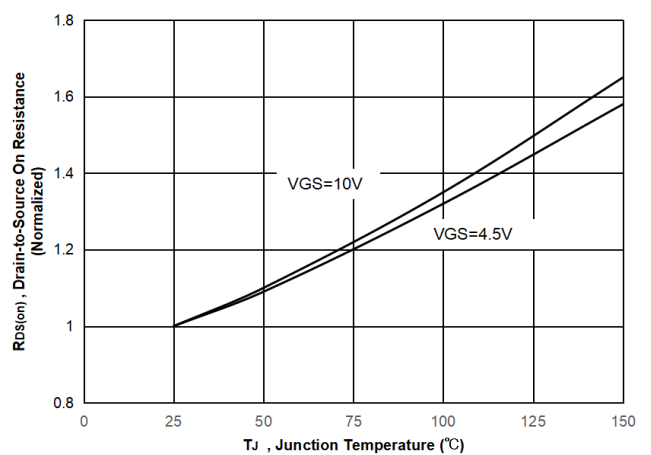


Figure 6. Normalized On-Resistance Vs. Temperature

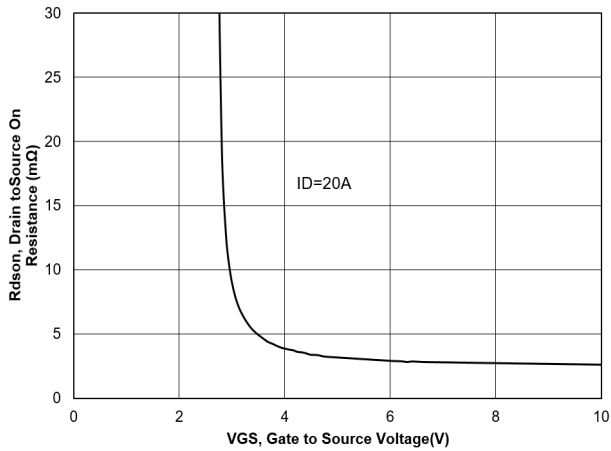


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

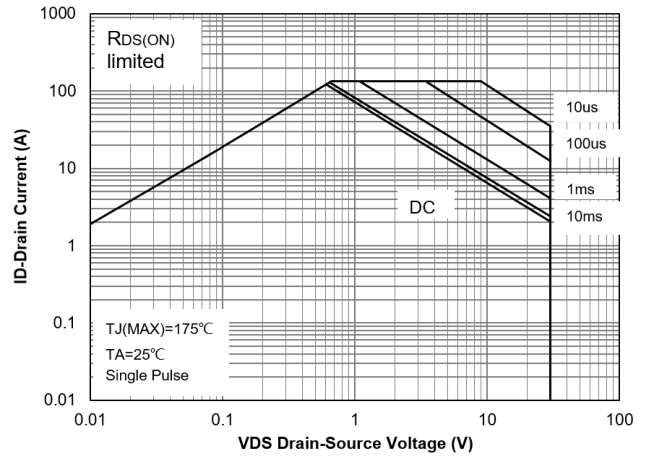


Figure 8. Safe Operation Area

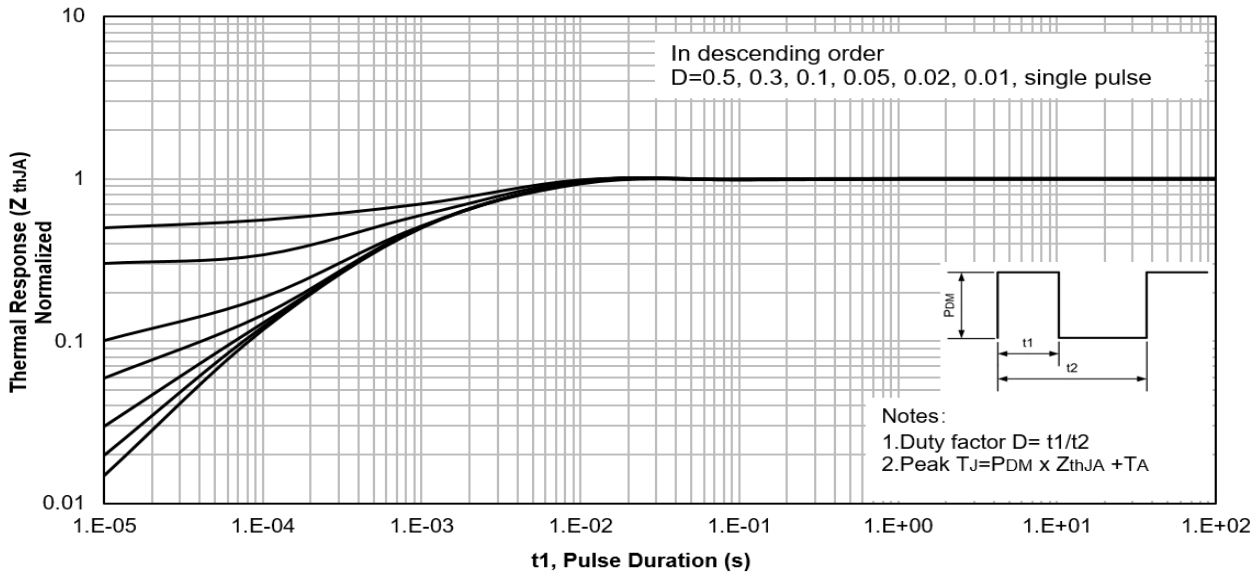


Figure 9. Maximum Effective Transient Thermal Impedance, Junction-to-Case

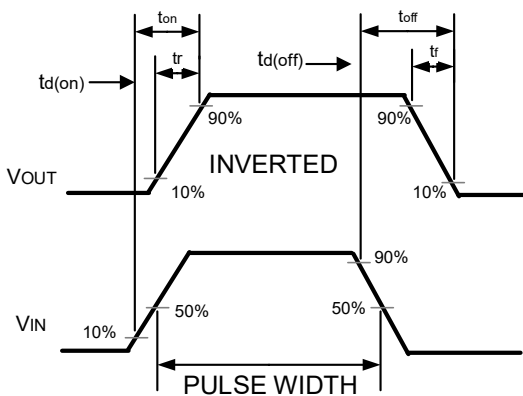
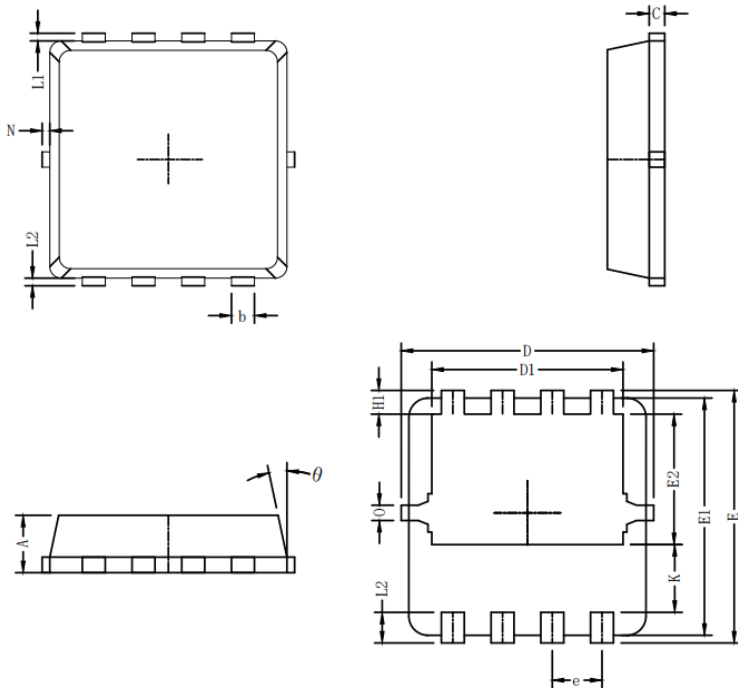


Figure 10. Switching wave

**PDFN 3.3x3.3 Package Outline Drawing**


Symbol	Millimeters		
	Min.	Nom.	Max.
A	0.65	0.75	0.85
b	0.25	0.30	0.35
c	0.15	0.20	0.25
D	3.00	3.10	3.20
D1	2.40	2.50	2.60
E	3.20	3.30	3.40
E1	3.00	3.10	3.20
E2	1.60	1.70	1.80
e	0.65 BSC		
H1	0.21	0.31	0.41
H2	0.30	0.40	0.50
K	0.78	0.88	0.98
L1/L2	0.10 REF		
θ	11°	12°	13°
N	0	—	0.15
O	0.20 REF		

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