

### Description

The CMN3003TF5 is the N-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

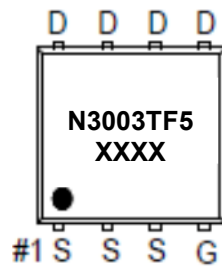
### Features

- V<sub>DS</sub>: 30V
- I<sub>D</sub>: 124A
- R<sub>DS(on)</sub> (@V<sub>GS</sub>=10V) : < 3.0mΩ
- R<sub>DS(on)</sub> (@V<sub>GS</sub>=4.5V) : < 5.5mΩ
- High density cell design for extremely low R<sub>DS(on)</sub>
- Excellent on-resistance and DC current capability

### Applications

- Battery management
- Power management
- Load switch

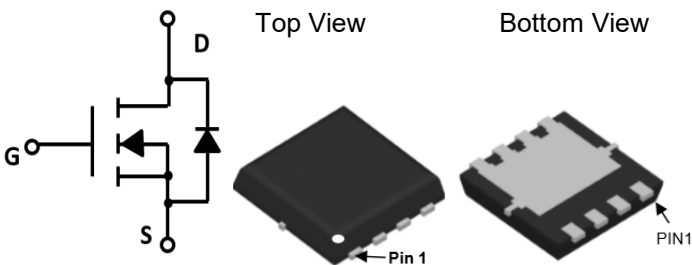
### Marking Information



Marking Code =N3003TF5

Date Code = XXXX

### Equivalent Circuit and Pin Configuration



### Ordering Information

Part Number	Packaging	Reel Size
CMN3003TF5	5000/Tape & Reel	13 inch

### Absolute Maximum Ratings (TA=25 °C unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V <sub>DS</sub>	30	V
Gate-source Voltage		V <sub>GS</sub>	±20	V
Drain Current <sup>(1)(6)</sup>	TC=25°C	I <sub>D</sub>	124	A
	TC=100°C		75	A
	TA=25°C	I <sub>D</sub>	35	A
	TA=100°C		21	A
Pulsed Drain Current <sup>(3)</sup>		I <sub>DM</sub>	248	A
Total Power Dissipation <sup>(4)</sup>	TC=25°C	P <sub>D</sub>	78	W
	TA=25°C		6.3	W
Thermal Resistance Junction-to-Ambient <sup>(2)(5)</sup>		R <sub>θJA</sub>	20	°C/W
Thermal Resistance Junction-to-Case		R <sub>θJC</sub>	1.6	°C/W
Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics (T<sub>J</sub>=25 °C unless otherwise noted)**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BVDSS	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, T <sub>C</sub> =25°C			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1		3	V
Static Drain-Source on-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A		2.5	3.0	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A		4.0	5.5	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V		0.8	1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				124	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz		3700		pF
Output Capacitance	C <sub>oss</sub>			450		
Reverse Transfer Capacitance	C <sub>rss</sub>			390		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =18A		68		nC
Gate Source Charge	Q <sub>gs</sub>			12		
Gate Drain Charge	Q <sub>gd</sub>			16		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =15V, I <sub>D</sub> =10A, R <sub>GEN</sub> =2.7Ω		21		ns
Turn-on Rise Time	t <sub>r</sub>			18.9		
Turn-off Delay Time	t <sub>D(off)</sub>			88		
Turn-off Fall Time	t <sub>f</sub>			30.2		

Noted: (1) Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

- (2) The value of R<sub>θJA</sub> is measured with the device mounted on lin2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> = 25°C. The Power dissipation PDSM is based on R<sub>θJA</sub> t ≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
- (3) Single pulse width limited by junction temperature T<sub>J(MAX)</sub> = 150°C.
- (4) The power dissipation PD is based on T<sub>J(MAX)</sub> = 150°C, using junction-to-case thermal resistance, and is more useful in setting the upper Dissipation limit for cases where additional heatsinking is used.
- (5) The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJA</sub> and case to ambient.
- (6) Drain current limited by maximum junction temperature.

**Typical Performance Characteristics**

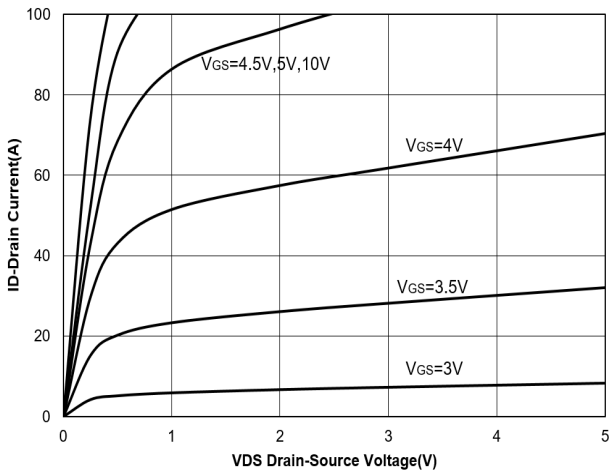


Figure 1. Output Characteristics

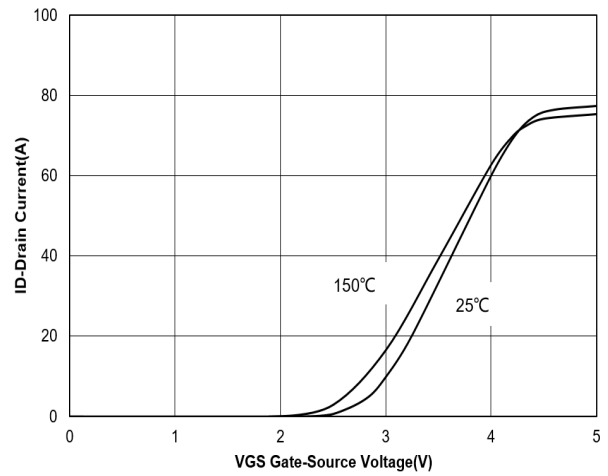


Figure 2. Transfer Characteristics

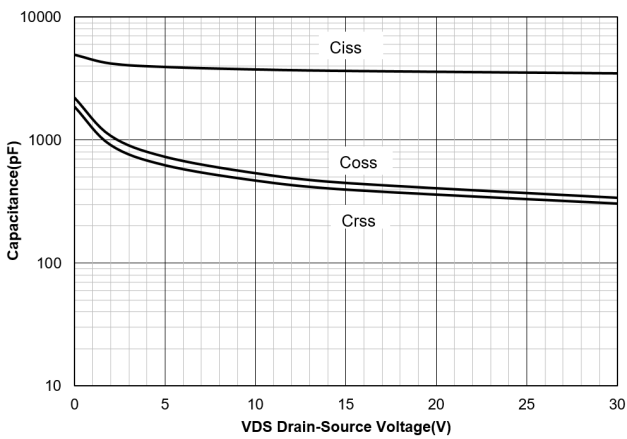


Figure 3. Capacitance Characteristics

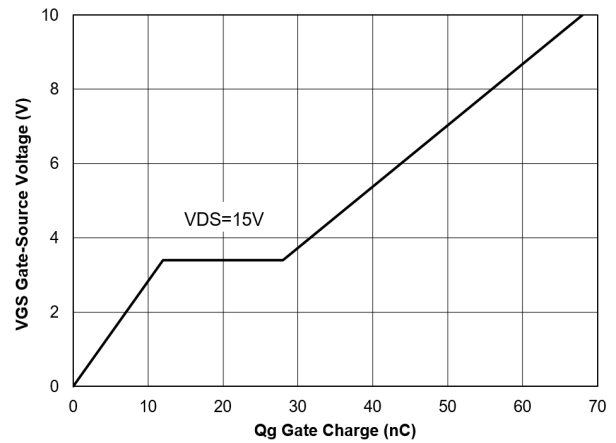


Figure 4. Gate Charge

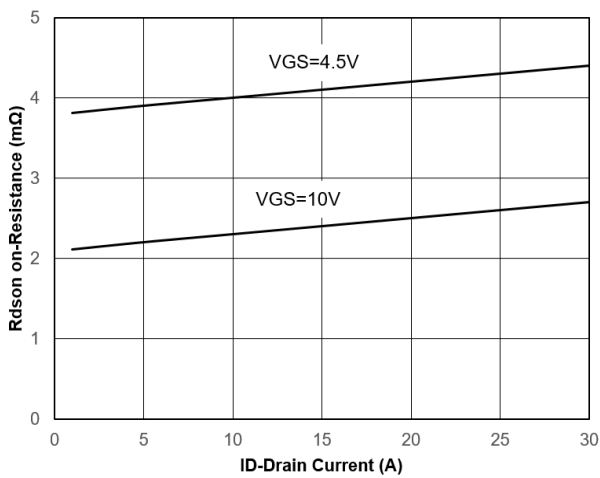


Figure 5. Drain-Source on Resistance

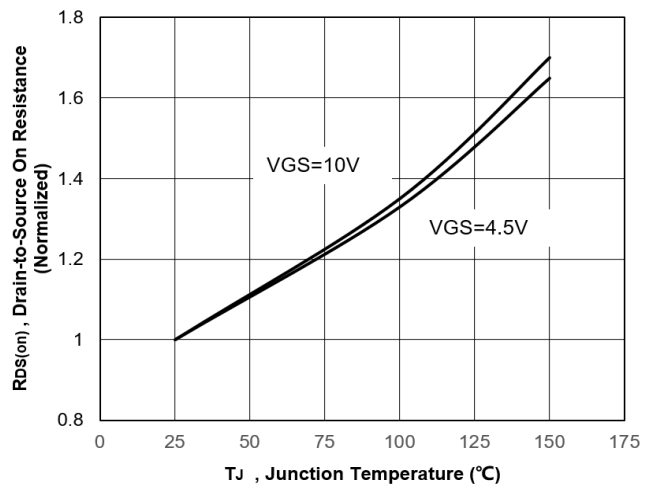


Figure 6. Normalized On-Resistance Vs. Temperature

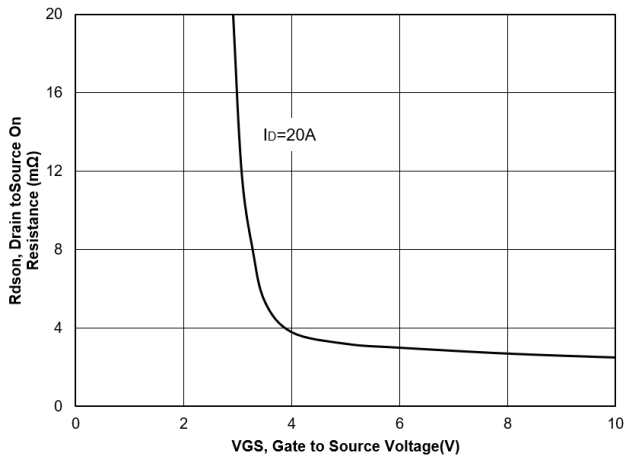


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

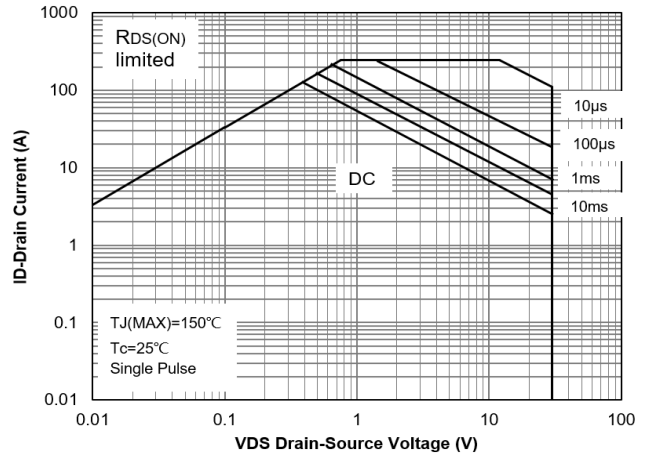


Figure 8. Safe Operation Area

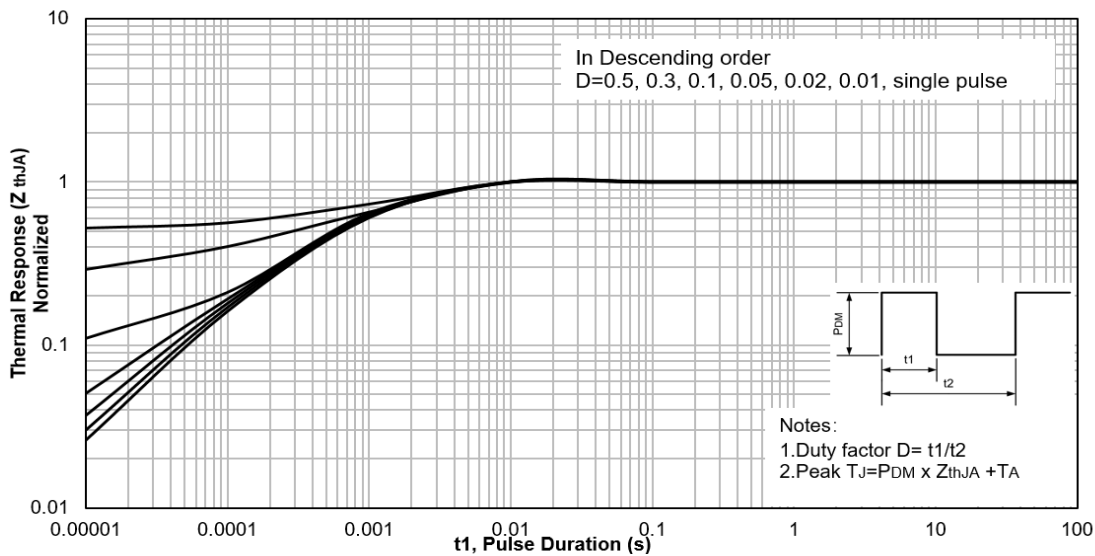


Figure 9. Maximum Effective Transient Thermal Impedance, Junction-to-Case

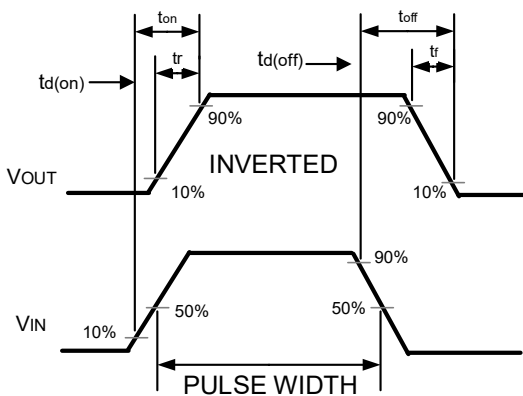
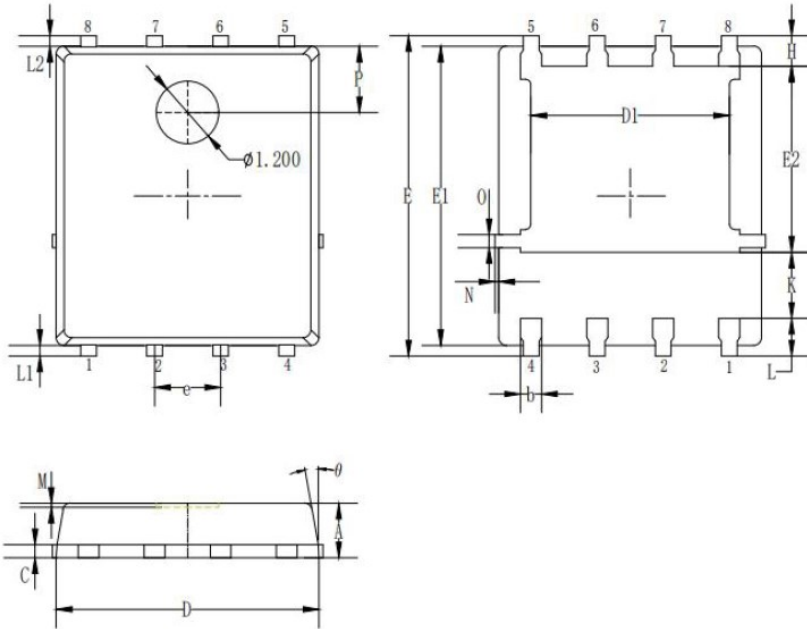


Figure 10. Switching wave

**PDFN 5X6 Package Outline Drawing**


Symbol	Millimeters		
	Min.	Nom.	Max.
A	0.90	1.05	1.20
b	0.35	0.40	0.50
c	0.20	0.25	0.35
D	4.90	5.05	5.20
D1	3.72	3.82	3.92
E	6.00	6.15	6.30
E1	5.60	5.75	5.90
E2	3.47	3.57	3.67
e	1.27 BSC		
H	0.48	0.58	0.68
K	1.17	1.27	1.37
L	0.64	0.74	0.84
L1/L2	0.20 REF		
$\theta$	8°	10°	12°
M	0.08 REF		
N	0	--	0.15
O	0.25 REF		
P	1.28 REF		