

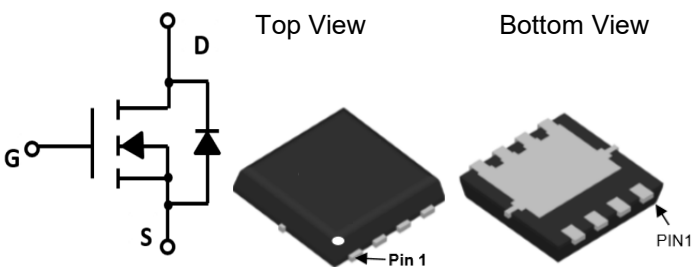
## Description

The CMN251R0F5 is the N-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

## Features

- $V_{DS}$ : 25V
- $I_D$ : 135A
- $R_{DS(on)}$  (@ $V_{GS}=10V$ ): < 1.35m $\Omega$
- High density cell design for extremely low  $R_{DS(on)}$
- Excellent on-resistance and DC current capability

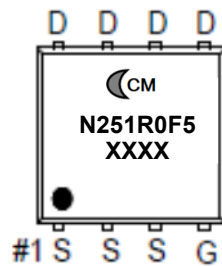
## Equivalent Circuit and Pin Configuration



## Applications

- Battery management
- Power management
- Load switch

## Marking Information



Marking Code = CMN251R0F5

Date Code = XXXX

## Ordering Information

Part Number	Packaging	Reel Size
CMN251R0F5	5000/Tape & Reel	13 inch

## Absolute Maximum Ratings (TA=25 °C unless otherwise noted)

Parameter	Symbol	Maximum	Unit	
Drain-source Voltage	$V_{DS}$	25	V	
Gate-source Voltage	$V_{GS}$	$\pm 20$	V	
Drain Current <sup>(1)(6)</sup>	$I_D$	TC=25°C	135	A
		TC=100°C	85	A
	$I_D$	TA=25°C	37	A
		TA=100°C	23	A
Pulsed Drain Current <sup>(3)</sup>	$I_{DM}$	540	A	
Total Power Dissipation <sup>(4)</sup>	PD	TC=25°C	54	W
		TA=25°C	4.1	W
Thermal Resistance Junction-to-Ambient <sup>(2)(5)</sup>	$R_{\theta JA}$	30	°C/W	
Thermal Resistance Junction-to-Case	$R_{\theta Jc}$	2.3	°C/W	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	°C	

**Electrical Characteristics (T<sub>J</sub>=25 °C unless otherwise noted)**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BVDSS	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	25			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, T <sub>C</sub> =25°C			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.0		3.0	V
Static Drain-Source on-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =55A		1.0	1.35	mΩ
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =20A, V <sub>GS</sub> =0V			1.2	V
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=100KHz		7350		pF
Output Capacitance	C <sub>oss</sub>			2780		
Reverse Transfer Capacitance	C <sub>rss</sub>			195		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =15A		115		nC
Gate Source Charge	Q <sub>gs</sub>			20		
Gate Drain Charge	Q <sub>gd</sub>			18		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =30V, I <sub>D</sub> =25A, R <sub>GEN</sub> =2.5Ω		23.3		ns
Turn-on Rise Time	t <sub>r</sub>			17.3		
Turn-off Delay Time	t <sub>D(off)</sub>			151.3		
Turn-off Fall Time	t <sub>f</sub>			226		

Noted: (1) Pulse Test: Pulse Width ≤ 300μs, Duty cycle ≤ 2%.

(2) The value of R<sub>θJA</sub> is measured with the device mounted on lin2 FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub> = 25°C. The Power dissipation PDSM is based on R<sub>θJA</sub> t ≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

(3) Single pulse width limited by junction temperature T<sub>J(MAX)</sub> = 150°C.

(4) The power dissipation PD is based on T<sub>J(MAX)</sub> = 150°C, using junction-to-case thermal resistance, and is more useful in setting the upper Dissipation limit for cases where additional heatsinking is used.

(5) The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJA</sub> and case to ambient.

(6) The maximum current rating is package limited.

**Typical Performance Characteristics**

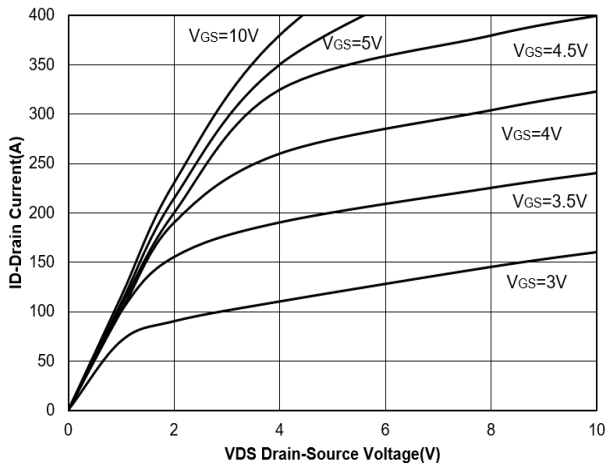


Figure 1. Output Characteristics

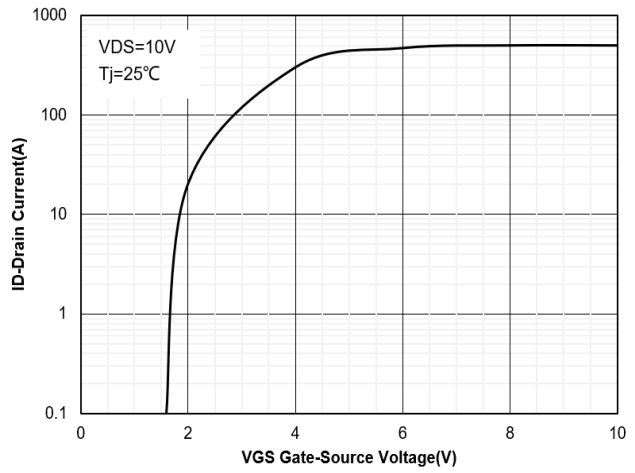


Figure 2. Transfer Characteristics

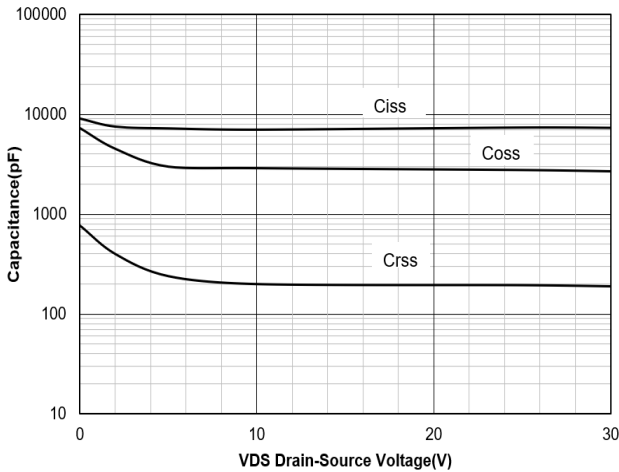


Figure 3. Capacitance Characteristics

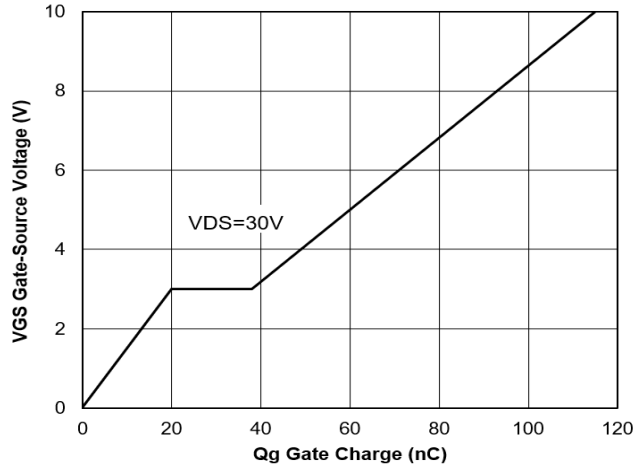


Figure 4. Gate Charge

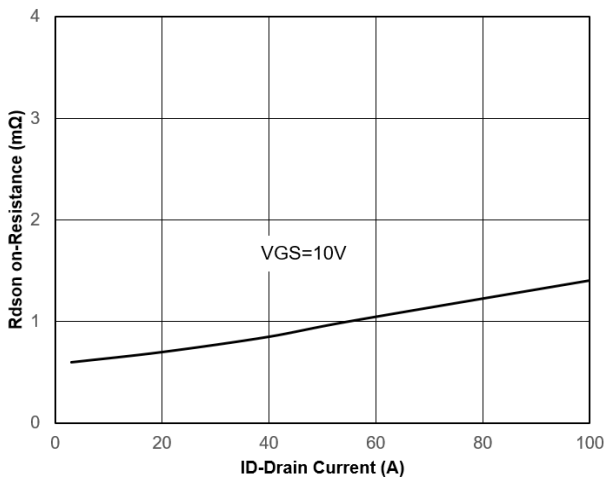


Figure 5. Drain-Source on Resistance

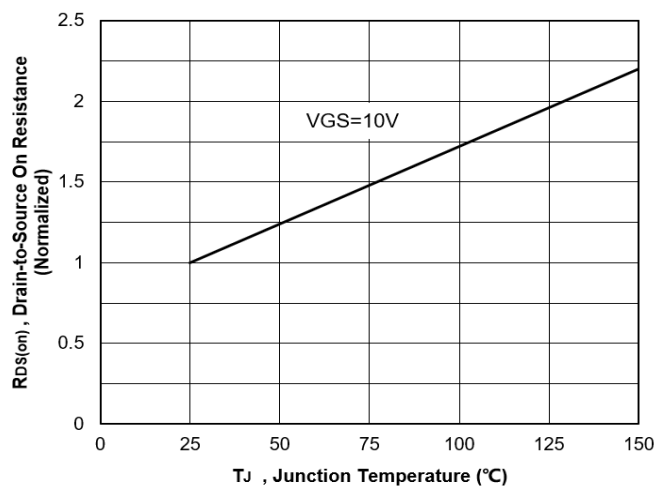


Figure 6. Normalized On-Resistance

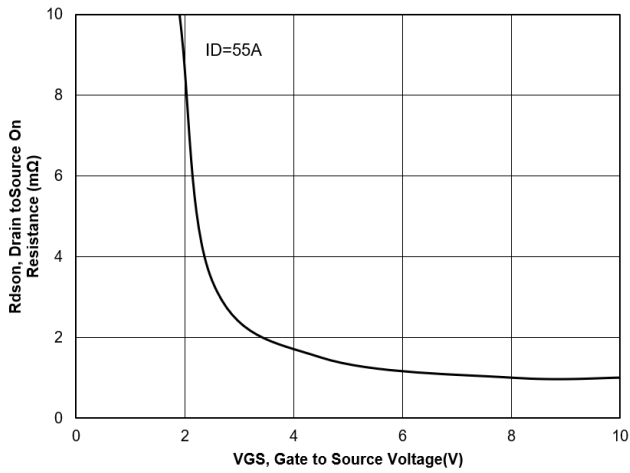


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

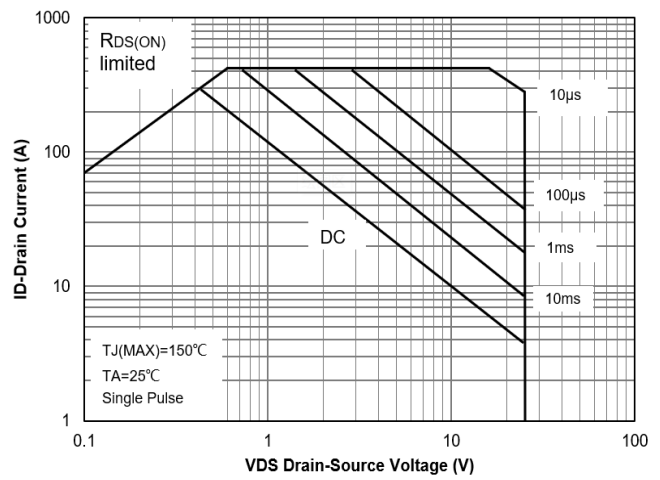


Figure 8. Safe Operation Area

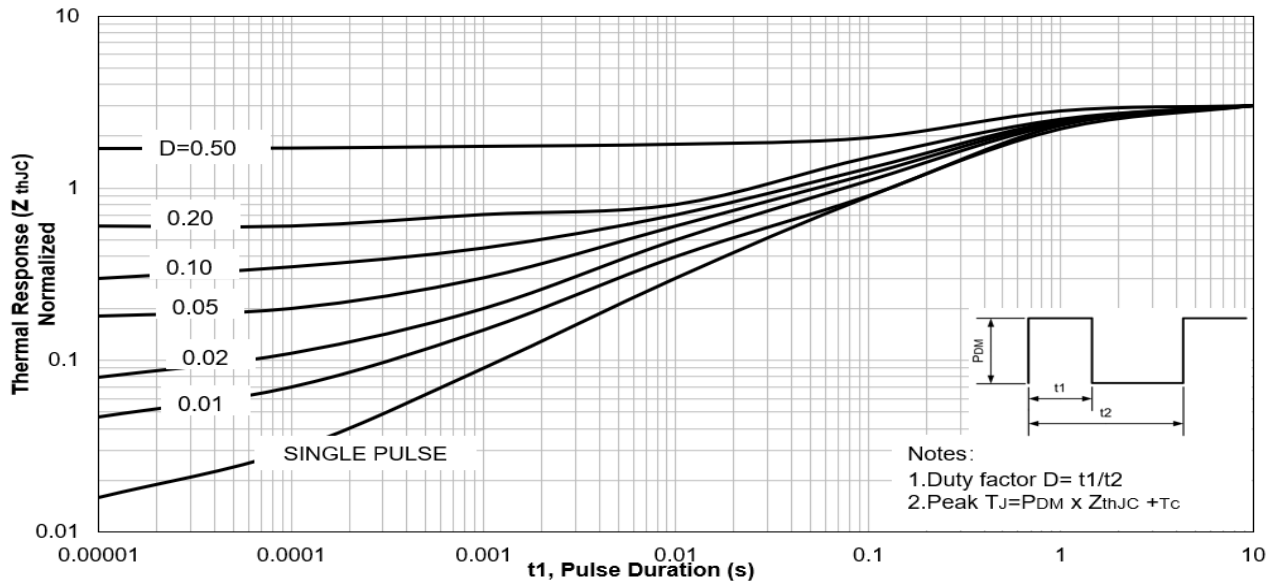


Figure 9. Maximum Effective Transient Thermal Impedance, Junction-to-Case

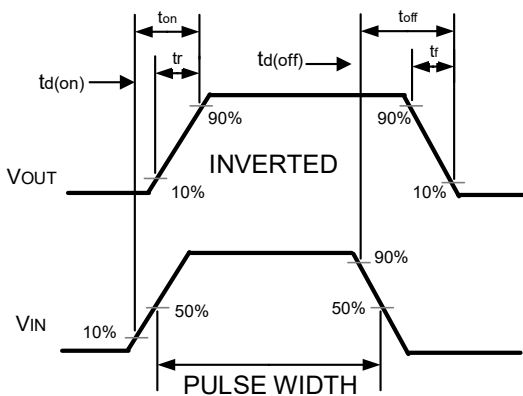
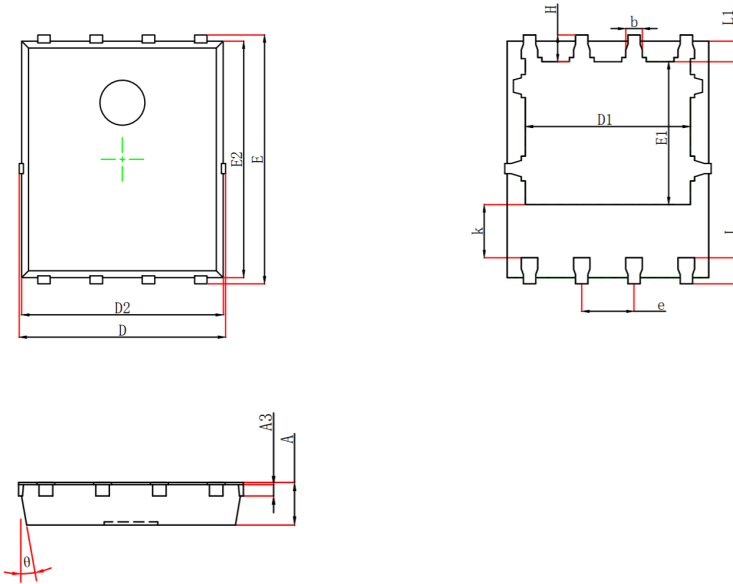


Figure 10. Switching wave

### DFN 5X6 Package Outline Drawing



Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254 REF.		0.010 REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270 TYP.		0.050 TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
$\theta$	10°	12°	10°	12°

### Contact Information

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