

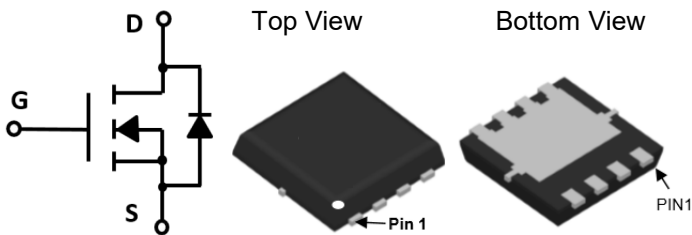
Description

The CMN2002F3 is the N-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

Features

- V_{DS} : 20V
- I_D : 69A
- $R_{DS(on)}$ (@ $V_{GS}=4.5V$) : < 2.8m Ω
- $R_{DS(on)}$ (@ $V_{GS}=2.5V$) : < 3.9m Ω
- High density cell design for extremely low $R_{DS(on)}$
- Excellent on-resistance and DC current capability

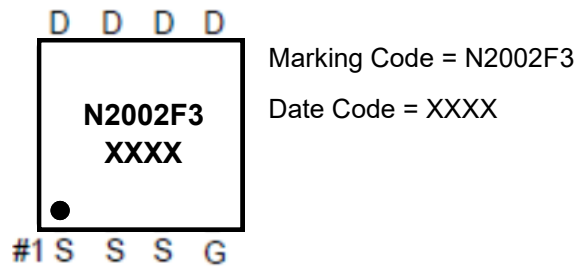
Equivalent Circuit and Pin Configuration



Applications

- Battery management
- Power management
- Load switch

Marking Information



Ordering Information

| Part Number | Packaging | Reel Size |
|-------------|------------------|-----------|
| CMN2002F3 | 5000/Tape & Reel | 13 inch |

Absolute Maximum Ratings (TA=25 °C unless otherwise noted)

| Parameter | Symbol | Maximum | Unit |
|----------------------------------------------------------|-----------------|-------------|---------------|
| Drain-source Voltage | V_{DS} | 20 | V |
| Gate-source Voltage | V_{GS} | ± 12 | V |
| Drain Current ⁽¹⁾⁽⁶⁾ | I_D | 69 | A |
| | | 45 | A |
| | I_D | 20 | A |
| | | 13 | A |
| Pulsed Drain Current ⁽³⁾ | I_{DM} | 138 | A |
| Total Power Dissipation ⁽⁴⁾ | P_D | 23 | W |
| | | 2.0 | W |
| Thermal Resistance Junction-to-Ambient ⁽²⁾⁽⁵⁾ | $R_{\theta JA}$ | 63 | $^{\circ}C/W$ |
| Thermal Resistance Junction-to-Case | $R_{\theta Jc}$ | 6.5 | $^{\circ}C/W$ |
| Junction and Storage Temperature Range | T_J, T_{STG} | -55 to +150 | $^{\circ}C$ |

Electrical Characteristics (T_J=25 °C unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---------------------------------------|---------------------|------------------------------------------------------------------------------------------|-----|------|------|-------|
| Static Parameter | | | | | | |
| Drain-Source Breakdown Voltage | BVDSS | V _{GS} =0V, I _D =250μA | 20 | | | V |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} =20V, V _{GS} =0V, T _C =25°C | | | 1 | μA |
| Gate-Body Leakage Current | I _{GSS} | V _{GS} =±12V, V _{DS} =0V | | | ±100 | nA |
| Gate Threshold Voltage | V _{GS(th)} | V _{DS} =V _{GS} , I _D =250μA | 0.6 | | 1.3 | V |
| Static Drain-Source on-Resistance | R _{DS(on)} | V _{GS} =4.5V, I _D =15A | | 2.2 | 2.8 | mΩ |
| | | V _{GS} =2.5V, I _D =10A | | 3.0 | 3.9 | |
| Diode Forward Voltage | V _{SD} | I _S =15A, V _{GS} =0V | | 0.8 | 1.2 | V |
| Maximum Body-Diode Continuous Current | I _S | | | | 69 | A |
| Dynamic Parameters | | | | | | |
| Input Capacitance | C _{iss} | V _{DS} =10V, V _{GS} =0V, f=1MHz | | 6200 | | pF |
| Output Capacitance | C _{oss} | | | 820 | | |
| Reverse Transfer Capacitance | C _{rss} | | | 700 | | |
| Switching Parameters | | | | | | |
| Total Gate Charge | Q _g | V _{GS} =4.5V, V _{DS} =10V, I _D =15A | | 63 | | nC |
| Gate Source Charge | Q _{gs} | | | 10 | | |
| Gate Drain Charge | Q _{gd} | | | 20 | | |
| Turn-on Delay Time | t _{D(on)} | V _{GS} =10V, V _{DD} =10V, I _D =10A, R _{GEN} =6Ω | | 18 | | ns |
| Turn-on Rise Time | t _r | | | 15.8 | | |
| Turn-off Delay Time | t _{D(off)} | | | 324 | | |
| Turn-off Fall Time | t _f | | | 93.7 | | |

Noted: (1) Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

(2) The value of R_{θJA} is measured with the device mounted on lin2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C. The Power dissipation PDSM is based on R_{θJA} t ≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

(3) Single pulse width limited by junction temperature T_{J(MAX)} = 150°C.

(4) The power dissipation PD is based on T_{J(MAX)} = 150°C, using junction-to-case thermal resistance, and is more useful in setting the upper Dissipation limit for cases where additional heatsinking is used.

(5) The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJA} and case to ambient.

(6) The maximum current rating is package limited.

Typical Performance Characteristics

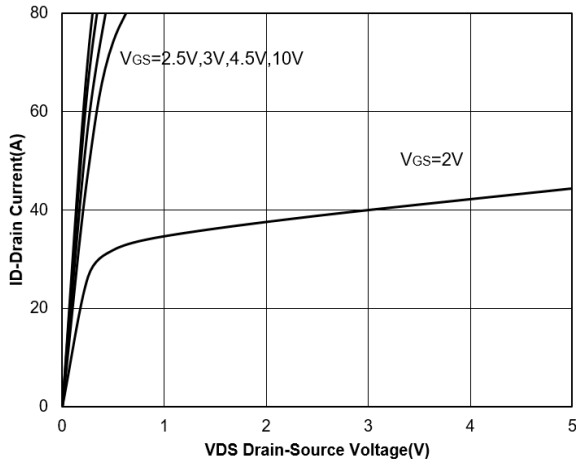


Figure 1. Output Characteristics

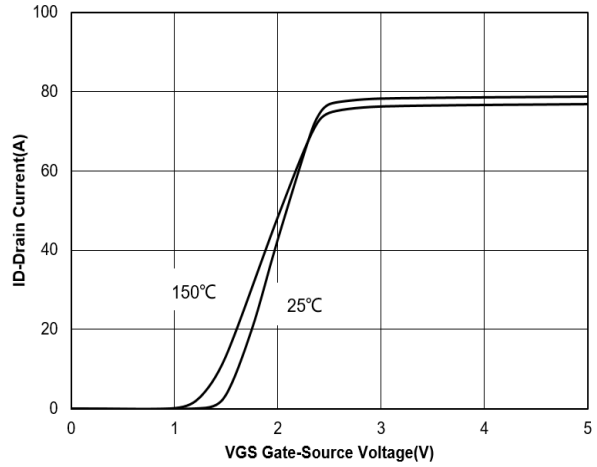


Figure 2. Transfer Characteristics

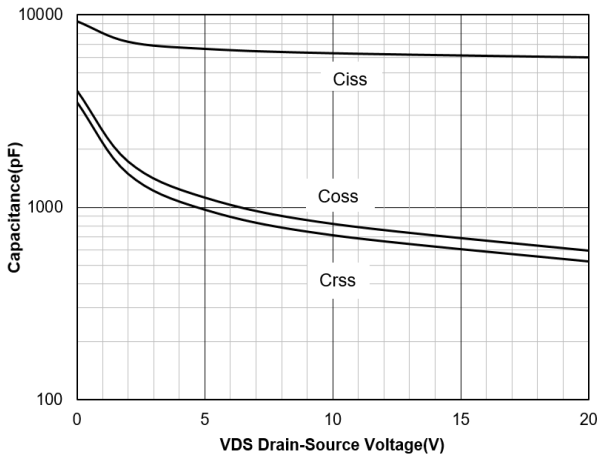


Figure 3. Capacitance Characteristics

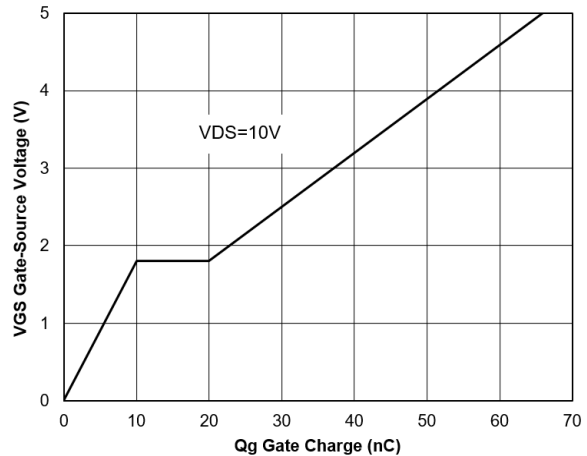


Figure 4. Gate Charge

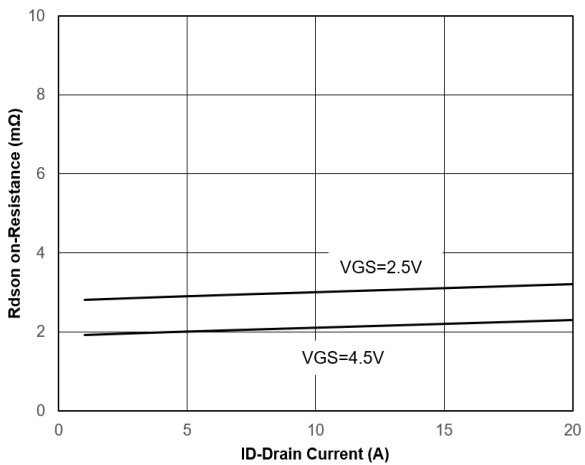


Figure 5. Drain-Source on Resistance

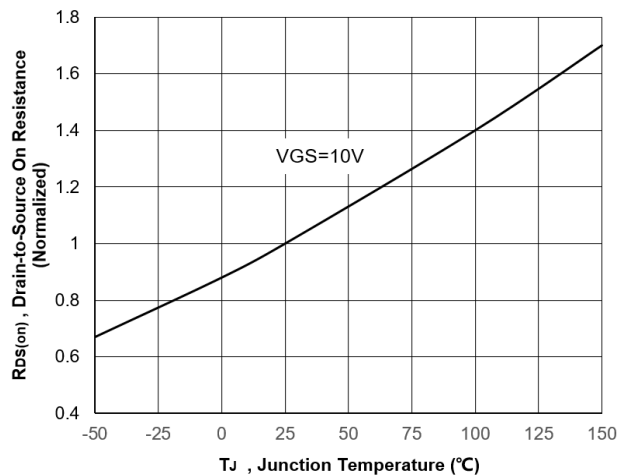


Figure 6. Normalized On-Resistance

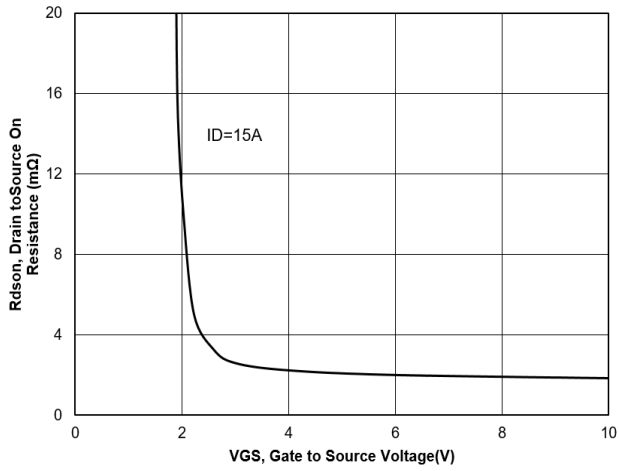


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

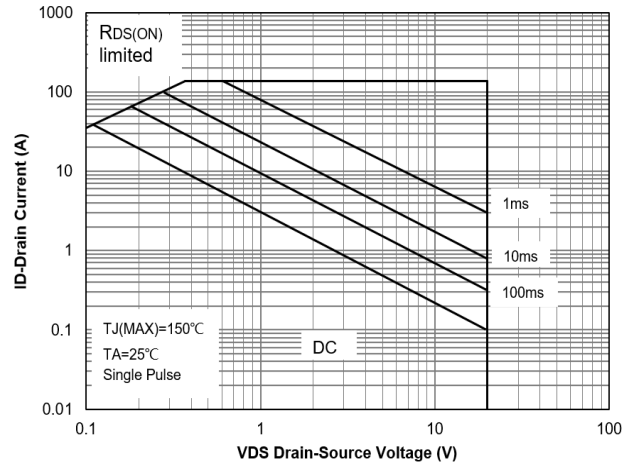


Figure 8. Safe Operation Area

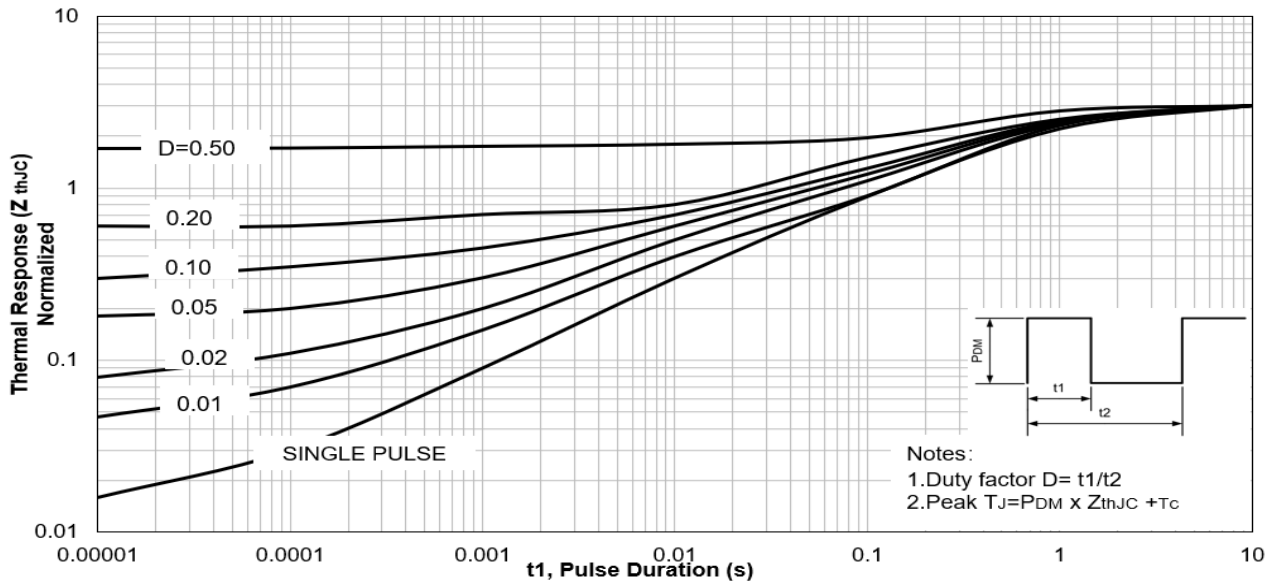


Figure 9. Maximum Effective Transient Thermal Impedance, Junction-to-Case

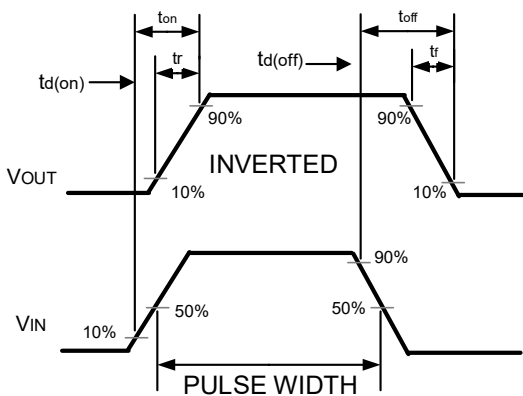
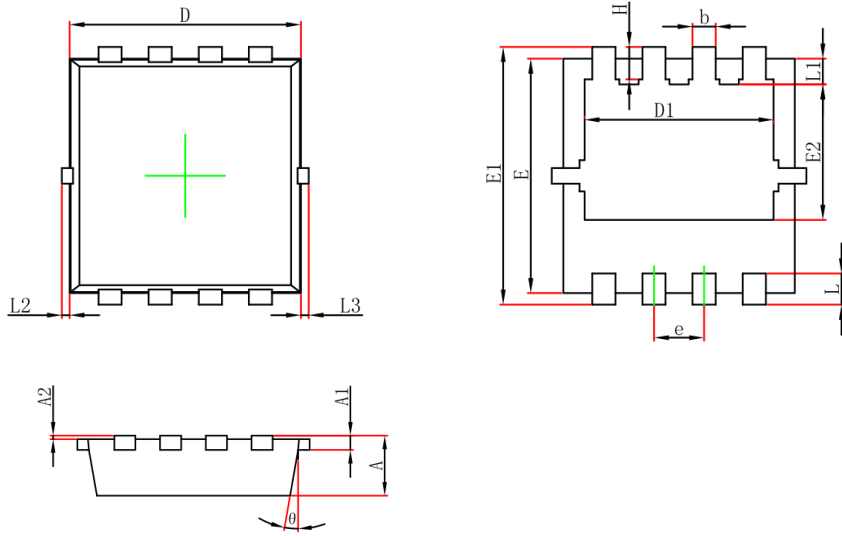


Figure 10. Switching wave

PDFN 3.3x3.3 Package Outline Drawing


| Symbol | Millimeters | | Inches | |
|--------|-------------|-------|------------|-------|
| | Min. | Max. | Min. | Max. |
| A | 0.650 | 0.850 | 0.026 | 0.033 |
| A1 | 0.152 REF. | | 0.006 REF. | |
| A2 | 0~0.05 | | 0~0.002 | |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| D1 | 2.300 | 2.600 | 0.091 | 0.102 |
| E | 2.900 | 3.100 | 0.114 | 0.122 |
| E1 | 3.150 | 3.450 | 0.124 | 0.136 |
| E2 | 1.535 | 1.935 | 0.060 | 0.076 |
| b | 0.200 | 0.400 | 0.008 | 0.016 |
| e | 0.550 | 0.750 | 0.022 | 0.030 |
| L | 0.300 | 0.500 | 0.012 | 0.020 |
| L1 | 0.180 | 0.480 | 0.007 | 0.019 |
| L2 | 0~0.100 | | 0~0.004 | |
| L3 | 0~0.100 | | 0~0.004 | |
| H | 0.315 | 0.515 | 0.012 | 0.020 |
| θ | 9° | 13° | 9° | 13° |