

Description

CMD101312RSF5 is the Dual N and P-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

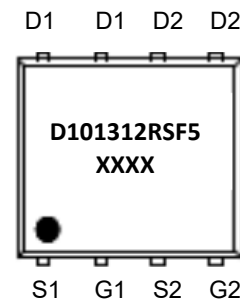
Features

- N-Channel V_{DS} : 100V
- N-Channel I_D : 8A
- N-Channel $R_{DS(on)}$ (@ $V_{GS}=10V$): < 120m Ω
- N-Channel $R_{DS(on)}$ (@ $V_{GS}=4.5V$): < 180m Ω
- P-Channel V_{DS} : -100V
- P-Channel I_D : -11A
- P-Channel $R_{DS(on)}$ (@ $V_{GS}=-10V$): < 115m Ω
- P-Channel $R_{DS(on)}$ (@ $V_{GS}=-4.5V$): < 130m Ω
- High density cell design for extremely low $R_{DS(on)}$
- Excellent on-resistance and DC current capability

Applications

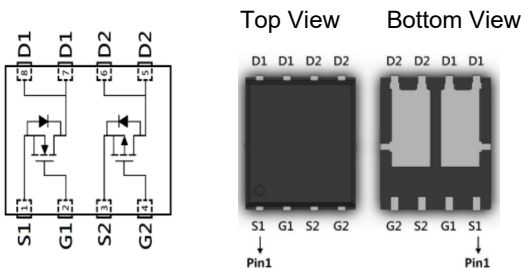
- Cellular Handsets and Accessories
- Personal Digital Assistants
- Portable Instrumentation
- Load switch

Marking Information



Marking Code = D101312RSF5
 Date Code = XXXX

Equivalent Circuit and Pin Configuration



Ordering Information

Part Number	Packaging	Reel Size
CMD101312RSF5	5000/Tape & Reel	13 inch

Absolute Maximum Ratings (TA=25 °C unless otherwise noted)

Parameter	Symbol	Maximum		Unit	
		N-Channel	P-Channel		
Drain-source Voltage	V_{DS}	100	-100	V	
Gate-source Voltage	V_{GS}	± 20	± 20	V	
Drain Current ⁽¹⁾⁽⁶⁾	I_D	$T_C=25^\circ C$	8	-11	A
		$T_C=100^\circ C$	3	-3	A
Pulsed Drain Current ⁽³⁾	I_{DM}	30	-44	A	
Total Power Dissipation ⁽⁴⁾	PD	17	28	W	
Thermal Resistance Junction-to-Ambient ⁽²⁾⁽⁵⁾	$R_{\theta JA}$	63	58	$^\circ C/W$	
Thermal Resistance Junction-to-Case	$R_{\theta Jc}$	7.4	4.5	$^\circ C/W$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	$^\circ C$	

N-Channel Electrical Characteristics (T_J=25 °C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V, T _C =25°C			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0		2.5	V
Static Drain-Source on-Resistance	R _{DSON}	V _{GS} =10V, I _D =5A		100	120	mΩ
		V _{GS} =4.5V, I _D =4A		140	180	
Diode Forward Voltage	V _{SD}	I _S =8A, V _{GS} =0V		0.85	1.2	V
Maximum Body-Diode Continuous Current	I _S				8	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHz		196		pF
Output Capacitance	C _{oss}			27		
Reverse Transfer Capacitance	C _{rss}			1.85		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =2A		3.78		nC
Gate Source Charge	Q _{gs}			0.45		
Gate Drain Charge	Q _{gd}			0.83		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _D =1A, R _{GEN} =6Ω		10.6		ns
Turn-on Rise Time	t _r			5.2		
Turn-off Delay Time	t _{D(off)}			24.8		
Turn-off Fall Time	t _f			12.7		

Noted: (1) Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

(2) The value of R_{θJA} is measured with the device mounted on lin2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C. The Power dissipation P_{DSM} is based on R_{θJA} t ≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

(3) Single pulse width limited by junction temperature T_{J(MAX)} = 150°C.

(4) The power dissipation PD is based on T_{J(MAX)} = 150°C, using junction-to-case thermal resistance, and is more useful in setting the upper Dissipation limit for cases where additional heatsinking is used.

(5) The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJA} and case to ambient.

(6) The maximum current rating is package limited.

N-Channel Typical Performance Characteristics

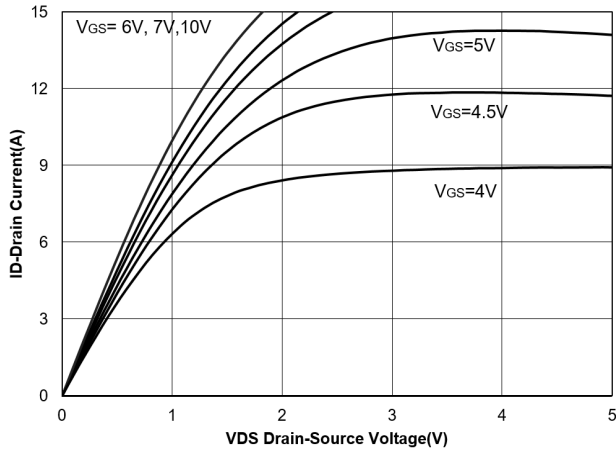


Figure 1. Output Characteristics

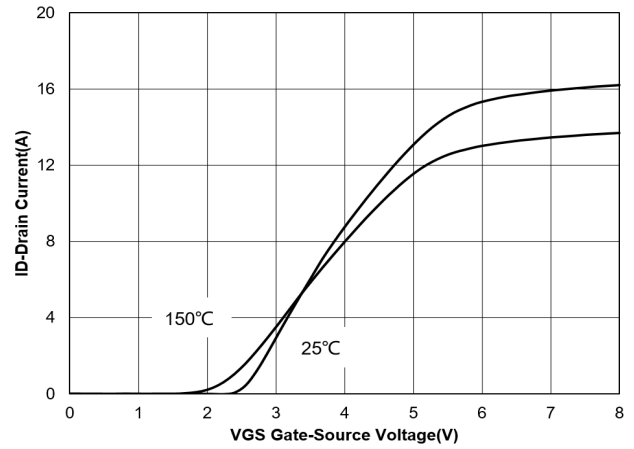


Figure 2. Transfer Characteristics

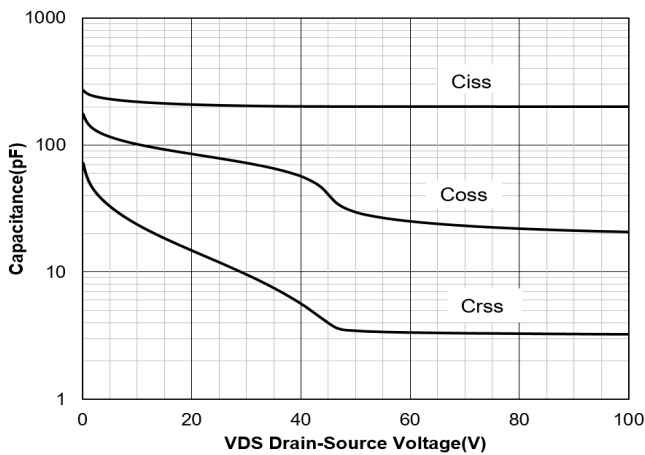


Figure 3. Capacitance Characteristics

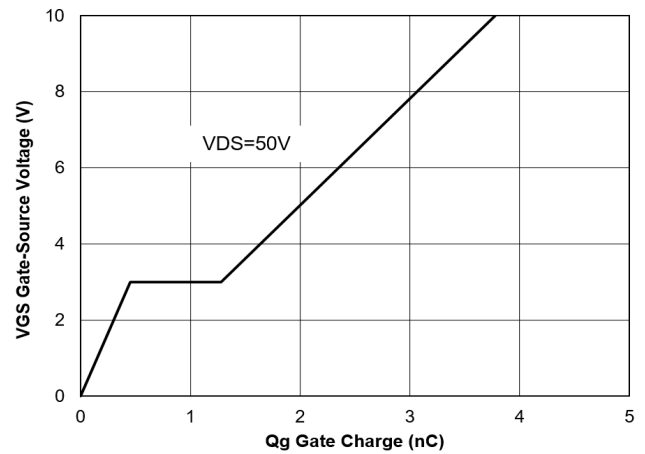


Figure 4. Gate Charge

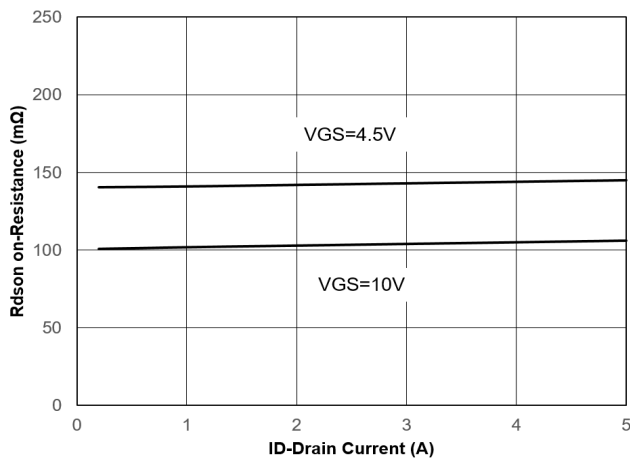


Figure 5. Drain-Source on Resistance

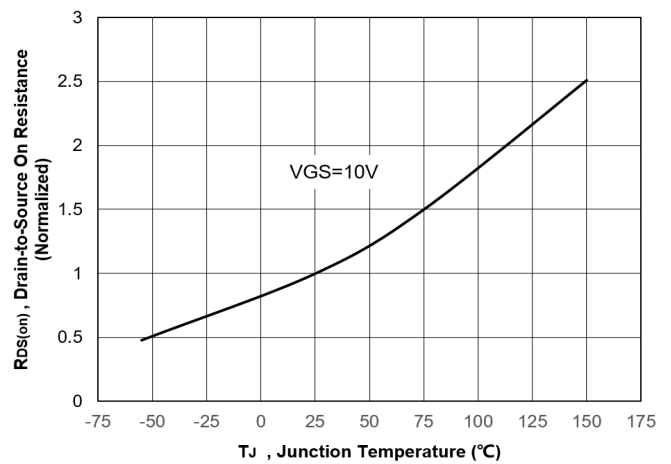


Figure 6. Normalized On-Resistance Vs. Temperature

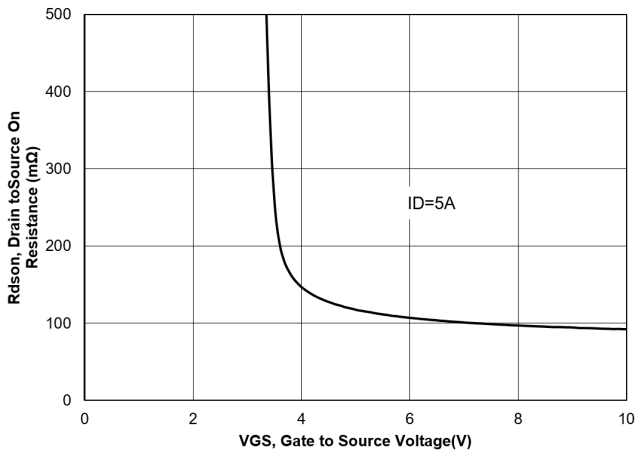


Figure 7. Typical Drain to Source ON Resistance

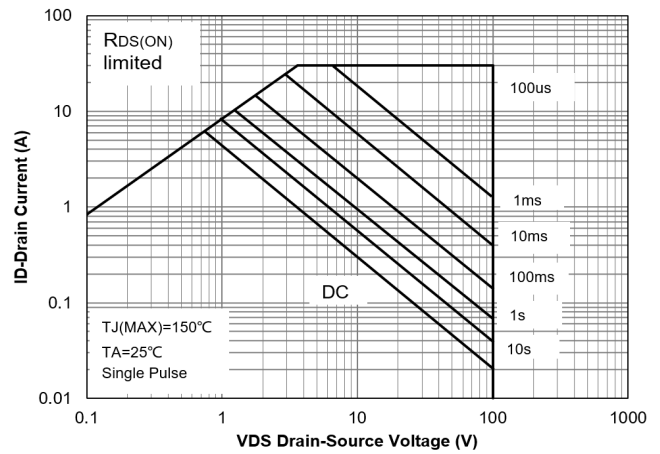


Figure 8. Safe Operation Area

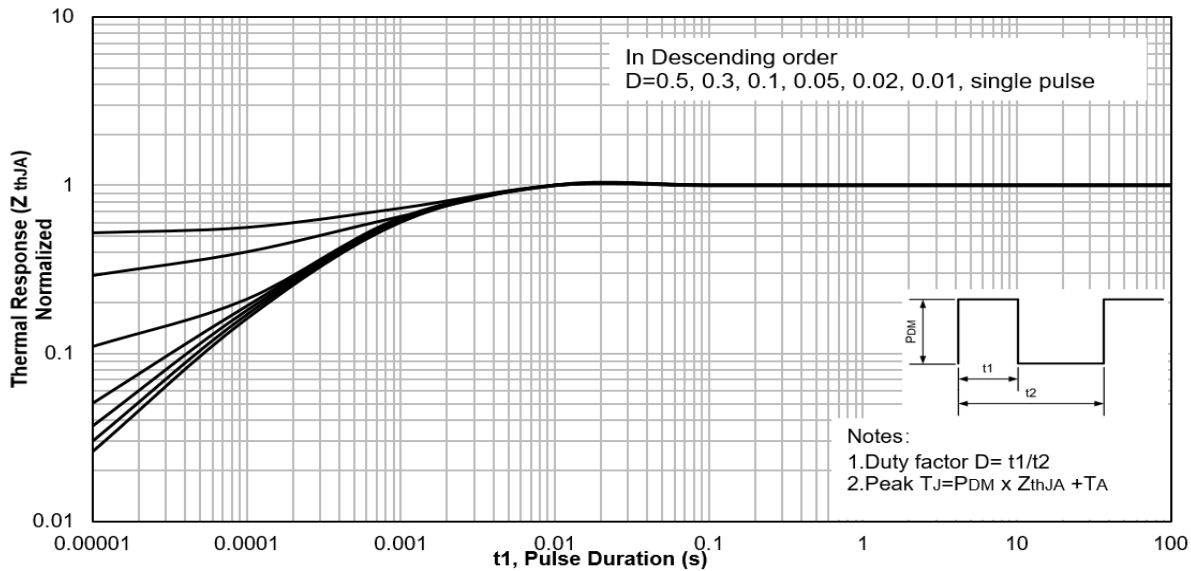


Figure 9. Maximum Effective Transient Thermal Impedance ,Junction-to-Ambient

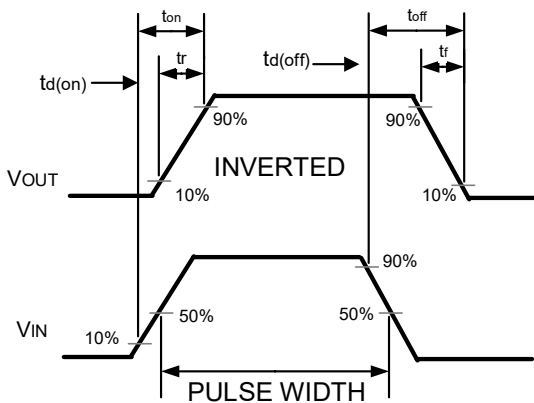


Figure 10. Switching wave

P-Channel Electrical Characteristics (T_J=25 °C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-100V, V _{GS} =0V, T _C =25°C			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1.0		-2.5	V
Static Drain-Source on-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-5A		95	115	mΩ
		V _{GS} =-4.5V, I _D =-4A		100	130	
Diode Forward Voltage	V _{SD}	I _S =-11A, V _{GS} =0V		-0.85	-1.2	V
Maximum Body-Diode Continuous Current	I _S				-11	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-50V, V _{GS} =0V, f=1MHz		3770		pF
Output Capacitance	C _{oss}			71.2		
Reverse Transfer Capacitance	C _{rss}			68.5		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-50V, I _D =-2A		60		nC
Gate Source Charge	Q _{gs}			3.3		
Gate Drain Charge	Q _{gd}			5.2		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DD} =-50V, I _D =-1A, R _{GEN} =6Ω		21		ns
Turn-on Rise Time	t _r			6.3		
Turn-off Delay Time	t _{D(off)}			246		
Turn-off Fall Time	t _f			28		

P-Channel Typical Performance Characteristics

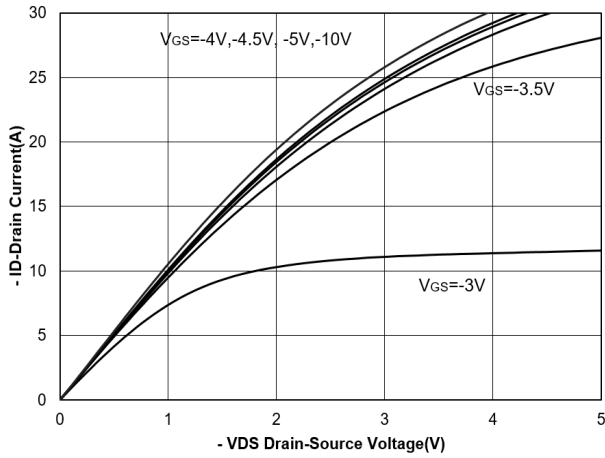


Figure 11. Output Characteristics

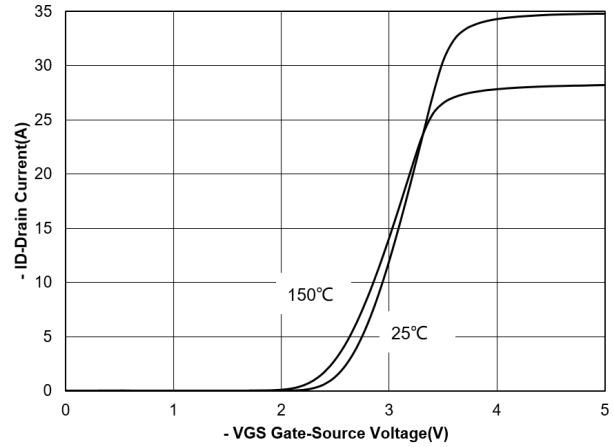


Figure 12. Transfer Characteristics

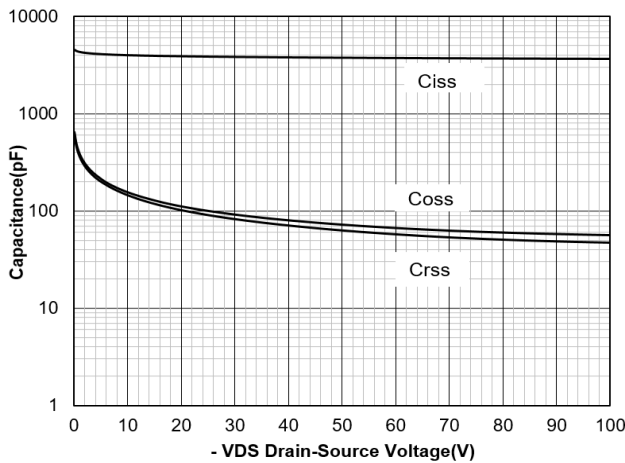


Figure 13. Capacitance Characteristics

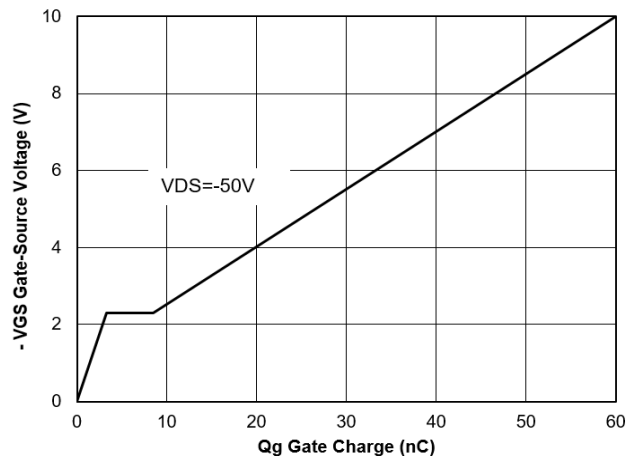


Figure 14. Gate Charge

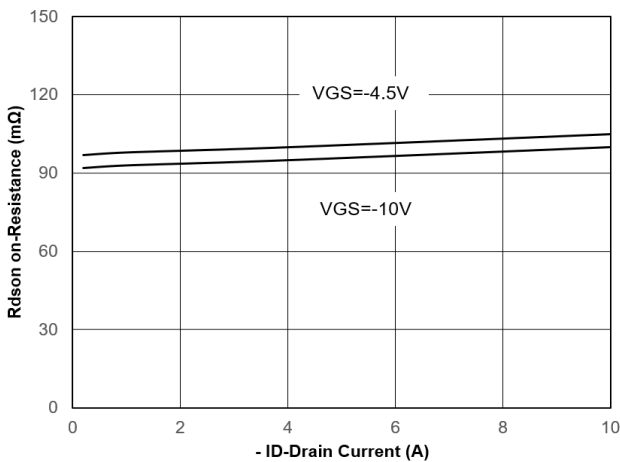


Figure 15. Drain-Source on Resistance

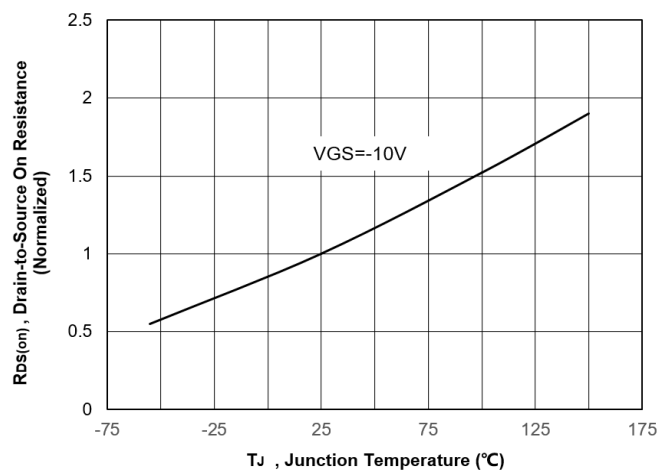


Figure 16. Normalized On-Resistance Vs. Temperature

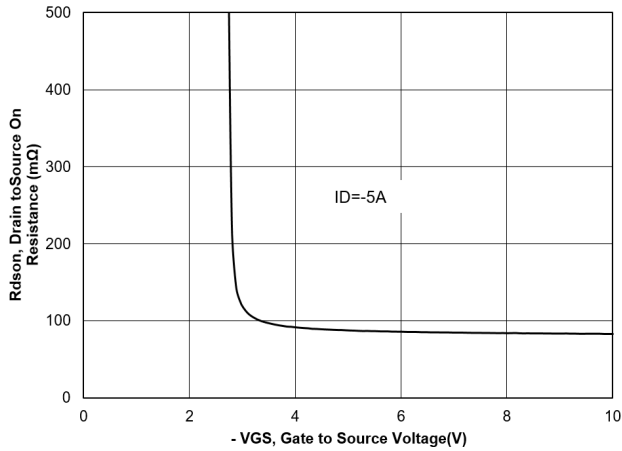


Figure 17. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

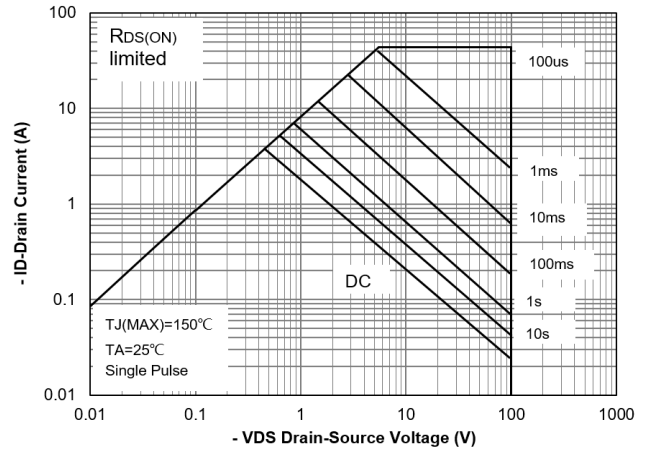


Figure 18. Safe Operation Area

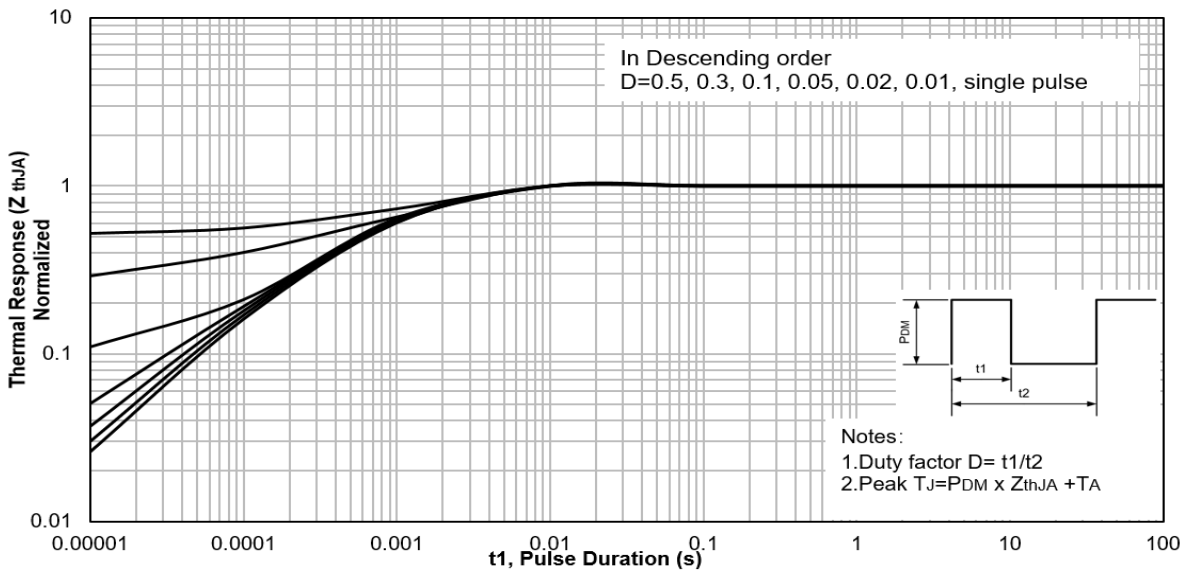


Figure 19. Maximum Effective Transient Thermal Impedance ,Junction-to-Ambient

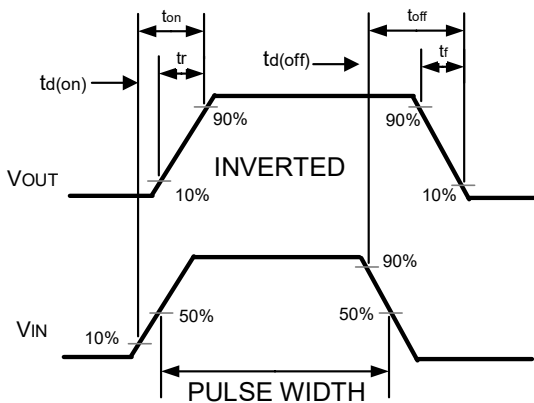
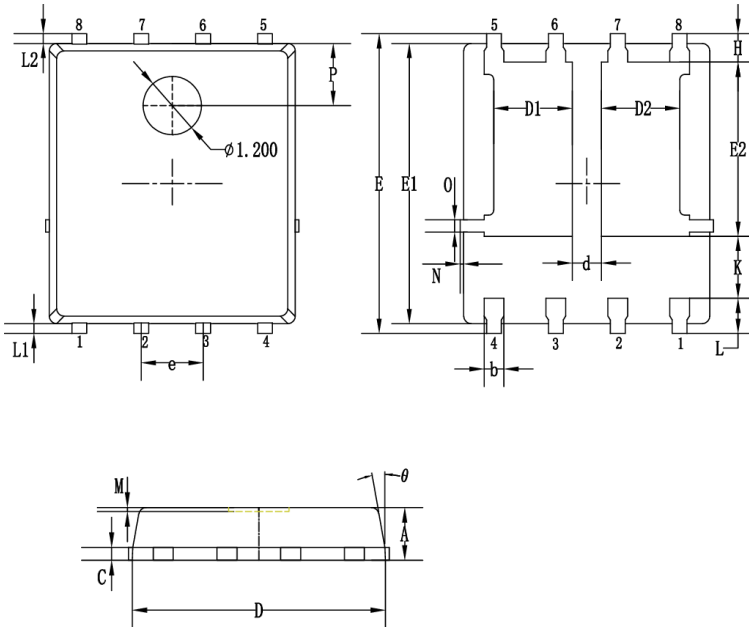


Figure 20. Switching wave

DFN 5x6 Package Outline Drawing



Symbol	Millimeters		
	Min.	Nom.	Max.
A	0.90	1.05	1.20
b	0.35	0.40	0.50
C	0.20	0.25	0.35
D	4.90	5.05	5.20
D1/D2	1.51	1.61	1.71
d	0.50	0.60	0.70
E	6.00	6.15	6.30
E1	5.60	5.75	5.90
E2	3.47	3.57	3.67
e	1.27 BSC		
H	0.48	0.58	0.68
K	1.17	1.27	1.37
L	0.64	0.74	0.84
L1/L2	0.20 REF		
θ	8°	10°	12°
M	0.08 REF		
N	0	--	0.15
O	0.25 REF		
P	1.28 REF		

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