

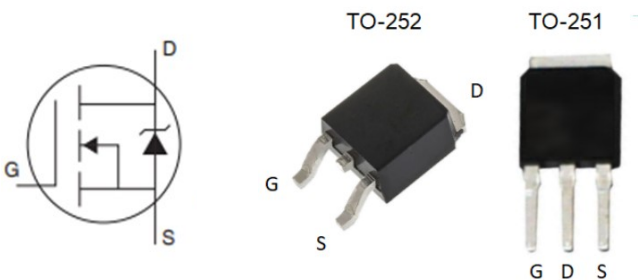
Description

The CM65R640XU/D is the N-Channel enhancement mode power field effect transistors with high cell density, high voltage Super Junction technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance, .

Features

- VDS: 650V
- ID (@VGS=10V): 7A
- RDS_{ON} (@VGS=10V) : < 615mΩ
- High density cell design for extremely low RDS_{ON}
- Excellent on-resistance and DC current capability

Equivalent Circuit and Pin Configuration



Applications

- AC/DC load switch
- SMPS
- LED power

Marking Information



X=Package type
 XXXX = Marking Code

Ordering Information

P/N	Package Type	Packaging
CM65R640XU	TO-252	Tape and reel
CM65R640XD	TO-251	Tube

Absolute Maximum Ratings (T_c=25 °C unless otherwise noted)

Parameter	Symbol	Maximum		Unit
		CM65R640XU	CM65R640XD	
Drain-source Voltage	V _{DS}	650		V
Gate-source Voltage	V _{GS}	±30		V
Continuous Drain Current ⁽¹⁾	I _D	T _c =25°C	7	A
		T _c =100°C	4.4	A
Pulsed Drain Current ⁽²⁾	I _{DM}	28		A
Total Power Dissipation ⁽³⁾	PD @ T _c =25°C	69		W
	Derating Factor above 25°C	0.56		W/°C
Thermal Resistance Junction-to-Case ⁽³⁾	R _{θJC}	1.8		°C/W
Junction and Storage Temperature Range	T _J ,T _{STG}	-55 to +150		°C

Electrical Characteristics (T_c=25 °C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BVDSS	V _{GS} =0V, I _D =250μA	650			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =650V, V _{GS} =0V, T _C =25°C			5	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2		4	V
Static Drain-Source on-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =3.5A		510	615	mΩ
Diode Forward Voltage	V _{SD}	I _S =7A, V _{GS} =0V		0.9	1.3	V
Maximum Body-Diode Continuous Current	I _S				7	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =100V, V _{GS} =0V, f=1MHz		417		pF
Output Capacitance	C _{oss}			35		
Reverse Transfer Capacitance	C _{rss}			6.3		
Switching Parameters						
Total Gate Charge	Q _g	V _{DS} =480V, I _D =3.5A, V _{GS} =10V		16.8		nC
Gate Source Charge	Q _{gs}			2.2		
Gate Drain Charge	Q _{gd}			10.2		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, R _L =15Ω, R _{GEN} =25Ω		46		ns
Turn-on Rise Time	t _r			39.3		
Turn-off Delay Time	t _{D(off)}			59		
Turn-off Fall Time	t _f			28.2		

Noted: (1) Pulse Test: Pulse Width ≤ 300μs, Duty cycle ≤ 2%

(2) Pulse width limited by maximum junction temperature

(3) Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. With 2oz Copper, t ≤ 10s

Typical Performance Characteristics

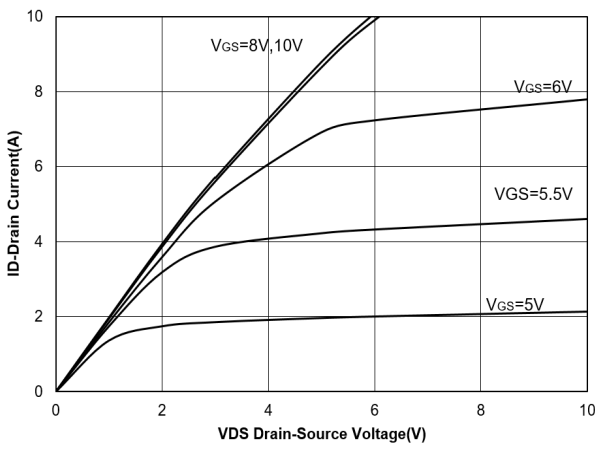


Figure 1. Output Characteristics

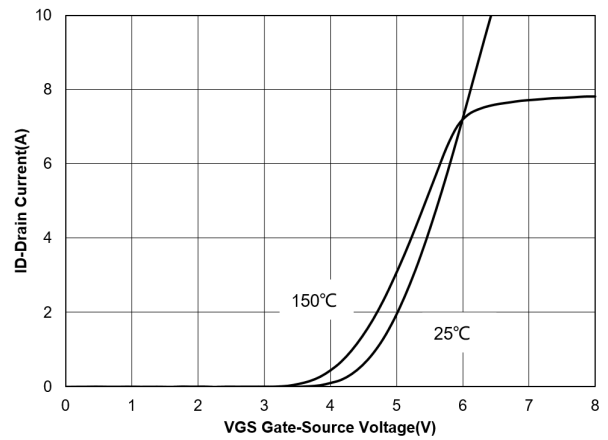


Figure 2. Transfer Characteristics

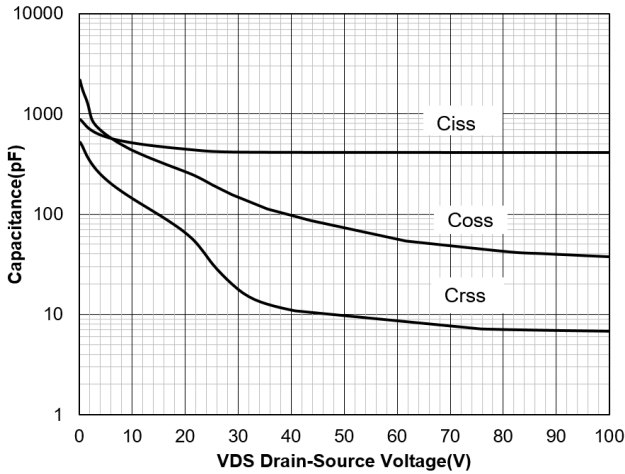


Figure 3. Capacitance Characteristics

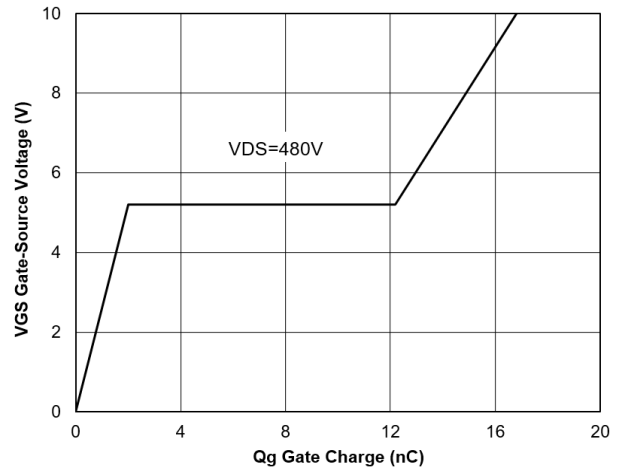


Figure 4. Gate Charge

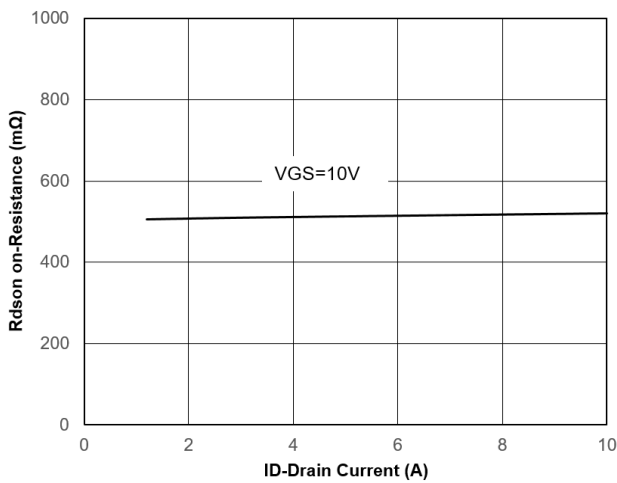


Figure 5. Drain-Source on Resistance

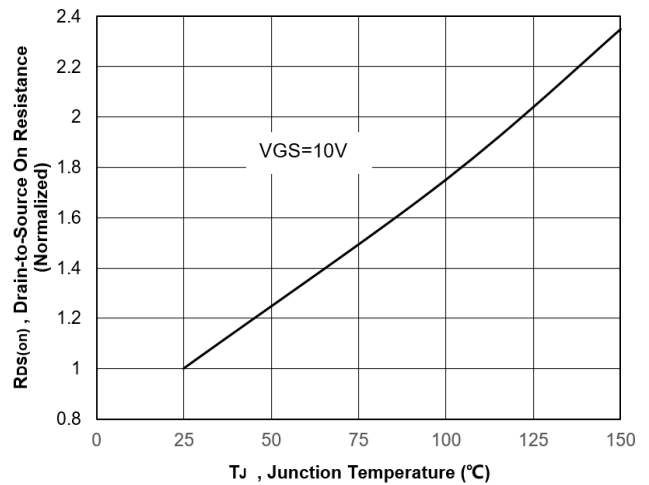


Figure 6. Normalized On-Resistance Vs. Temperature

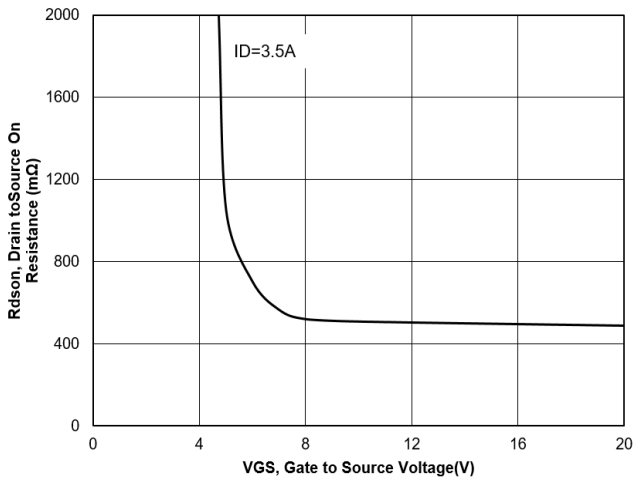


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

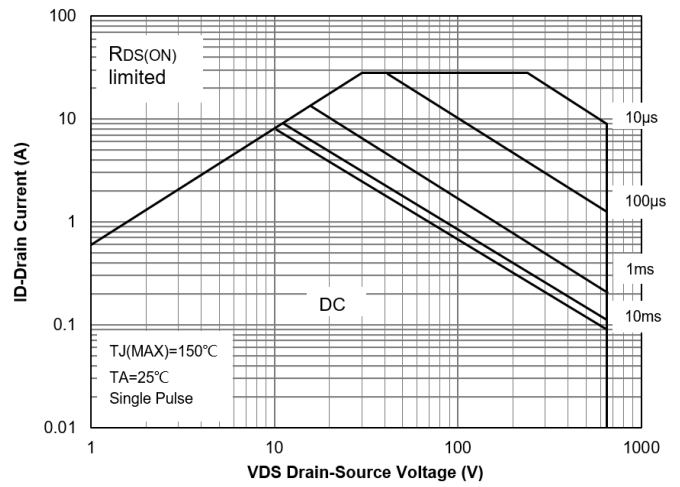


Figure 8. Safe Operation Area

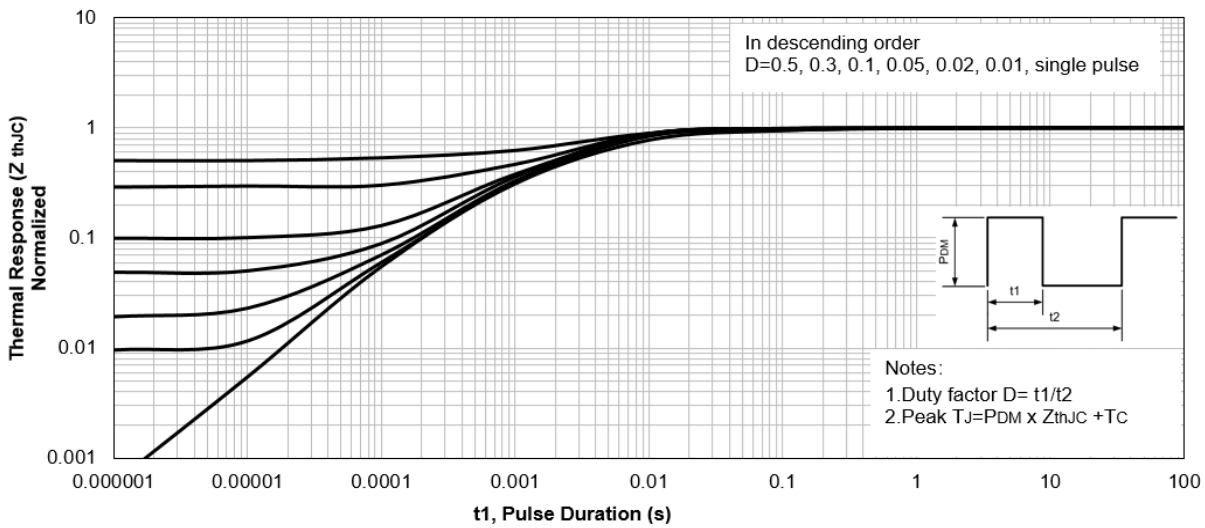


Figure 9. Maximum Effective Transient Thermal Impedance ,Junction-to-Case

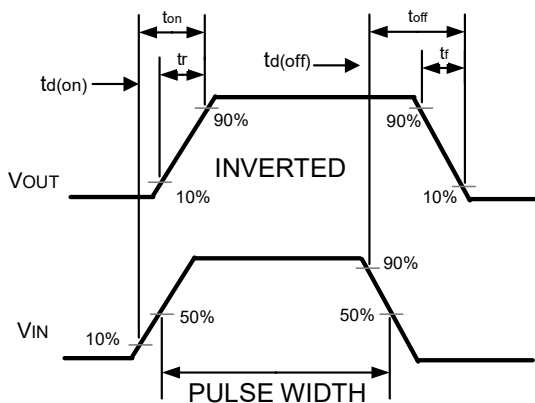
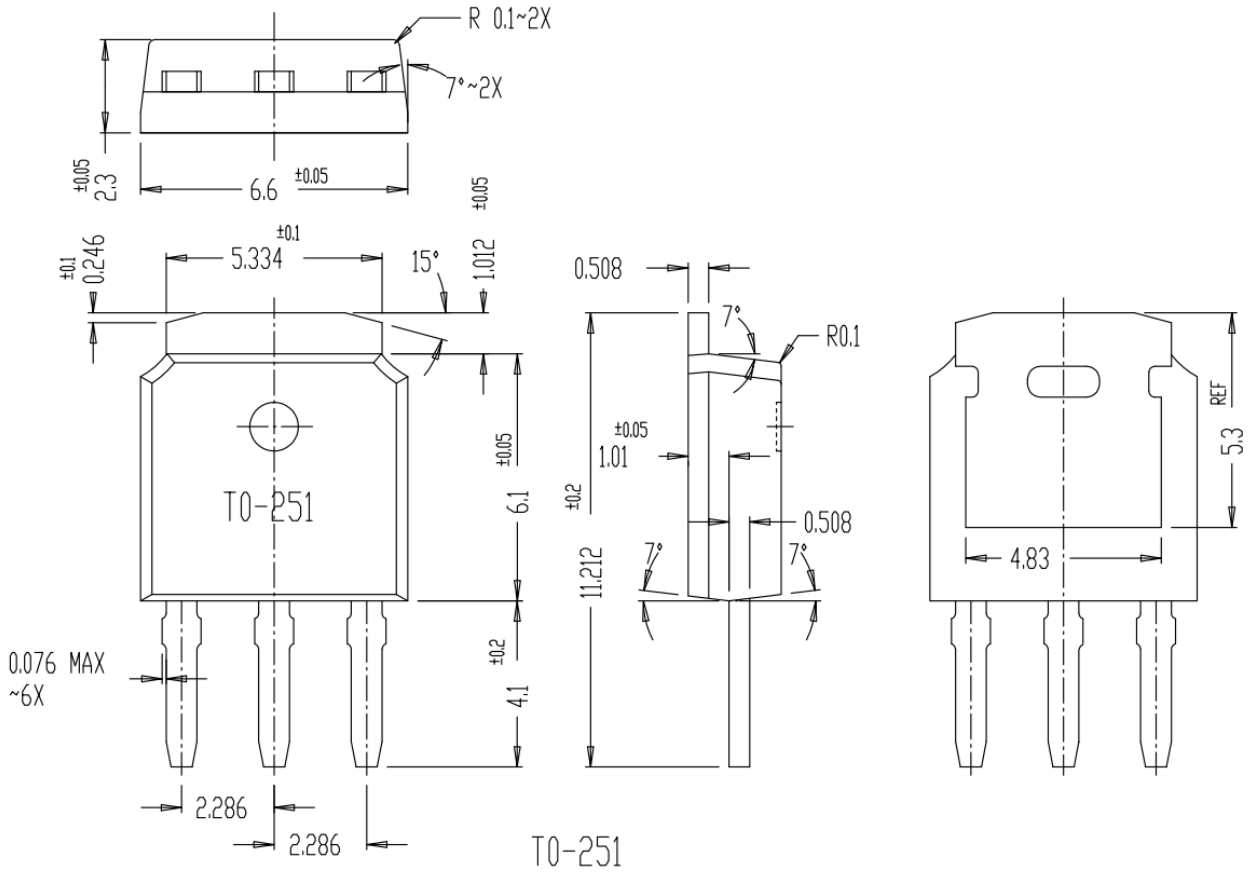
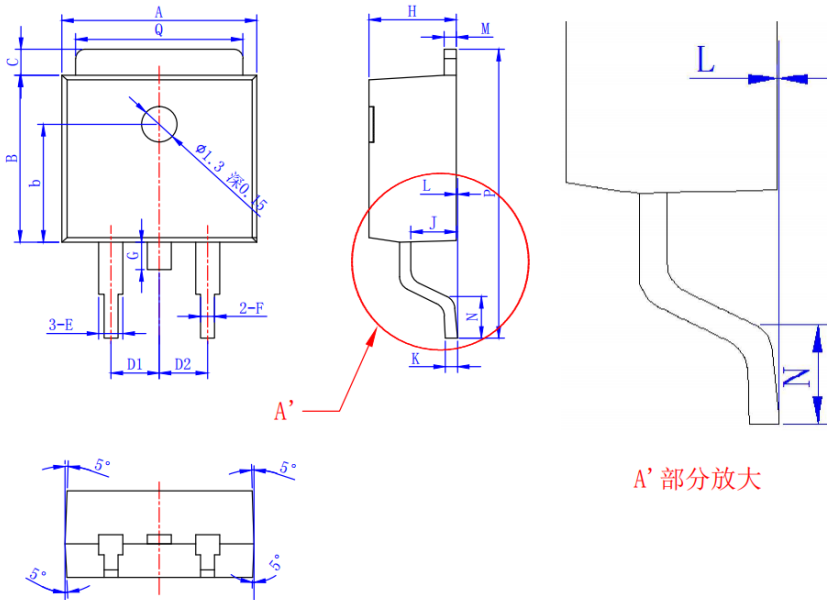


Figure 10. Switching wave

TO-251 Package Outline Drawing



TO-252 Package Outline Drawing



Symbol	MM		
	Min	Nom	Max
A	6.30	6.55	6.90
B	5.90	6.10	6.30
b	4.10	4.30	4.50
C	0.90	1.00	1.10
D1		2.29BSC	
D2		2.29BSC	
E	0.61	0.76	0.91
F	0.50	0.60	0.70
G	0.60	0.80	1.00
H	2.10	2.30	2.50
J	0.90	1.00	1.10
K	0.40	0.50	0.60
L	0.00	0.05	0.127
M	0.45	0.50	0.55
N	1.39	—	1.77
P	9.60	9.90	10.30
Q	5.10	5.30	5.50

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