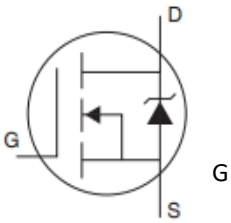
Description

The CM65R640XP is the N-Channel enhancement mode power field effect transistors with high cell density, high voltage Super Junction technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance, .

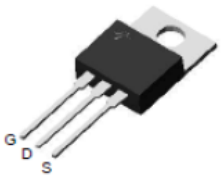
Features

- VDS: 650V
- ID (@VGS=10V): 7A
- RDS_{ON} (@VGS=10V) : < 612mΩ
- High density cell design for extremely low RDS_{ON}
- Excellent on-resistance and DC current capability

Equivalent Circuit and Pin Configuration



TO-220



G

Applications

- AC/DC load switch
- SMPS
- LED power

Marking Information

65R640XP
XXXX

X=Package type

XXXX = Marking Code

Ordering Information

P/N	Package Type	Packaging
CM65R640XP	TO-220	Tube

Absolute Maximum Ratings (Tc=25 ℃ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		VDS	650	V
Gate-source Voltage		VGS	±30	V
Continuous Drain Current (1)	Tc=25°C	ID	7(4)	A
	Tc=100°C		4.2(4)	A
Pulsed Drain Current(2)		IDM	28(4)	A
Total Power Dissipation (3)		PD @ Tc=25°C	83	W
		Derating Factor above 25°C	1.67	W/°C
Thermal Resistance Junction-to-Case (3)		RθJC	1.5	°C/W
Junction and Storage Temperature Range		TJ,TSTG	-55 to +150	°C

Electrical Characteristics (T_C=25 ℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	650			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=650V,V_{GS}=0V,T_C=25°C			5	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±30V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2.0		4.0	V
Static Drain-Source on-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=3.5A		510	612	mΩ
Diode Forward Voltage	V_{SD}	I_S=7A,V_{GS}=0V		0.85	1.3	V
Maximum Body-Diode Continuous Current	I_S				7	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=100V,V_{GS}=0V,f=1MHz		410		pF
Output Capacitance	C_{oss}			28		
Reverse Transfer Capacitance	C_{rss}			3		
Switching Parameters						
Total Gate Charge	Q_g	V_{DS}=480V,I_D=3.5A,V_{GS}=10V		16.8		nC
Gate Source Charge	Q_{gs}			2		
Gate Drain Charge	Q_{gd}			10.2		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=50V, R_L=15Ω,R_{GEN}=25Ω		46		ns
Turn-on Rise Time	t_r			39.3		
Turn-off Delay Time	$t_{D(off)}$			59		
Turn-off Fall Time	t_f			28.2		

Noted: (1) Pulse Test: Pulse Width≤300us,Duty cycle ≤2%

(2) Pulse width limited by maximum junction temperature

(3) Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. With 2oz Copper, t≤10s

(4) Drain current limited by maximum junction temperature

Typical Performance Characteristics

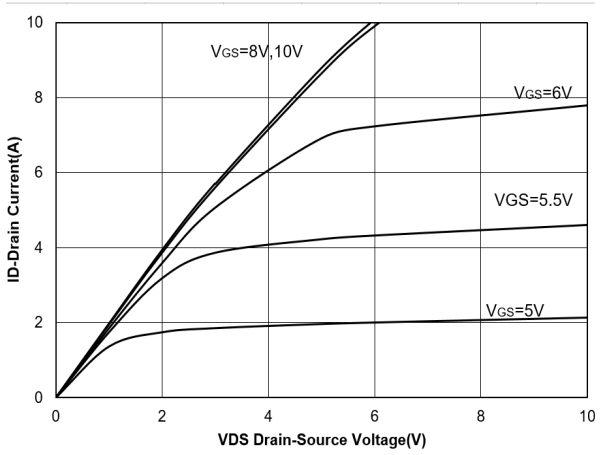


Figure 1. Output Characteristics

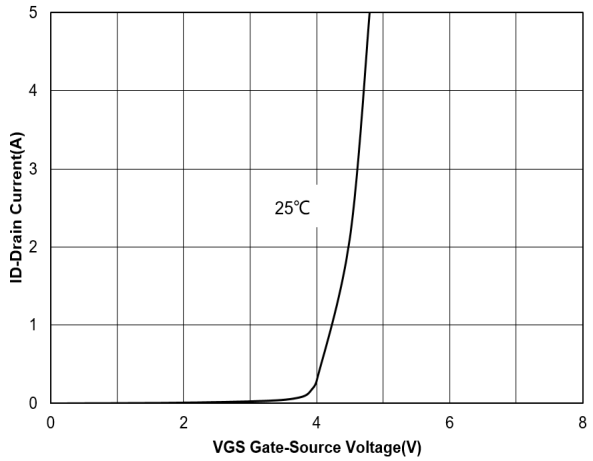


Figure 2. Transfer Characteristics

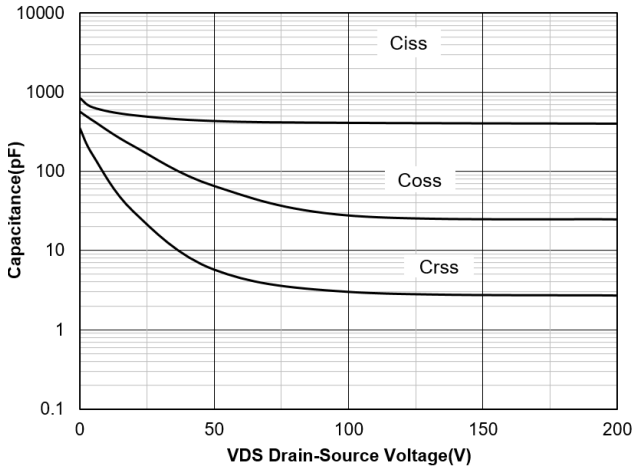


Figure 3. Capacitance Characteristics

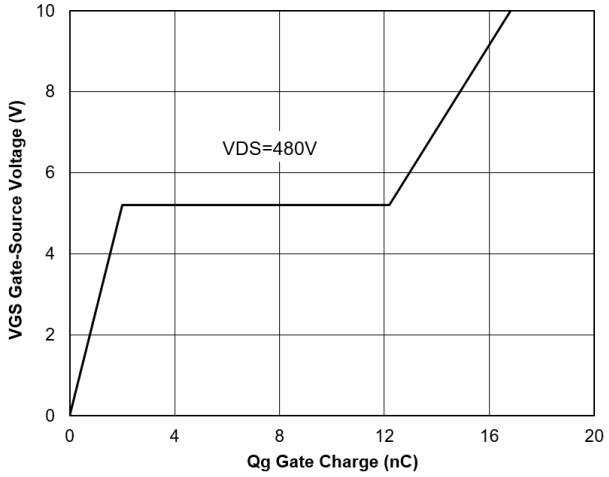


Figure 4. Gate Charge

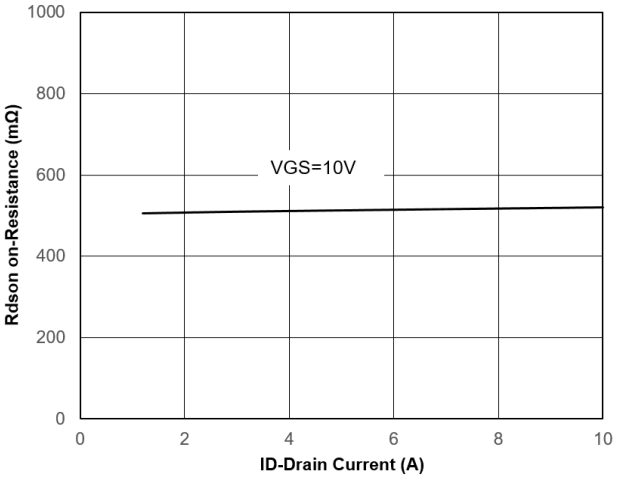


Figure 5. Drain-Source on Resistance

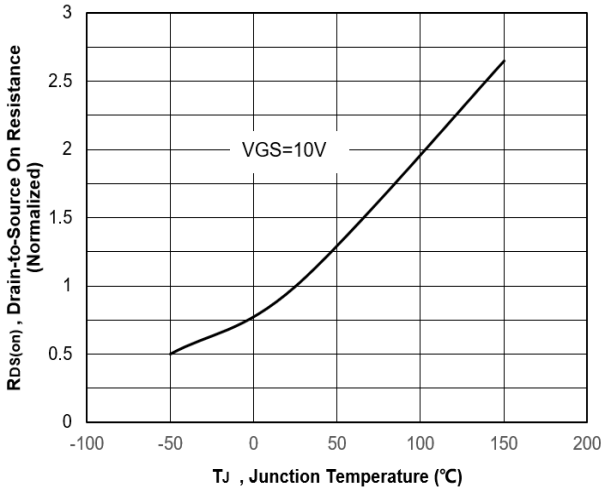


Figure 6. Normalized On-Resistance Vs. Temperature

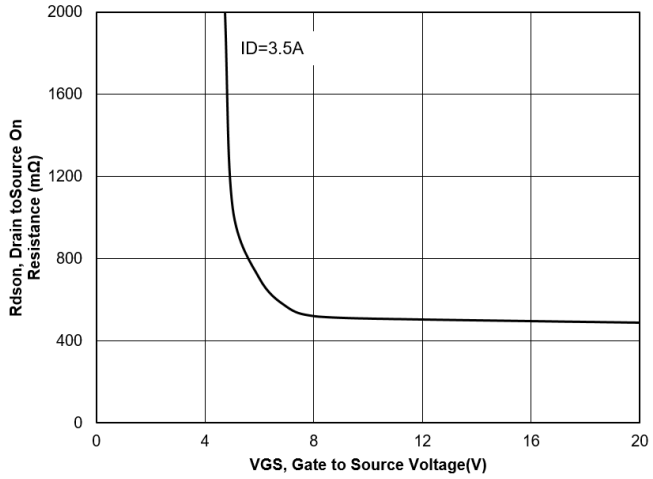


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

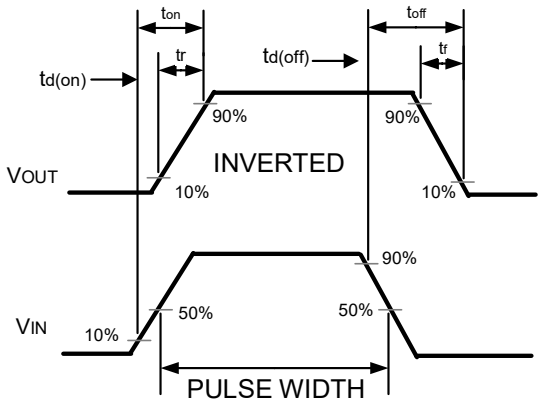


Figure 8. Switching wave

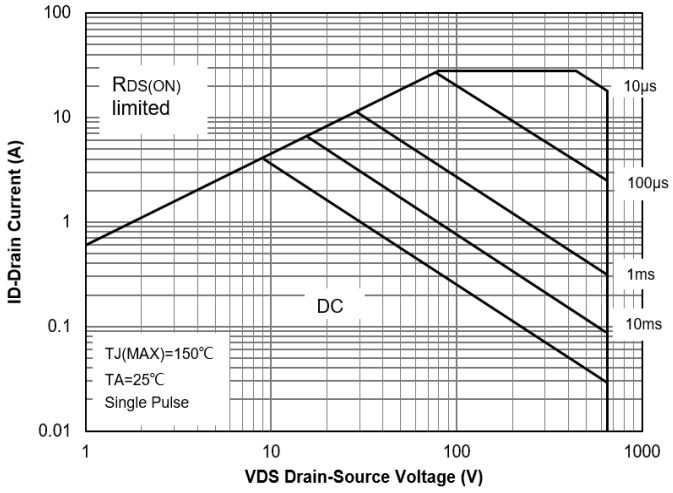


Figure 9. Safe Operation Area
（TO-220）

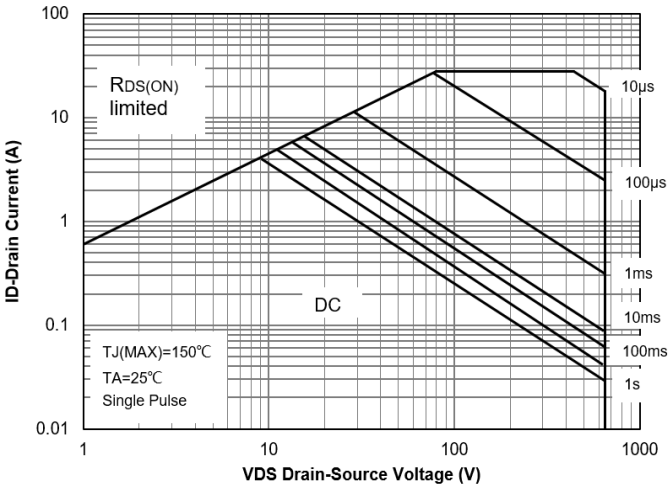


Figure 10. Safe Operation Area
（TO-220F）

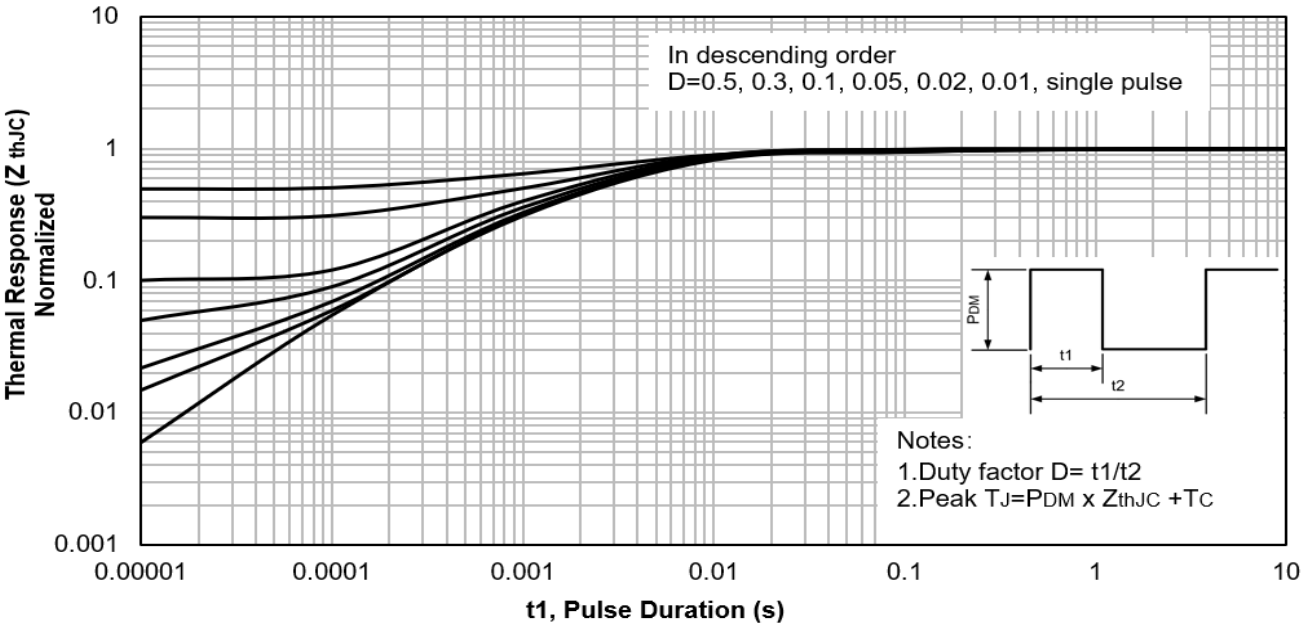


Figure 11. Maximum Effective Transient Thermal Impedance ,Junction-to-Case (TO-220)

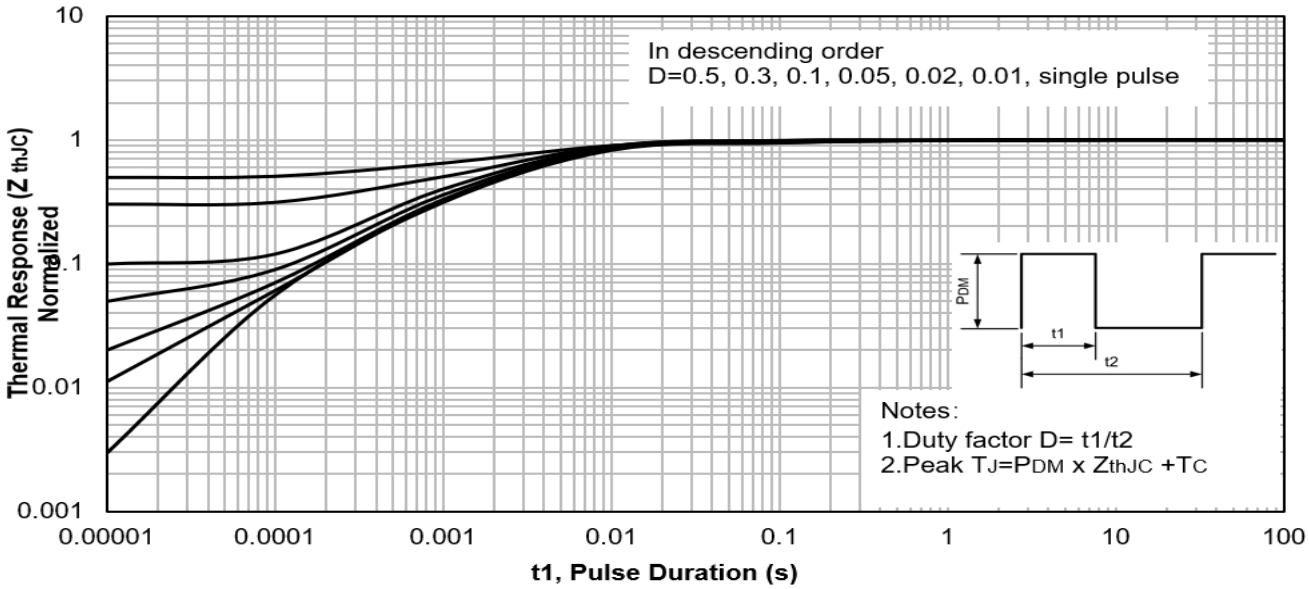
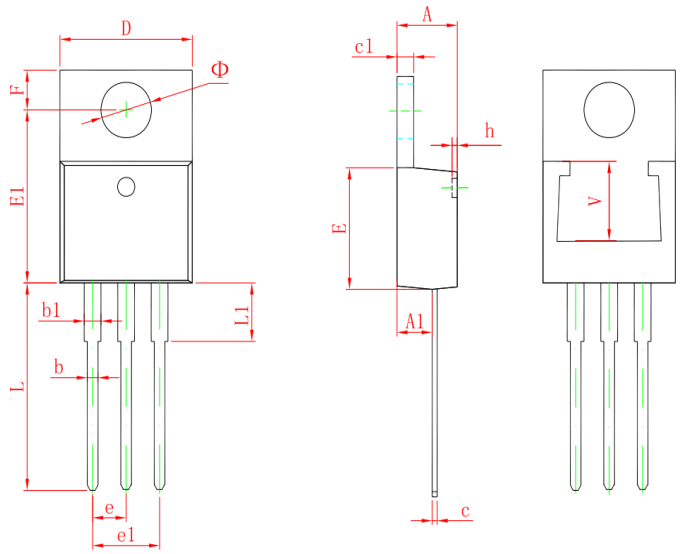


Figure 12. Maximum Effective Transient Thermal Impedance ,Junction-to-Case (TO-220F)

TO-220 Package Outline Drawing



Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.470	4.670	0.176	0.184
A1	2.520	2.820	0.099	0.111
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
E1	12.060	12.460	0.475	0.491
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.590	2.890	0.102	0.114
h	0.000	0.300	0.000	0.012
L	13.400	13.800	0.528	0.543
L1	3.560	3.960	0.140	0.156
Φ	3.735	3.935	0.147	0.155
V	5.600 REF.		0.220 REF.	