

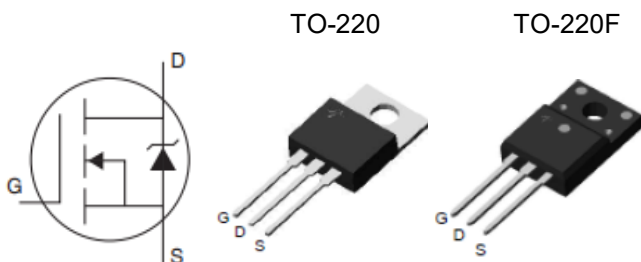
### Description

The CM65R175P/F is the N-Channel enhancement mode power field effect transistors with high cell density, high voltage Super Junction technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

### Features

- VDS: 650V
- ID (@VGS=10V): 21A
- RDS<sub>ON</sub> (@VGS=10V): < 175mΩ
- High density cell design for extremely low RDS<sub>ON</sub>
- Excellent on-resistance and DC current capability

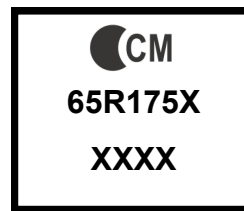
### Equivalent Circuit and Pin Configuration



### Applications

- AC/DC load switch
- SMPS
- LED power

### Marking Information



X=Package type

XXXX = Marking Code

### Ordering Information

P/N	Package Type	Packaging
CM65R175P	TO-220	Tube
CM65R175F	TO-220F	Tube

### Absolute Maximum Ratings (T<sub>c</sub>=25 °C unless otherwise noted)

Parameter	Symbol	Maximum		Unit	
		CM65R175P	CM65R175F		
Drain-source Voltage	V <sub>DS</sub>	650		V	
Gate-source Voltage	V <sub>GS</sub>	±30		V	
Continuous Drain Current <sup>(1)</sup>	I <sub>D</sub>	T <sub>c</sub> =25°C	21	21 <sup>(4)</sup>	A
		T <sub>c</sub> =100°C	13	13 <sup>(4)</sup>	A
Pulsed Drain Current <sup>(2)</sup>	I <sub>DM</sub>	84	84 <sup>(4)</sup>	A	
Total Power Dissipation <sup>(3)</sup>	PD @ T <sub>c</sub> =25°C	208	35	W	
	Derating Factor above 25°C	1.67	0.3	W/°C	
Thermal Resistance Junction-to-Case <sup>(3)</sup>	R <sub>θJC</sub>	0.6	3.6	°C/W	
Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150		°C	

**Electrical Characteristics (T<sub>c</sub>=25 °C unless otherwise noted)**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	B <sub>V</sub> D <sub>SS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	650			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =650V, V <sub>GS</sub> =0V, T <sub>C</sub> =25°C			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±30V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2.0		4.0	V
Static Drain-Source on-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =10.5A		140	175	mΩ
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =21A, V <sub>GS</sub> =0V			1.4	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				21	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V, f=1MHz		1550		pF
Output Capacitance	C <sub>oss</sub>			67		
Reverse Transfer Capacitance	C <sub>rss</sub>			1.5		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =480V, I <sub>D</sub> =10.5A, V <sub>GS</sub> =10V		38		nC
Gate Source Charge	Q <sub>gs</sub>			6.6		
Gate Drain Charge	Q <sub>gd</sub>			15.2		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =60V, I <sub>D</sub> =4A, R <sub>GEN</sub> =25Ω		48		ns
Turn-on Rise Time	t <sub>r</sub>			57		
Turn-off Delay Time	t <sub>D(off)</sub>			80		
Turn-off Fall Time	t <sub>f</sub>			48		

Noted: (1) Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%

(2) Pulse width limited by maximum junction temperature

(3) Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. With 2oz Copper, t ≤ 10s

(4) Drain current limited by maximum junction temperature

**Typical Performance Characteristics**

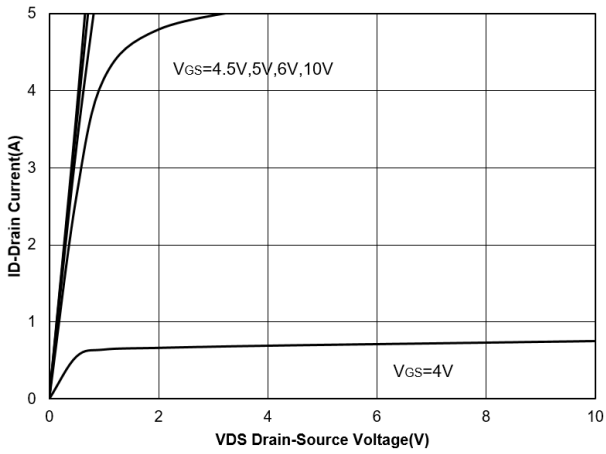


Figure 1. Output Characteristics

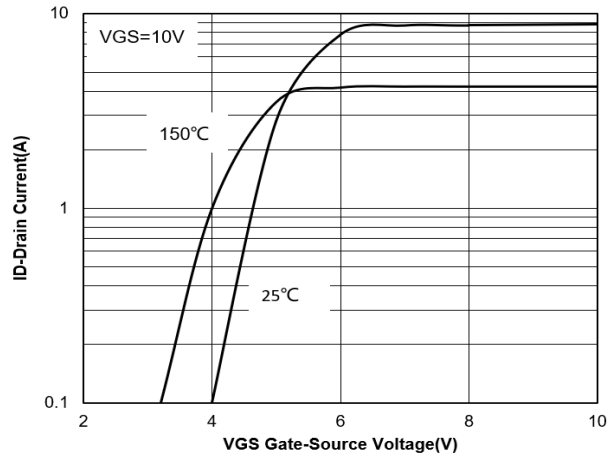


Figure 2. Transfer Characteristics

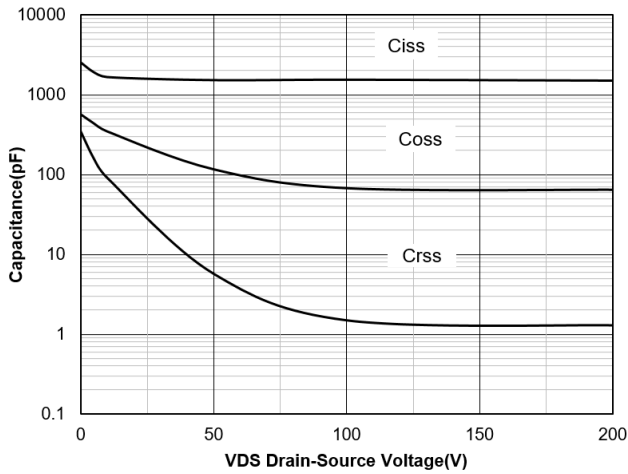


Figure 3. Capacitance Characteristics

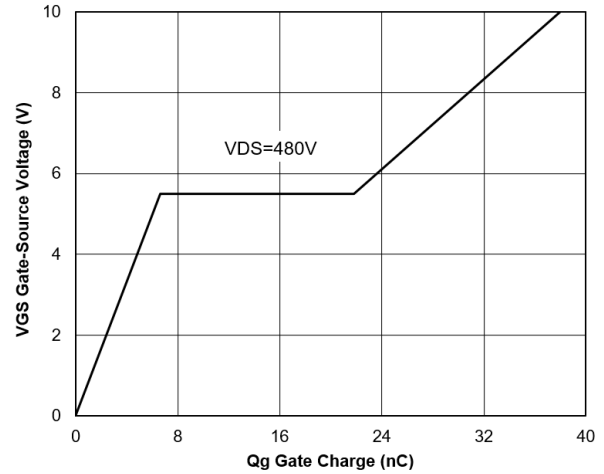


Figure 4. Gate Charge

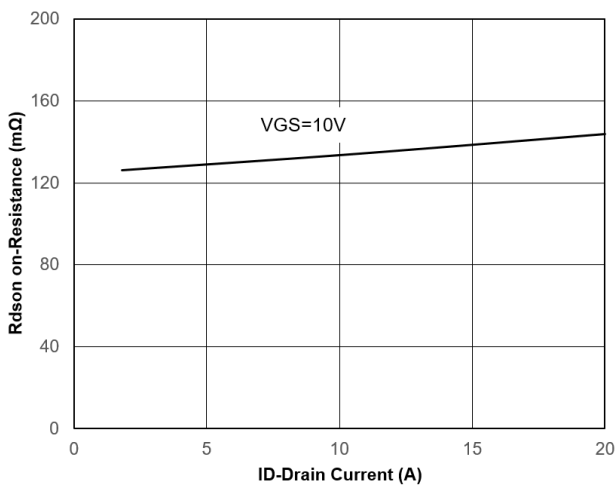


Figure 5. Drain-Source on Resistance

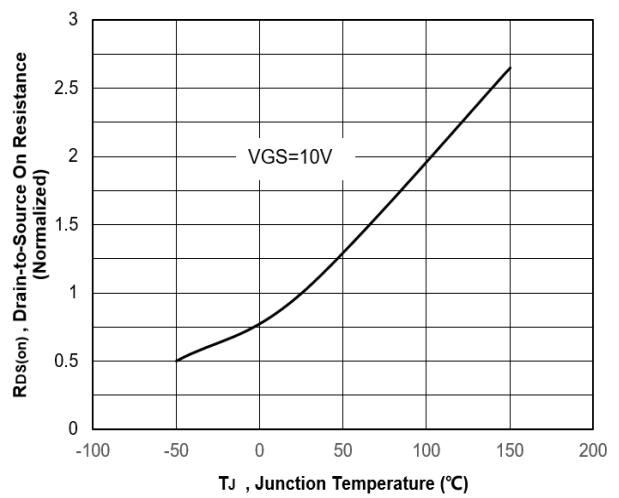


Figure 6. Normalized On-Resistance Vs. Temperature

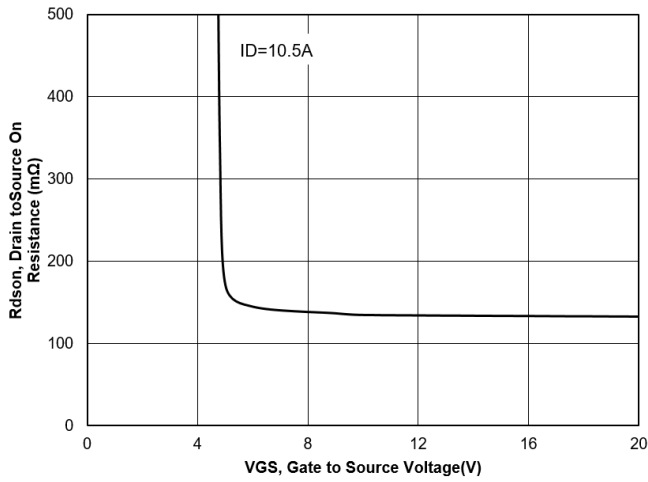


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

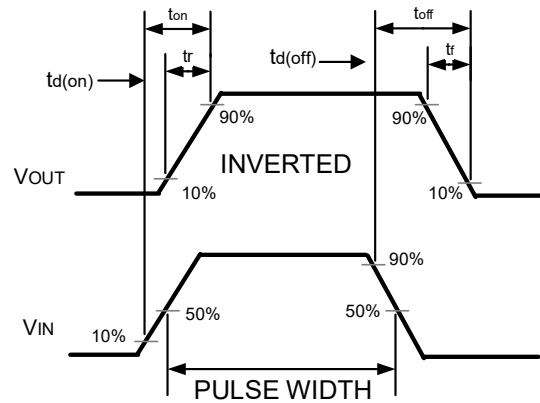


Figure 8. Switching wave

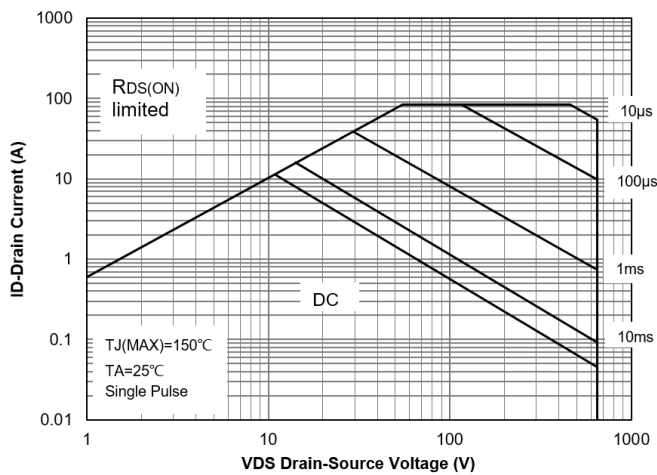


Figure 9. Safe Operation Area (TO-220)

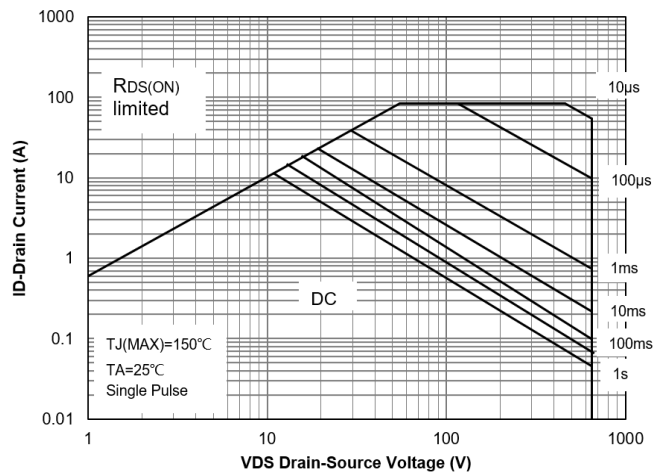


Figure 10. Safe Operation Area (TO-220F)

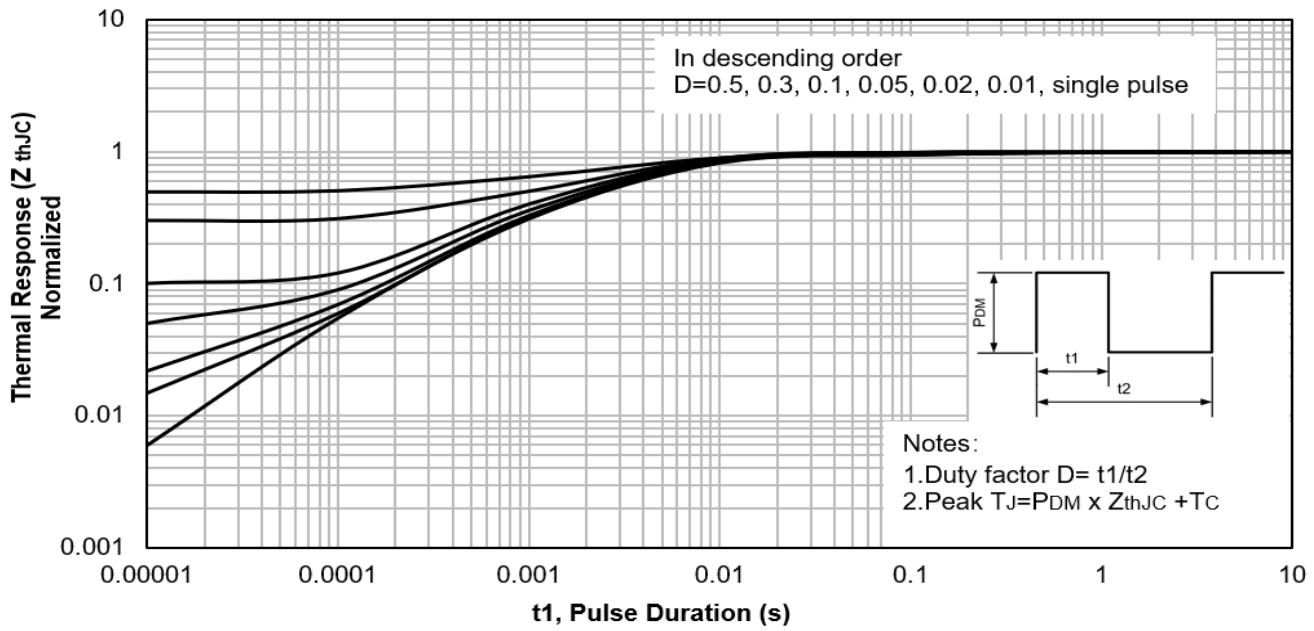


Figure 11. Maximum Effective Transient Thermal Impedance ,Junction-to-Case (TO-220)

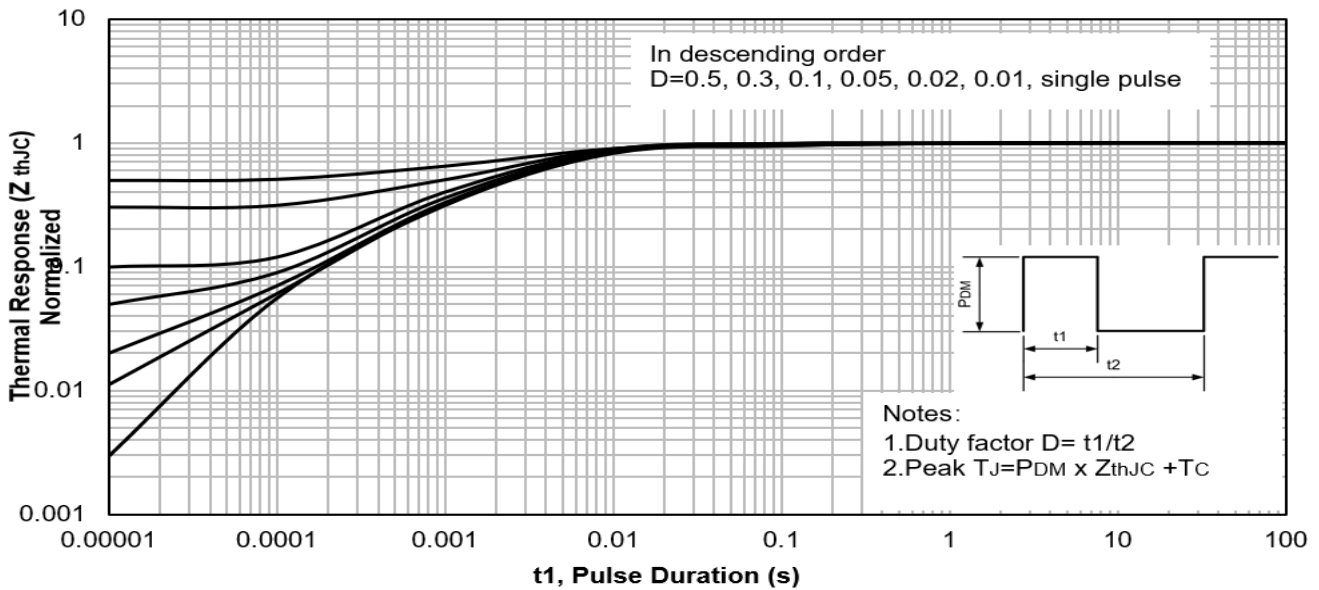
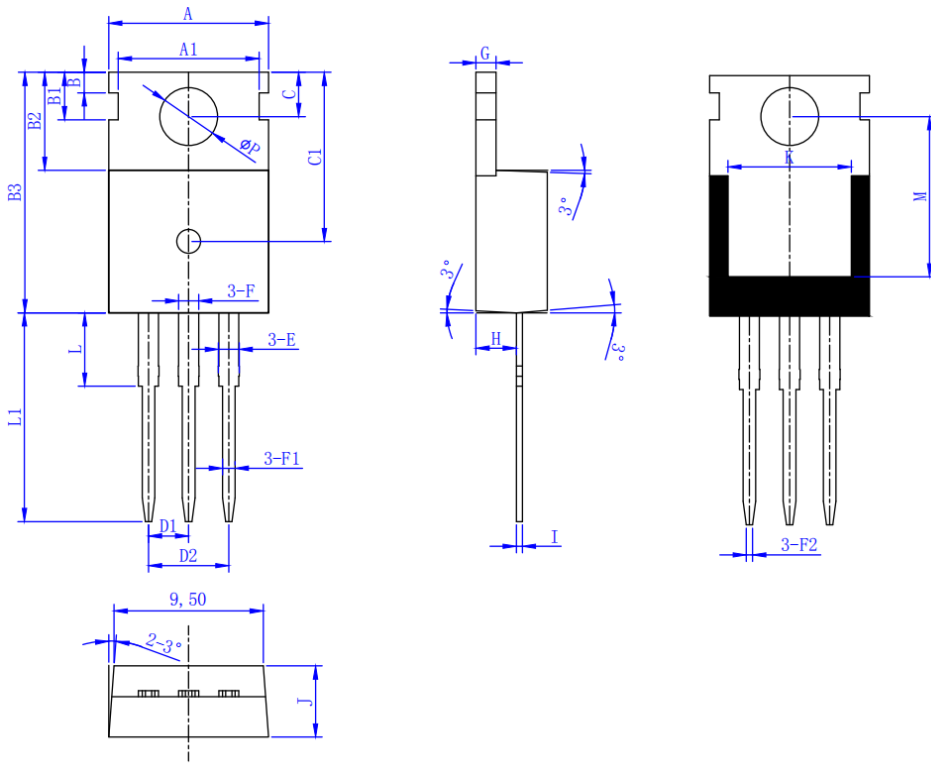
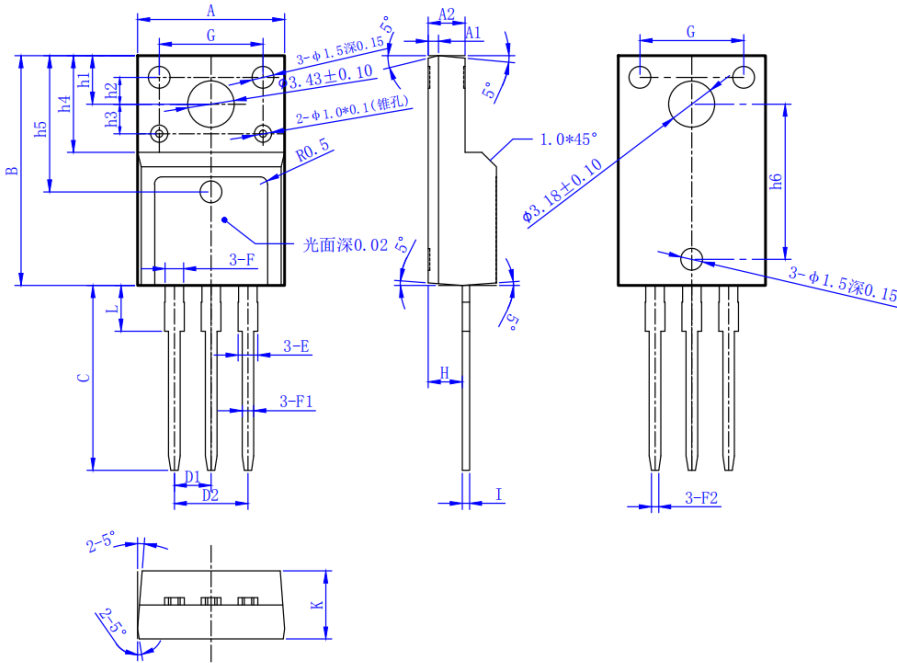


Figure 12. Maximum Effective Transient Thermal Impedance ,Junction-to-Case (TO-220F)

**TO-220 Package Outline Drawing**


Symbol	Millimeters		
	Min.	Nom.	Max.
A	9.90	10.00	10.10
A1		8.70	
B		1.30	
B1		3.00	
B2		6.48	
B3	15.60	15.78	16.00
C		2.80	
C1		11.08	
D1		2.54BSC	
D2		5.08BSC	
E	1.27	1.30	1.35
F	1.15	1.25	1.35
F1	0.70	0.80	0.90
F2	0.30	0.40	0.50
G	1.25	1.30	1.35
H	2.30	2.50	2.70
I	0.45	0.50	0.60
J	4.40	4.50	4.60
K	7.50	7.60	7.70
L	2.68	2.88	3.08
L1	12.95	13.00	13.15
M		10.50	
N	9.40	9.50	9.65
ΦP	3.60	3.65	3.70

**TO-220F Package Outline Drawing**


Symbol	Millimeters		
	Min.	Nom.	Max.
A	10.00	10.20	10.40
A1		0.70	
A2	2.35	2.55	2.75
B	15.70	15.90	16.10
C	13.00	13.25	13.50
D1		2.54 BSC	
D2		5.08 BSC	
E	1.27	1.32	1.40
F	1.25	1.28	1.30
F1	0.75	0.80	0.85
F2	0.35	0.40	0.50
G	6.90	7.00	7.10
H	2.66	2.76	2.86
h1	3.20	3.30	3.40
h2	1.70	1.80	1.90
h3	2.00	2.10	2.20
h4	6.70	6.79	6.90
h5	9.30	9.41	9.50
h6	10.44	10.54	10.64
I	0.40	0.50	0.60
K	4.60	4.70	4.80
L	2.90	3.00	3.10