Description

The CM60N10AGP is the N-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

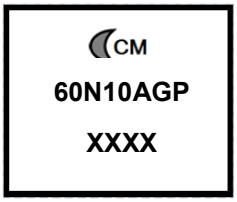
Applications

- Battery management
- Power management
- Load switch

Features

- V_{DS}: 100V
- I_D: 77A
- $R_{DS_{ON}}$ (@V_{GS}=10V) : < 9.5mΩ
- High density cell design for extremely low $R_{DS_{ON}}$
- Excellent on-resistance and DC current capability

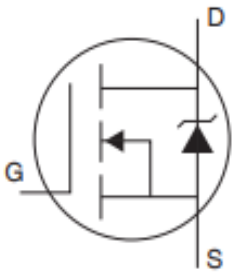
Marking Information



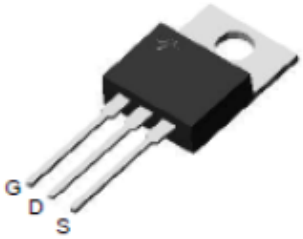
Marking Code = CM60N10AGP

Date Code = XXXX

Equivalent Circuit and Pin Configuration



TO-220



Ordering Information

Part Number	Package Type	Packaging
CM60N10AGP	TO-220	Tube

Absolute Maximum Ratings (T_A=25 ℃ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	±20	V
Continuous Drain Current (1)	T_C=25°C	I_D	77	A
	T_C=100°C		55	A
Pulsed Drain Current(2)		I_{DM}	308	A
Total Power Dissipation (3)		P_D @ T_C=25°C	107	W
		Derating Factor above 25°C	0.71	W/°C
Thermal Resistance Junction-to-Case (3)		$R_{\theta JC}$	1.4	°C/W
Junction and Storage Temperature Range		T_J,T_{STG}	-55 to +175	°C

Electrical Characteristics (T_J=25 ℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V,T_C=25°C			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2.0		4.0	V
Static Drain-Source on-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=20A		7.5	9.5	mΩ
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V			1.2	V
Maximum Body-Diode Continuous Current	I_S				60	A
Dynamic Parameters						
Input Capacitance	Ciss	V_{DS}=50V,V_{GS}=0V,f=1MHz		1780		pF
Output Capacitance	Coss			348		
Reverse Transfer Capacitance	Crss			6.8		
Switching Parameters						
Total Gate Charge	Qg	V_{GS}=10V,V_{DS}=50V,I_D=25A		28		nC
Gate Source Charge	Qgs			8.8		
Gate Drain Charge	Qgd			7.8		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=30V, R_L=30Ω, I_D=1A，R_{GEN}=6Ω		20		ns
Turn-on Rise Time	tr			8		
Turn-off Delay Time	$t_{D(off)}$			30		
Turn-off Fall Time	tf			65		

Noted: (1) Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

(2) Pulse width limited by maximum junction temperature.

(3) Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. With 2oz Copper, t≤10s.

Typical Performance Characteristics

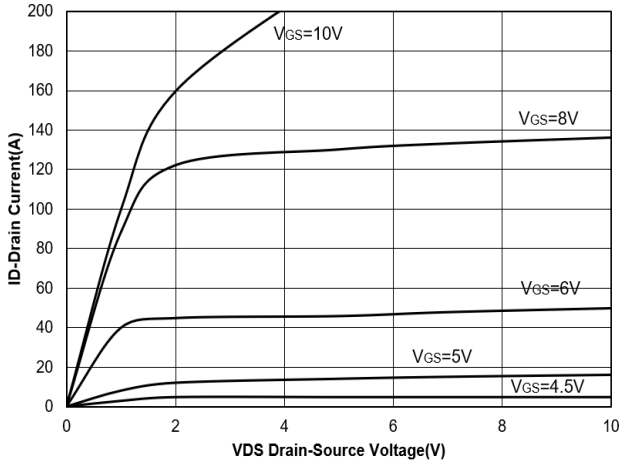


Figure 1. Output Characteristics

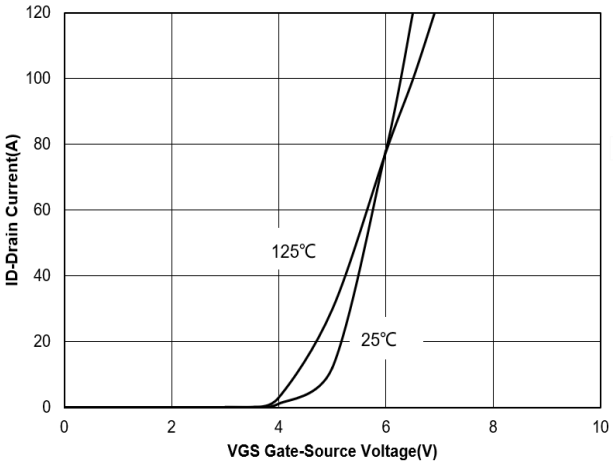


Figure 2. Transfer Characteristics

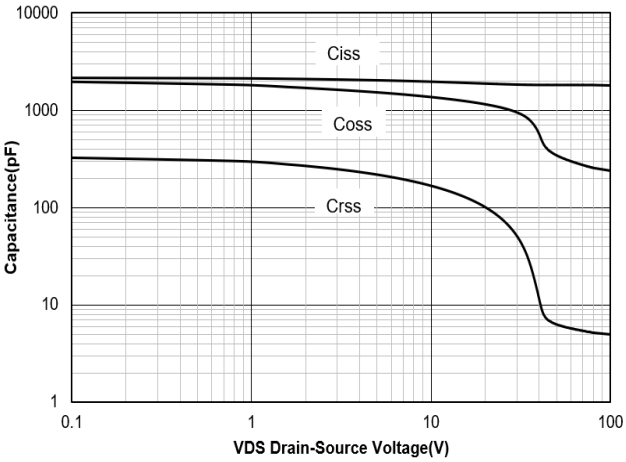


Figure 3. Capacitance Characteristics

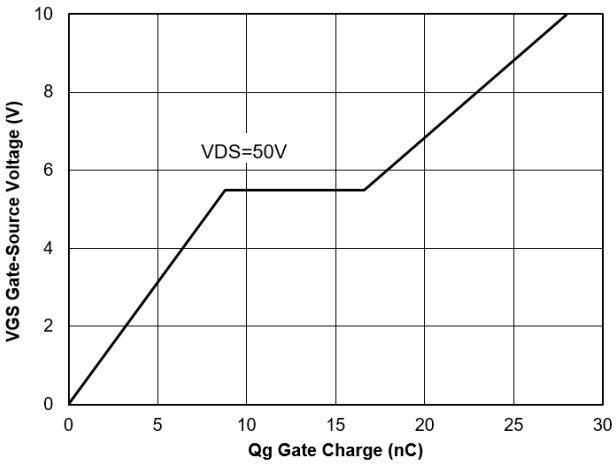


Figure 4. Gate Charge

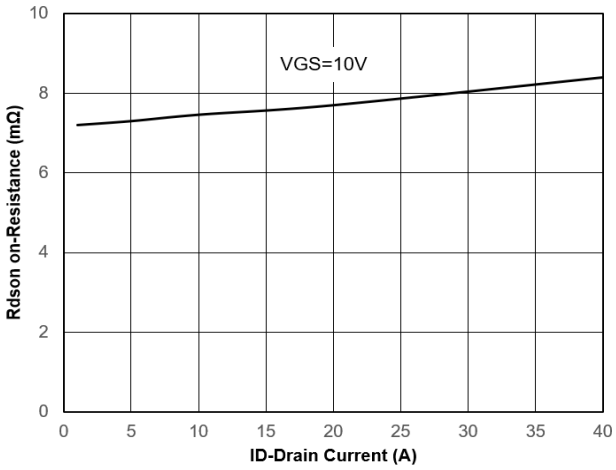


Figure 5. Drain-Source on Resistance

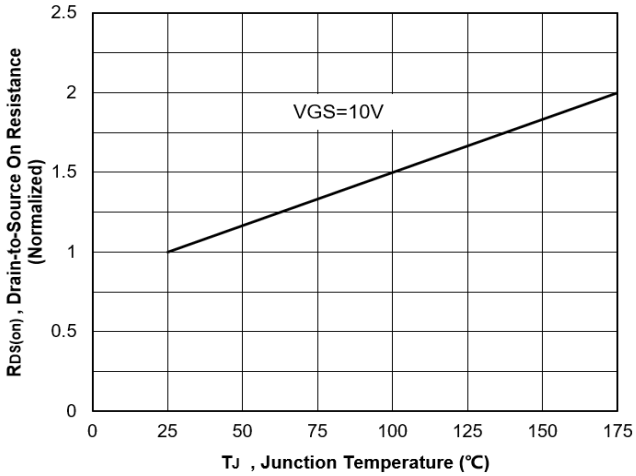


Figure 6. Normalized On-Resistance Vs. Temperature

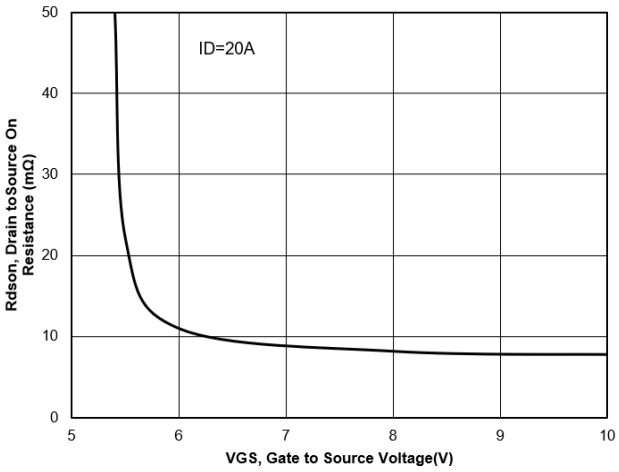


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

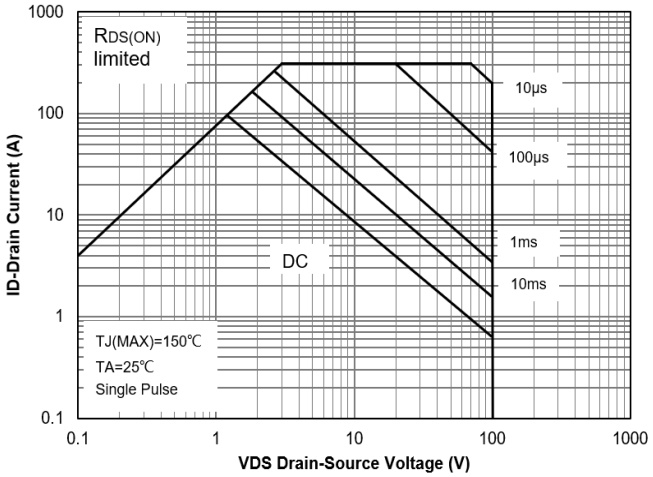


Figure 8. Safe Operation Area

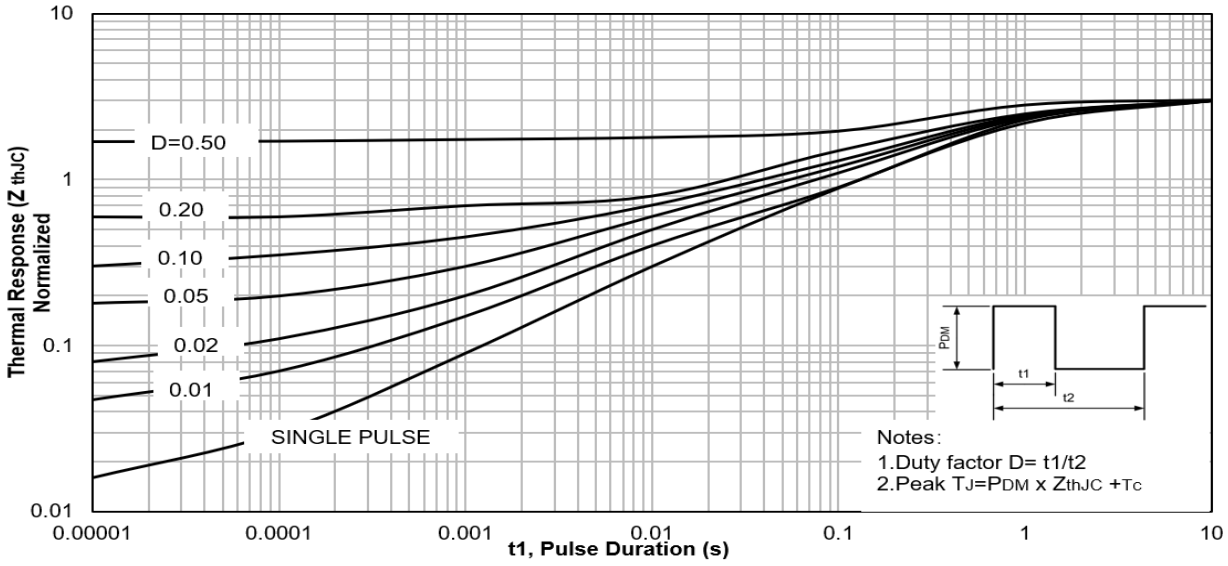


Figure 9. Maximum Effective Transient Thermal Impedance ,Junction-to-Case

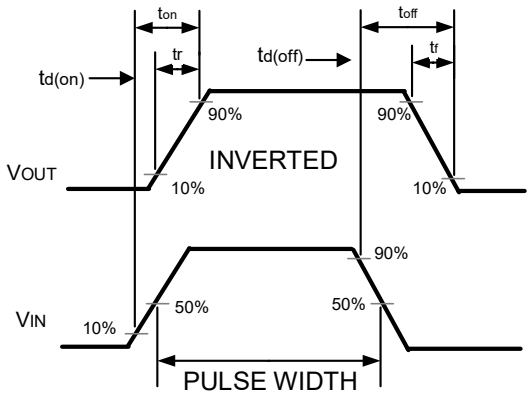
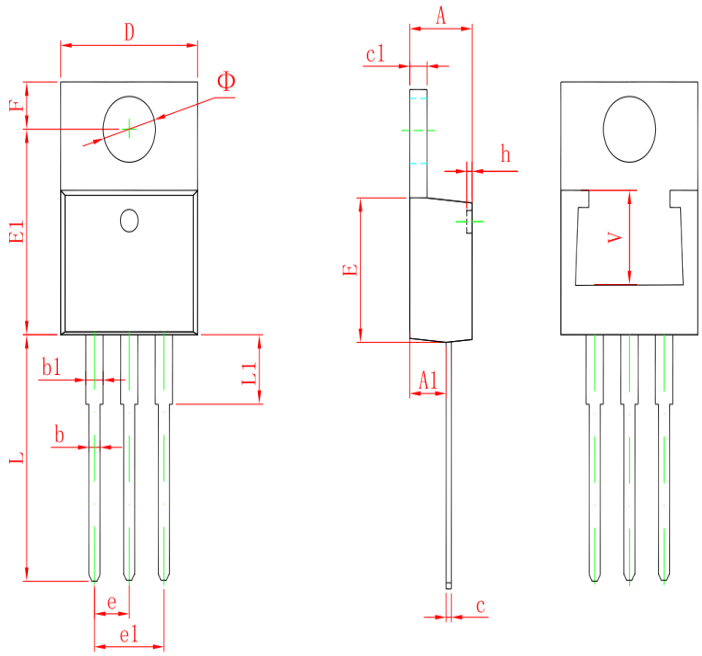


Figure 10. Switching wave

TO-220 Package Outline Drawing



Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.470	4.670	0.176	0.184
A1	2.520	2.820	0.099	0.111
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
E1	12.060	12.460	0.475	0.491
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.590	2.890	0.102	0.114
h	0.000	0.300	0.000	0.012
L	13.400	13.800	0.528	0.543
L1	3.560	3.960	0.140	0.156
Φ	3.735	3.935	0.147	0.155
V	5.600 REF.		0.220 REF.	