

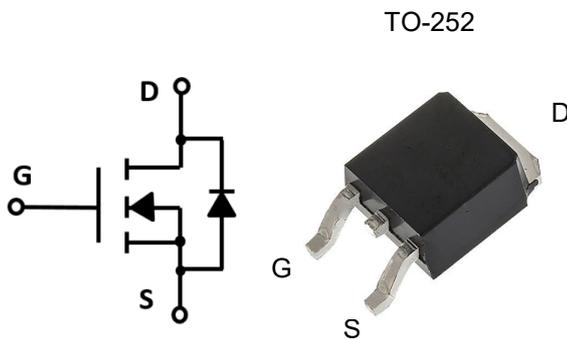
Description

The CM45N10GU is the N-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

Features

- VDS: 100V
- ID : 47A
- RDS_{ON} (@VGS=10V) : < 17.5mΩ
- RDS_{ON} (@VGS=4.5V) : < 22mΩ
- High density cell design for extremely low RDS_{ON}
- Excellent on-resistance and DC current capability

Equivalent Circuit and Pin Configuration



Applications

- AC/DC load switch
- SMPS
- LED power

Marking Information



Marking Code = 45N10GU

Date Code = XXXX

Ordering Information

Part Number	Packaging	Remark
CM45N10GU	2500/Tape & Reel	ROHS

Absolute Maximum Ratings (T_c=25 °C unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	V _{DS}	100	V
Gate-source Voltage	V _{GS}	±20	V
Continuous Drain Current	I _D	T _c =25°C	47
		T _c =70°C	30
Pulsed Drain Current ⁽¹⁾	I _{DM}	188	A
Total Power Dissipation ⁽²⁾	P _D @ T _c =25°C	75	W
	Derating Factor above 25°C	0.6	W/°C
Thermal Resistance Junction-to-Case ⁽²⁾	R _{θJC}	1.67	°C/W
Junction and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

Electrical Characteristics (T_c=25 °C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BVDSS	V _{GS} =0V, I _D =250μA	100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V, T _C =25°C			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0		3.0	V
Static Drain-Source on-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A		14	17.5	mΩ
		V _{GS} =4.5V, I _D =20A		17	22	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V			1.3	V
Maximum Body-Diode Continuous Current	I _S				47	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHz		1136		pF
Output Capacitance	C _{oss}			400		
Reverse Transfer Capacitance	C _{rss}			17		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =25A		16		nC
Gate Source Charge	Q _{gs}			5.5		
Gate Drain Charge	Q _{gd}			2.3		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _D =25A, R _{GEN} =2.2Ω		39		ns
Turn-on Rise Time	t _r			11		
Turn-off Delay Time	t _{D(off)}			53		
Turn-off Fall Time	t _f			16		

Noted: (1) Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

(2) Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch with 2oz. Copper, t ≤ 10s.

Typical Performance Characteristics

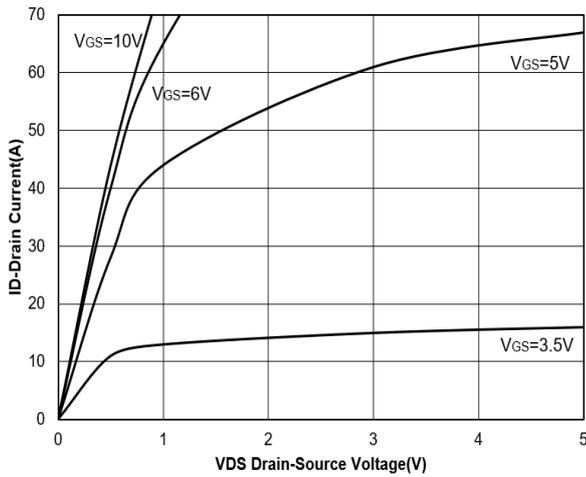


Figure 1. Output Characteristics

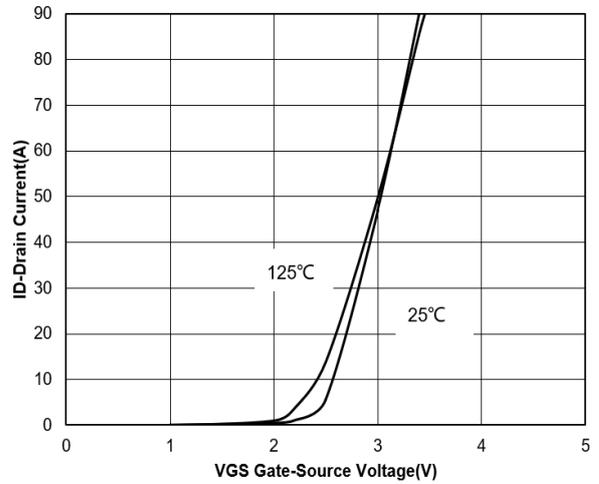


Figure 2. Transfer Characteristics

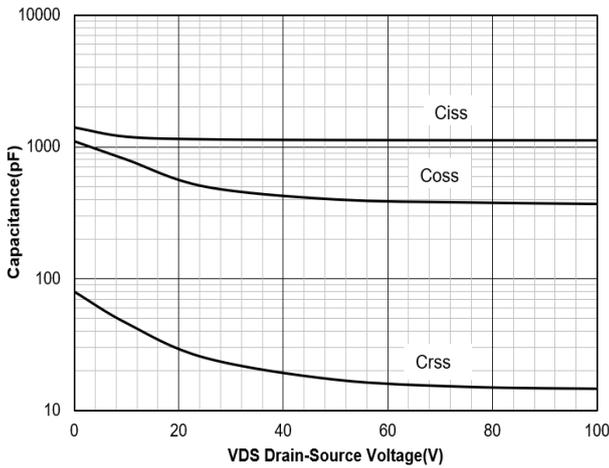


Figure 3. Capacitance Characteristics

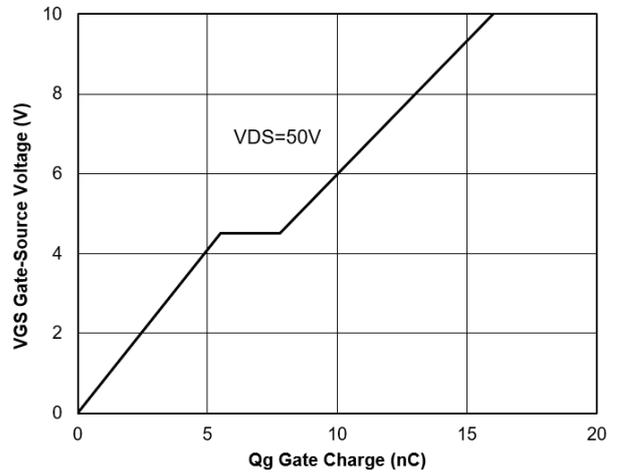


Figure 4. Gate Charge

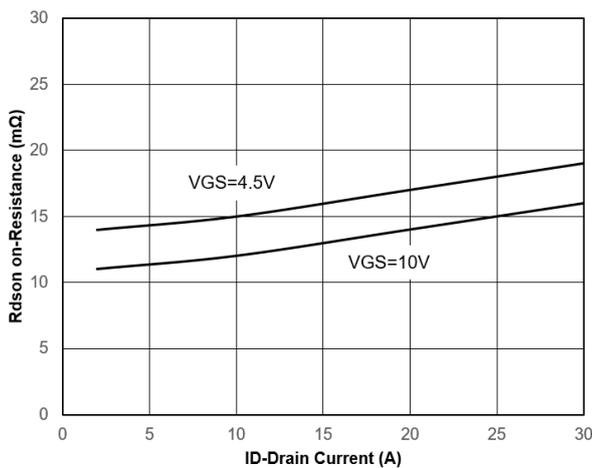


Figure 5. Drain-Source on Resistance

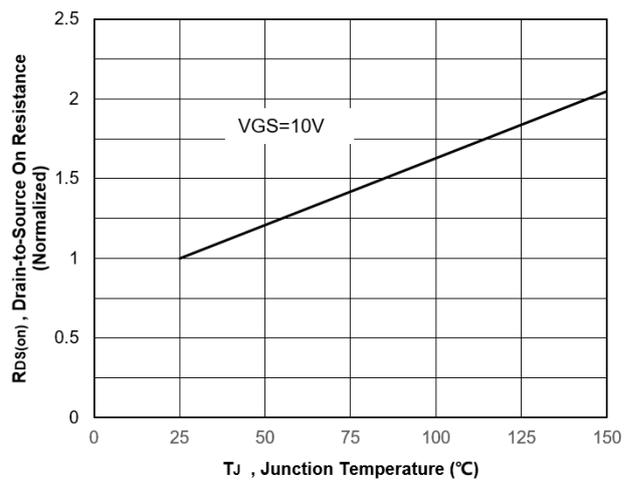


Figure 6. Normalized On-Resistance Vs. Temperature

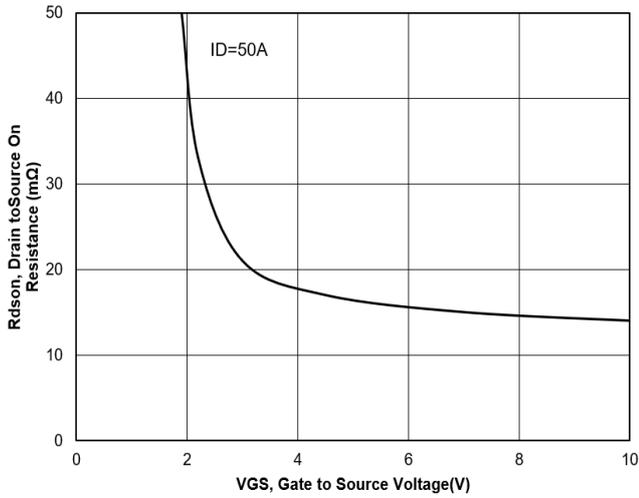


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

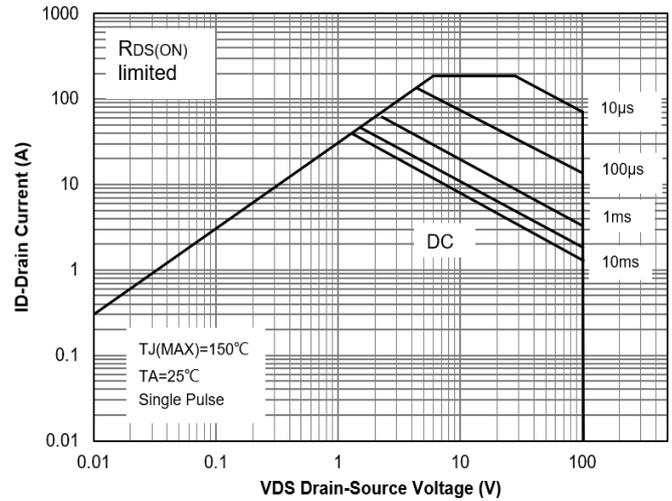


Figure 8. Safe Operation Area

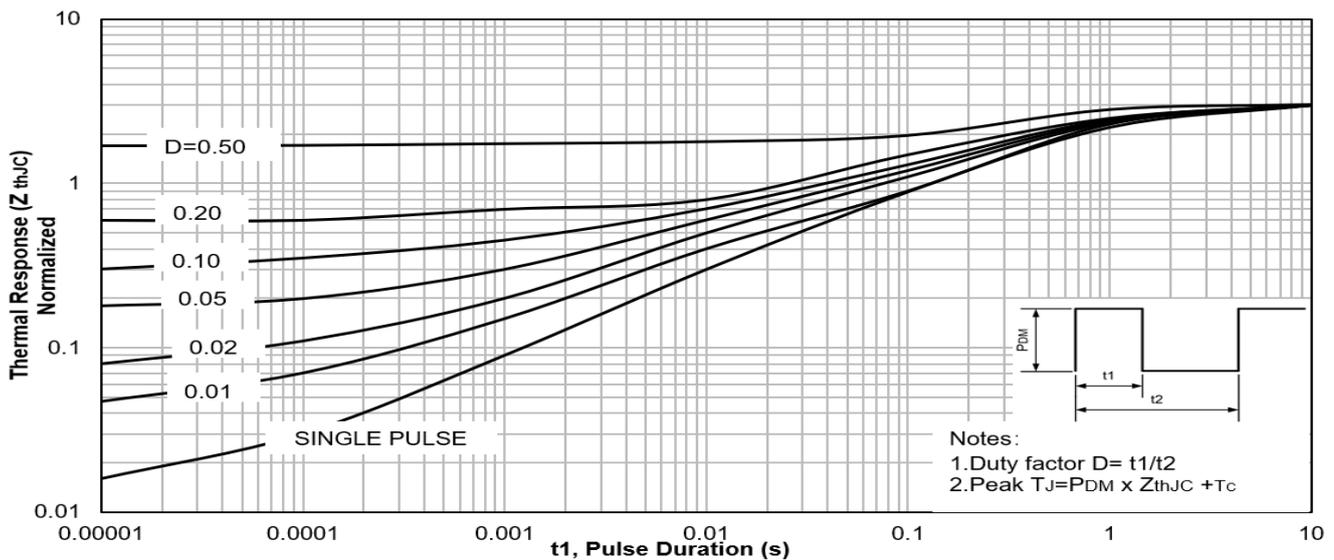


Figure 9. Maximum Effective Transient Thermal Impedance ,Junction-to-Case

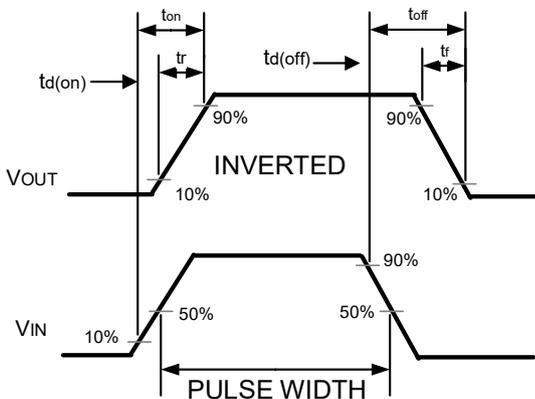
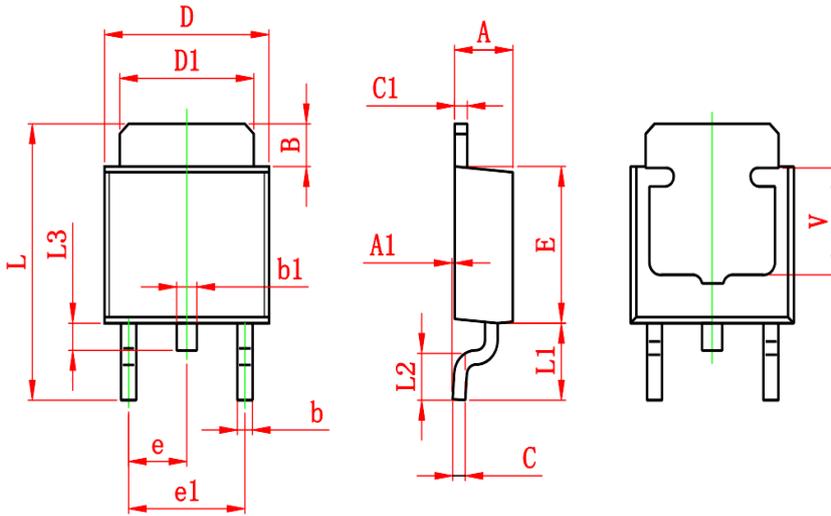


Figure 10. Switching wave

TO-252 Package Outline Drawing



Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP.		0.091 TYP.	
e1	4.500	4.700	0.177	0.185
L	9.500	9.900	0.374	0.390
L1	2.550	2.900	0.100	0.114
L2	1.400	1.780	0.055	0.070
L3	0.600	0.900	0.024	0.035
V	3.800 REF.		0.150 REF.	

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