Description

CM3139BT is the P-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

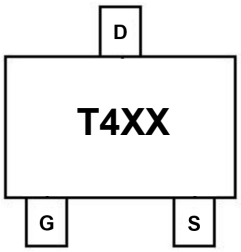
Features

- V_{DS}: -20V
- I_D: -0.5A
- $R_{DS_{ON}}$ (@V_{GS}=-4.5V) : < 850mΩ
- $R_{DS_{ON}}$ (@V_{GS}=-2.5V) : < 1200mΩ
- High density cell design for extremely low $R_{DS_{ON}}$
- Excellent on-resistance and DC current capability

Applications

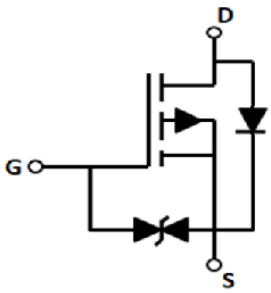
- Cellular Handsets and Accessories
- Personal Digital Assistants
- Portable Instrumentation
- Load switch

Marking Information



Device Code = T4
Date Code = XX

Equivalent Circuit and Pin Configuration



SOT-523 (Top View)

Ordering Information

Part Number	Packaging	Reel Size
CM3139BT	3000/Tape & Reel	7 inch

Absolute Maximum Ratings (T_A=25 ℃ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	-20	V
Gate-source Voltage		V_{GS}	±10	V
Continuous Drain Current	T_A=25°C , Steady State	I_D	-0.5	A
	T_A=75°C ,Steady State		-0.4	A
Pulsed Drain Current(1)		I_{DM}	-2	A
Total Power Dissipation @ T_A=25°C (2)	@Steady State	P_D	310	mW
Thermal Resistance Junction-to-Ambient (2)	@Steady State	$R_{\theta JA}$	400	°C/W
Junction and Storage Temperature Range		T_J,T_{STG}	-55 to +150	°C

Electrical Characteristics (T_J=25 ℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=-250μA	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V,V_{GS}=0V,T_C=25°C			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±10V,V_{DS}=0V			±10	uA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-0.35		-1.2	V
Static Drain-Source on-Resistance	$R_{DS(on)}$	V_{GS}=-4.5V,I_D=-0.5A		610	850	mΩ
		V_{GS}=-2.5V,I_D=-0.3A		930	1200	
Diode Forward Voltage	V_{SD}	I_S=-0.5A,V_{GS}=0V			-1.2	V
Maximum Body-Diode Continuous Current	I_S				-0.5	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-10V,V_{GS}=0V,f=1MHz		35		pF
Output Capacitance	C_{oss}			11		
Reverse Transfer Capacitance	C_{rss}			6		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-4.5V,V_{DS}=-10V,I_D=-0.5A		0.94		nC
Gate Source Charge	Q_{gs}			0.10		
Gate Drain Charge	Q_{gd}			0.14		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-4.5V,V_{DD}=-10V, R_L=2.5Ω,R_{GEN}=3Ω		9		ns
Turn-on Rise Time	t_r			7.8		
Turn-off Delay Time	$t_{D(off)}$			14		
Turn-off Fall Time	t_f			8.8		

Noted: (1) Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

(2) Surface mounted on FR4 board using the minimum recommended pad size.

Typical Performance Characteristics

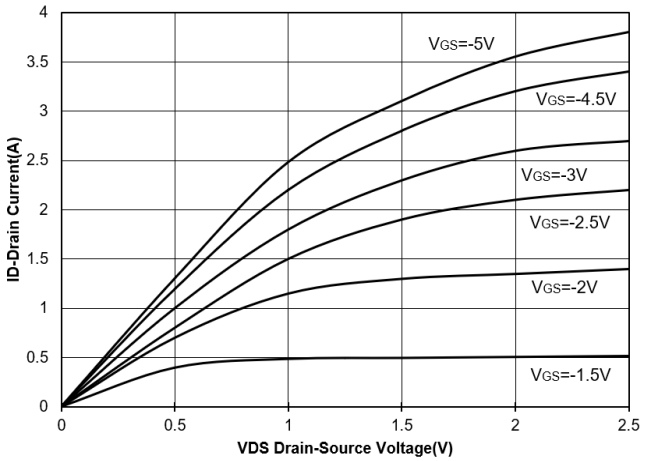


Figure 1. Output Characteristics

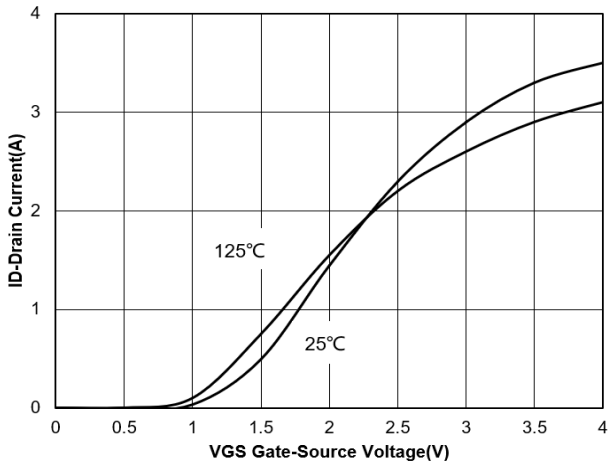


Figure 2. Transfer Characteristics

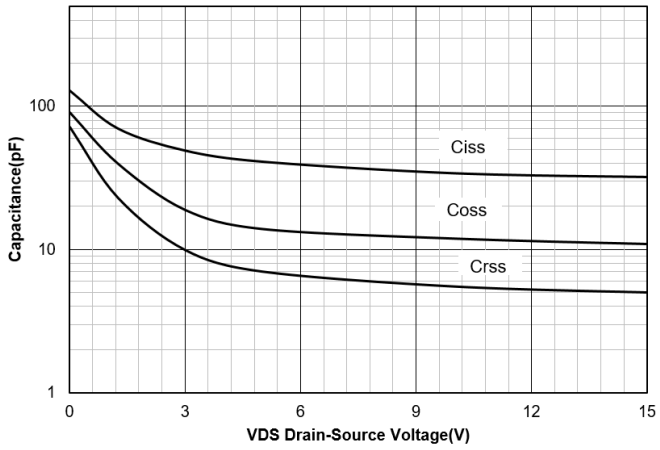


Figure 3. Capacitance Characteristics

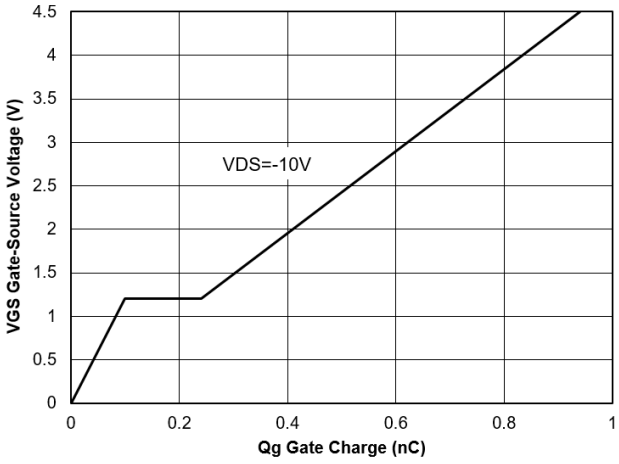


Figure 4. Gate Charge

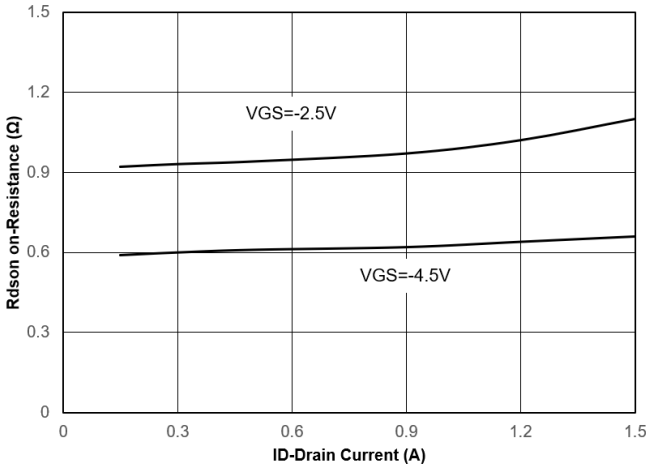


Figure 5. Drain-Source on Resistance

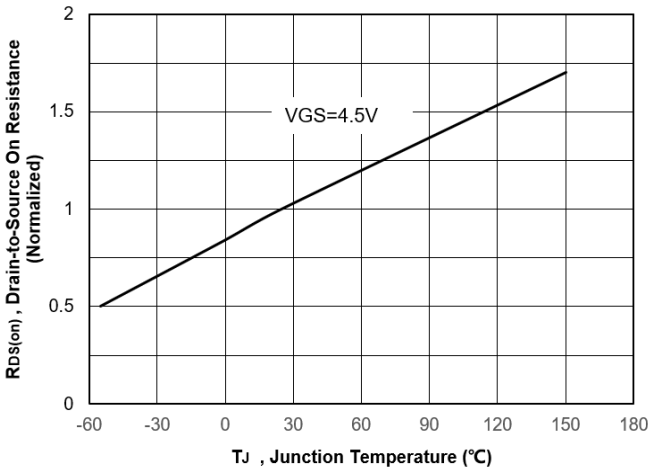


Figure 6. Normalized On-Resistance Vs. Temperature

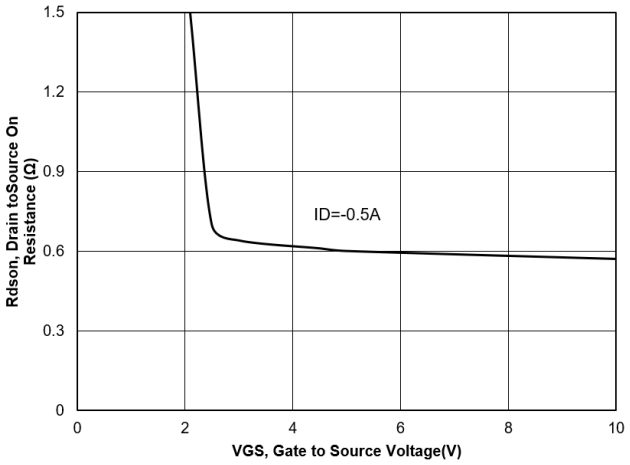


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

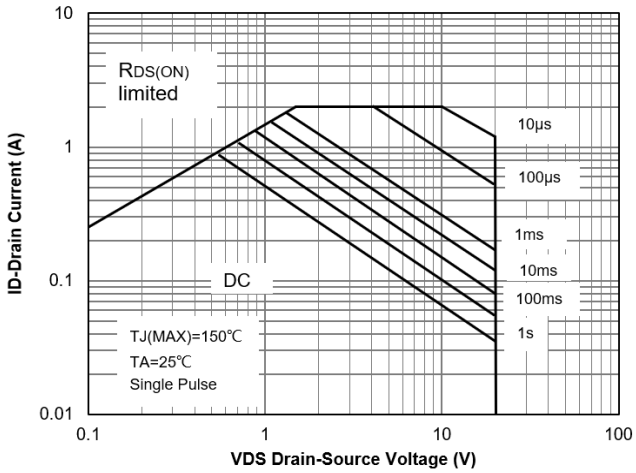


Figure 8. Safe Operation Area

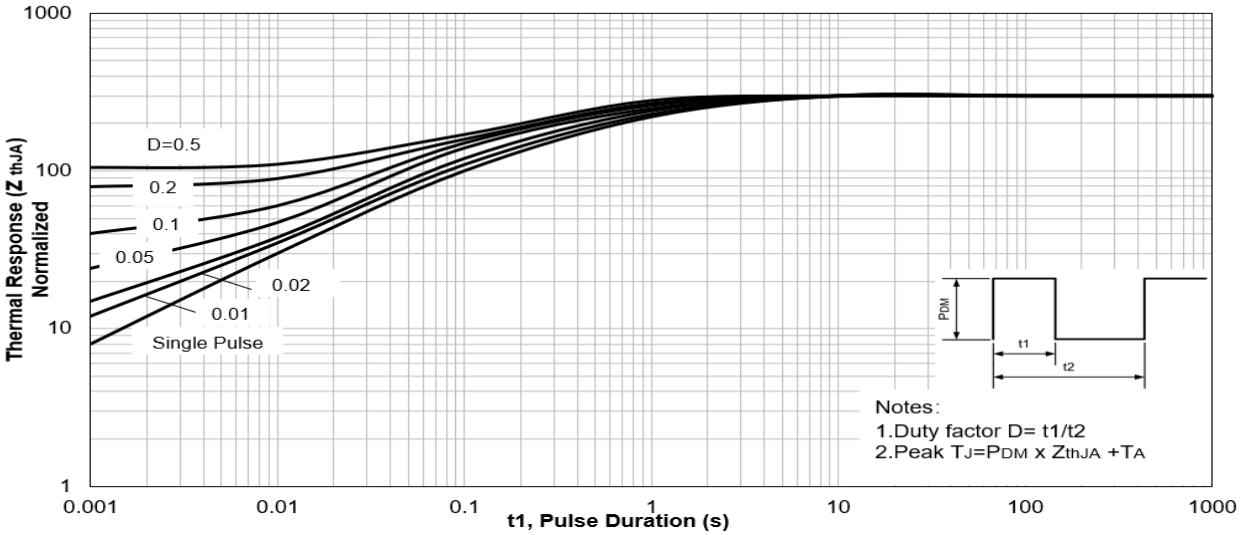


Figure 9. Maximum Effective Transient Thermal Impedance ,Junction-to-Ambient

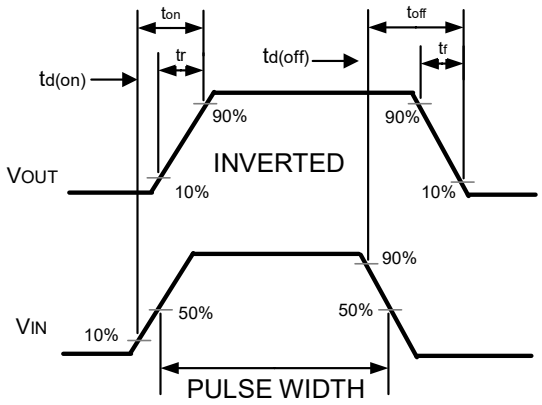
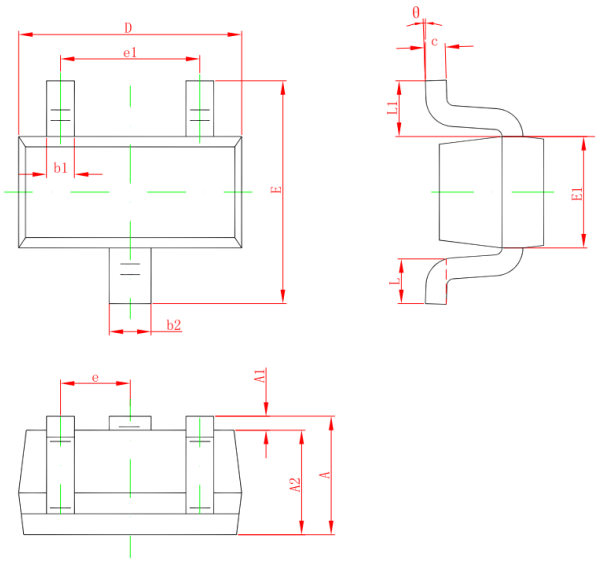


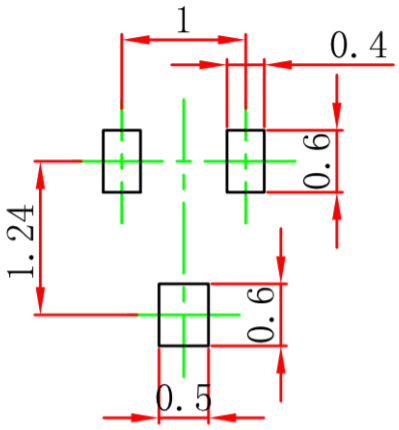
Figure 10. Switching wave

SOT-523 Package Outline Drawing



Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.900	0.028	0.035
A1	0.000	0.100	0.000	0.004
A2	0.700	0.800	0.028	0.031
b1	0.150	0.250	0.006	0.010
b2	0.250	0.350	0.010	0.014
c	0.100	0.200	0.004	0.008
D	1.500	1.700	0.059	0.067
E	1.450	1.750	0.057	0.069
E1	0.700	0.900	0.028	0.035
e	0.500 TYP.		0.020 TYP.	
e1	0.900	1.100	0.035	0.043
L	0.400 REF.		0.016 REF.	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

Suggested Land Pattern



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