

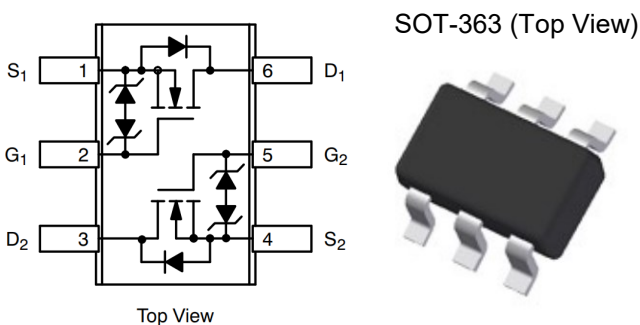
Description

CM2N72KCW is the N-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

Features

- V_{DS} : 60V
- I_D : 300mA
- $R_{DS(on)}$ (@ $V_{GS}=10V$): $< 2.5\Omega$
- $R_{DS(on)}$ (@ $V_{GS}=4.5V$): $< 3.0\Omega$
- High density cell design for extremely low $R_{DS(on)}$
- Excellent on-resistance and DC current capability

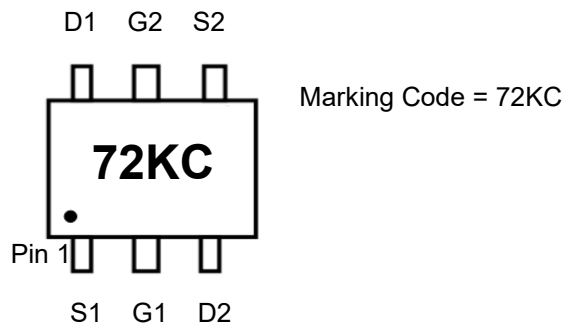
Equivalent Circuit and Pin Configuration



Applications

- Cellular Handsets and Accessories
- Personal Digital Assistants
- Portable Instrumentation
- Load switch

Marking Information



Ordering Information

Part Number	Packaging	Reel Size
CM2N72KCW	3000/Tape & Reel	7 inch

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Maximum	Unit	
Drain-source Voltage	V_{DS}	60	V	
Gate-source Voltage	V_{GS}	± 20	V	
Continuous Drain Current	I_D	$T_A=25^\circ\text{C}$	300	mA
		$T_A=70^\circ\text{C}$	240	mA
Pulsed Drain Current ⁽¹⁾	I_{DM}	1.5	A	
Total Power Dissipation @ $T_A=25^\circ\text{C}$ ⁽²⁾	P_D	300	mW	
Thermal Resistance Junction-to-Ambient ⁽²⁾	$R_{\theta JA}$	416	$^\circ\text{C/W}$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$	

Electrical Characteristics (T_J=25 °C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V, T _C =25°C			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±10	μA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0		2.5	V
Static Drain-Source on-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =300mA		1.9	2.5	Ω
		V _{GS} =4.5V, I _D =200mA		2.0	3.0	
Diode Forward Voltage	V _{SD}	I _S =300mA, V _{GS} =0V			1.2	V
Maximum Body-Diode Continuous Current	I _S				300	mA
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, f=1MHz		27		pF
Output Capacitance	C _{oss}			3.5		
Reverse Transfer Capacitance	C _{rss}			2.5		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =30V, I _D =0.3A		1.70		nC
Gate Source Charge	Q _{gs}			0.35		
Gate Drain Charge	Q _{gd}			0.55		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =30V, I _D =0.3A, R _{GEN} =6Ω		6.4		ns
Turn-off Delay Time	t _{D(off)}			9.8		

Noted: (1) Pulse Test: Pulse Width ≤ 300μs, Duty cycle ≤ 2%.

(2) Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. With 2oz Copper, t ≤ 10s

Typical Performance Characteristics

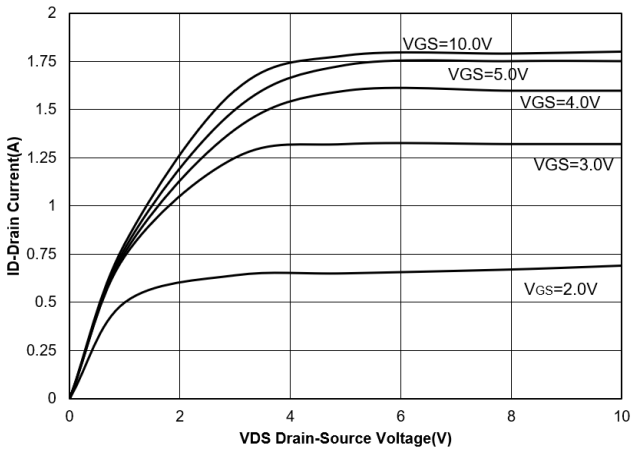


Figure 1. Output Characteristics

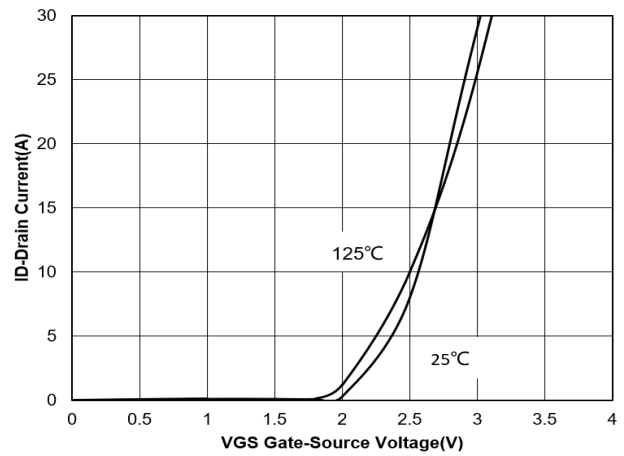


Figure 2. Transfer Characteristics

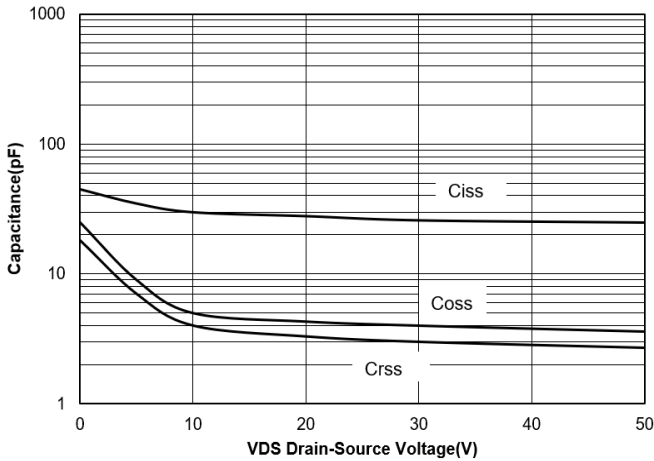


Figure 3. Capacitance Characteristics

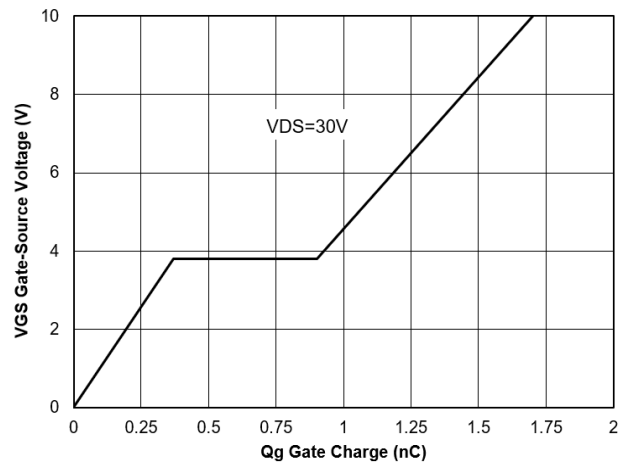


Figure 4. Gate Charge

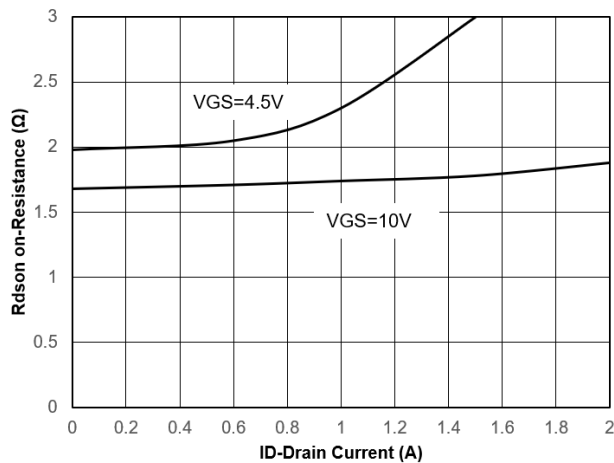


Figure 5. Drain-Source on Resistance

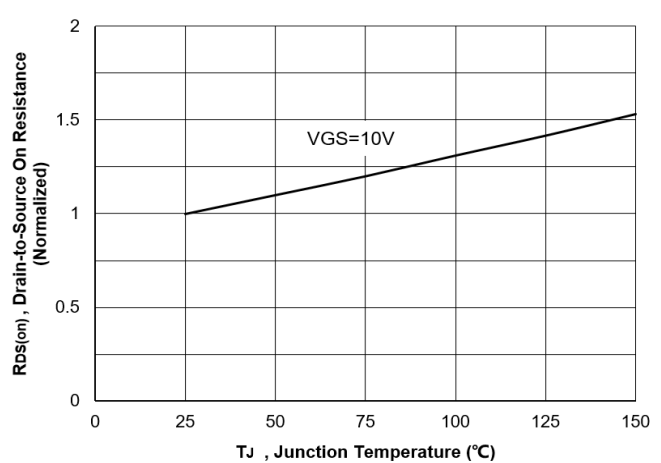


Figure 6. Normalized On-Resistance Vs. Temperature

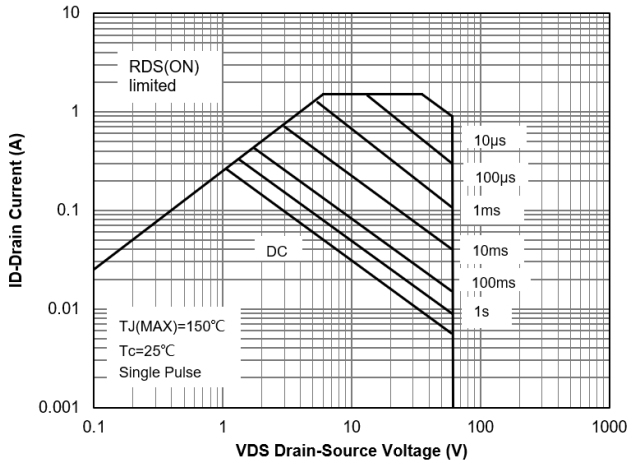


Figure 7. Safe Operation Area

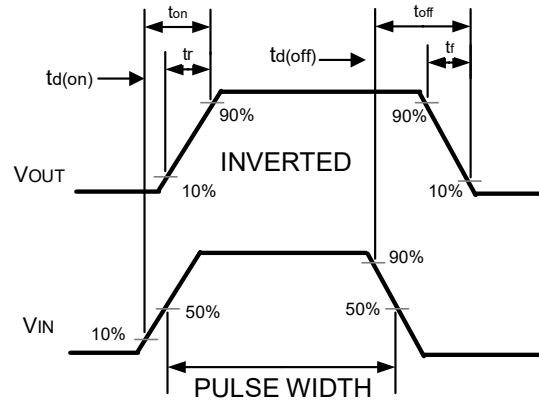


Figure 8. Switching wave

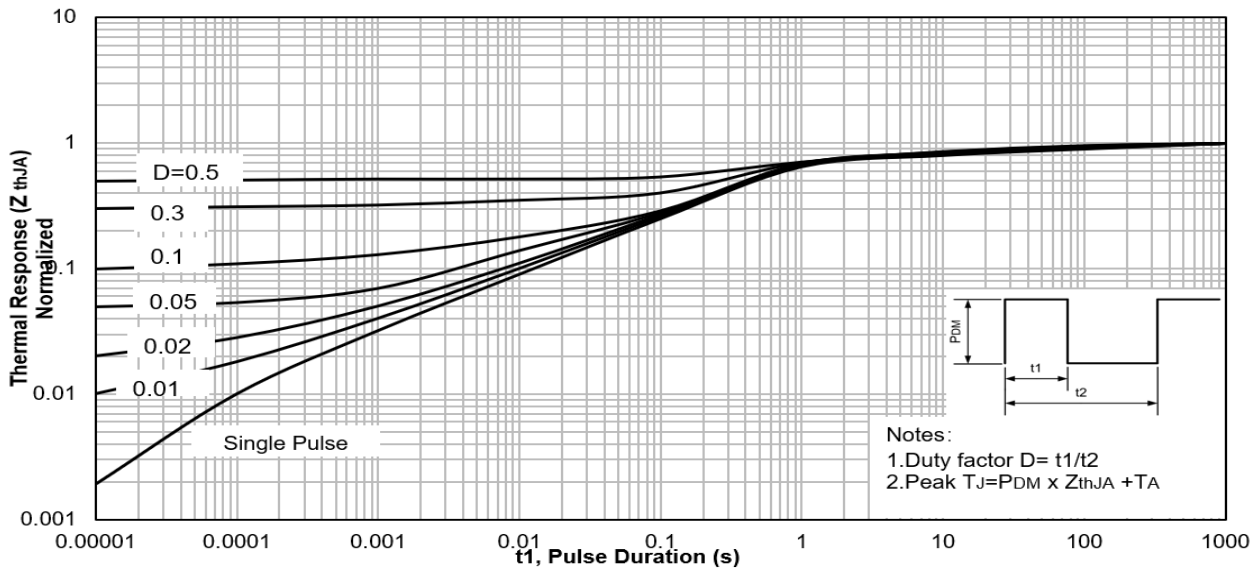
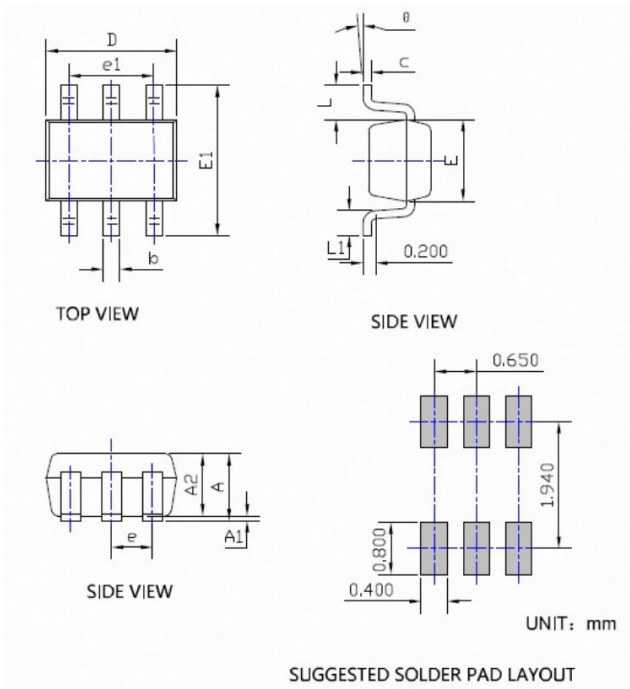


Figure 9. Maximum Effective Transient Thermal Impedance ,Junction-to-Ambient

SOT-363 Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	MOM	MAX
A	0.900	--	1.100	0.035	--	0.043
A1	0.000	--	0.100	0.000	--	0.004
A2	0.900	0.950	1.000	0.035	0.037	0.039
b	0.150	0.250	0.350	0.006	0.010	0.014
c	0.100	--	0.250	0.004	--	0.010
D	1.800	2.000	2.200	0.071	0.079	0.087
E	1.150	1.250	1.350	0.045	0.049	0.053
E1	2.150	2.300	2.450	0.085	0.091	0.096
e	0.650 TYP			0.026 TYP		
e1	1.200	1.300	1.400	0.047	0.051	0.055
L	0.525 REF			0.021 REF		
L1	0.260	0.360	0.460	0.010	0.014	0.018
θ	0°	--	8°	0°	--	8°

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