Description

CM26104 is the N-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

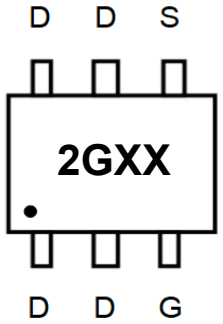
Features

- V_{DS}: 100V
- I_D: 3.1A
- $R_{DS_{ON}}$ ($@V_{GS}$=10V) : < 90mΩ
- $R_{DS_{ON}}$ ($@V_{GS}$=4.5V) : < 110mΩ
- High density cell design for extremely low $R_{DS_{ON}}$
- Excellent on-resistance and DC current capability

Applications

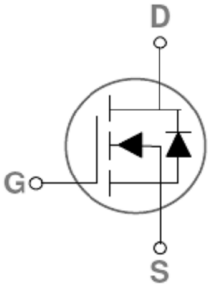
- Cellular Handsets and Accessories
- Personal Digital Assistants
- Portable Instrumentation
- Load switch

Marking Information

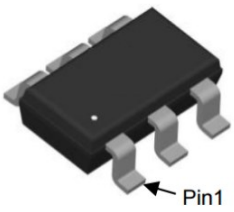


Device Code = 2G
Date Code=XX

Equivalent Circuit and Pin Configuration



SOT23-6 (Top View)



Ordering Information

Part Number	Packaging	Reel Size
CM26104	3000/Tape & Reel	7 inch

Absolute Maximum Ratings (T_A=25 ℃ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A=25°C	I_D	3.1	A
	T_A=70°C		2.5	A
Pulsed Drain Current[1]		I_{DM}	12.4	A
Total Power Dissipation @ T_A=25°C [2]		P_D	1.4	W
Thermal Resistance Junction-to-Ambient [2]		$R_{\theta JA}$	90	°C/W
Junction and Storage Temperature Range		T_J,T_{STG}	-55 to +150	°C

Electrical Characteristics (T_J=25 ℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V,T_C=25°C			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.2		3.0	V
Static Drain-Source on-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=1A		68	90	mΩ
		V_{GS}=4.5V,I_D=0.5A		80	110	
Diode Forward Voltage	V_{SD}	I_S=3.1A,V_{GS}=0V		0.8	1.2	V
Maximum Body-Diode Continuous Current	I_S				3.1	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V,f=1MHz		454		pF
Output Capacitance	C_{oss}			152		
Reverse Transfer Capacitance	C_{rss}			14.5		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=2A		7.6		nC
Gate Source Charge	Q_{gs}			0.9		
Gate Drain Charge	Q_{gd}			1.8		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=20V, I_D=1A,R_{GEN}=3.3Ω		5.4		ns
Turn-on Rise Time	t_r			2.1		
Turn-off Delay Time	$t_{D(off)}$			14.2		
Turn-off Fall Time	t_f			6.2		

Noted: (1) Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

(2) Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. With 2oz Copper ,t≤10s

Typical Performance Characteristics

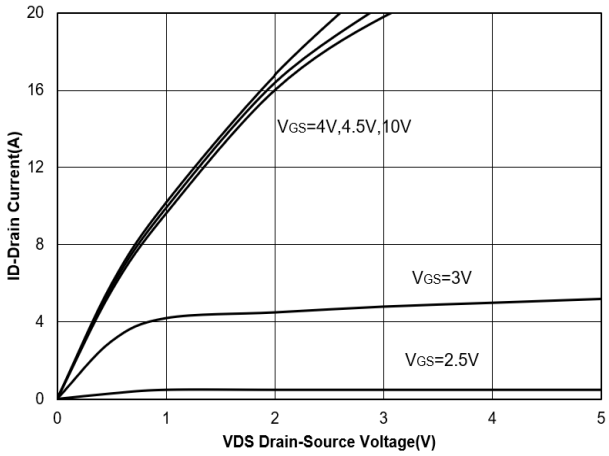


Figure 1. Output Characteristics

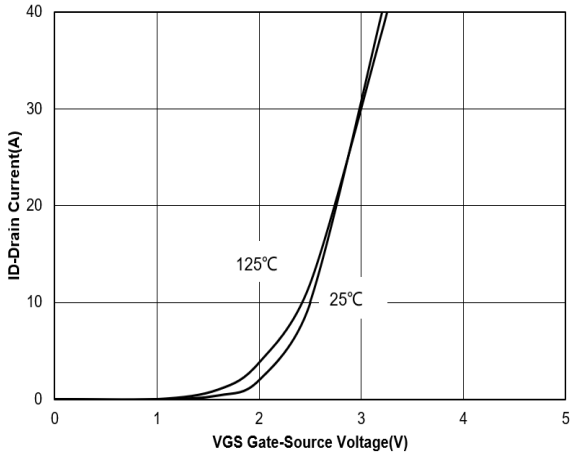


Figure 2. Transfer Characteristics

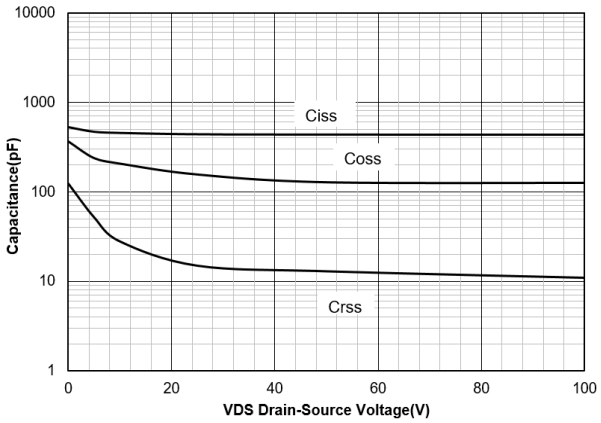


Figure 3. Capacitance Characteristics

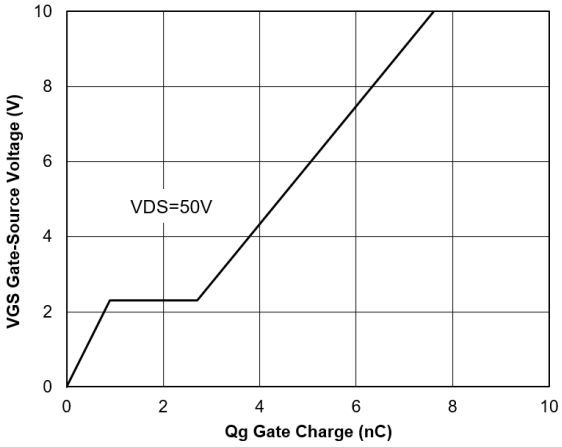


Figure 4. Gate Charge

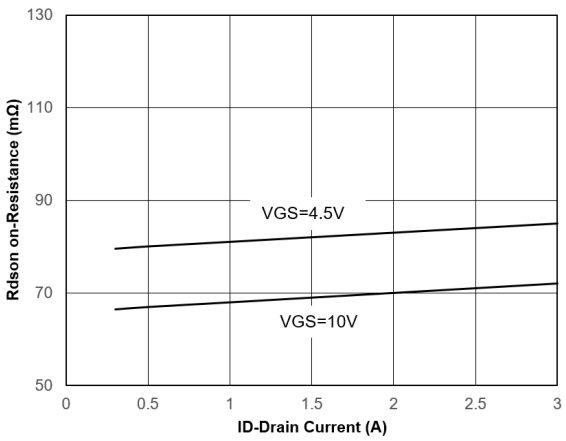


Figure 5. Drain-Source on Resistance

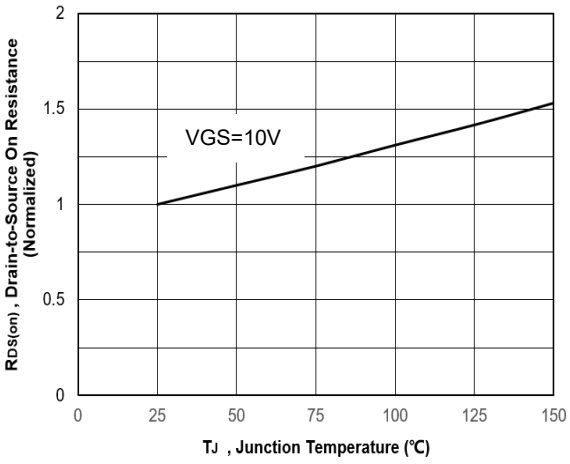


Figure 6. Normalized On-Resistance Vs. Temperature

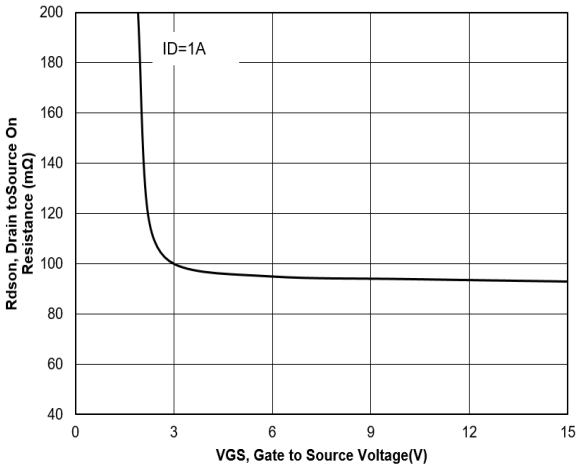


Figure 7. On-Resistance VS Gate-Source Voltage

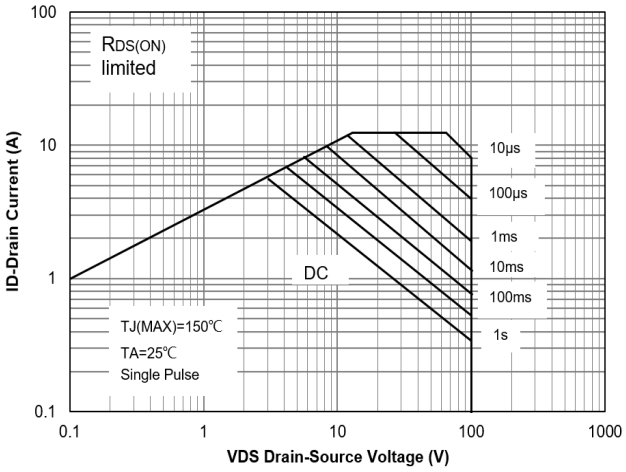


Figure 8. Safe Operation Area

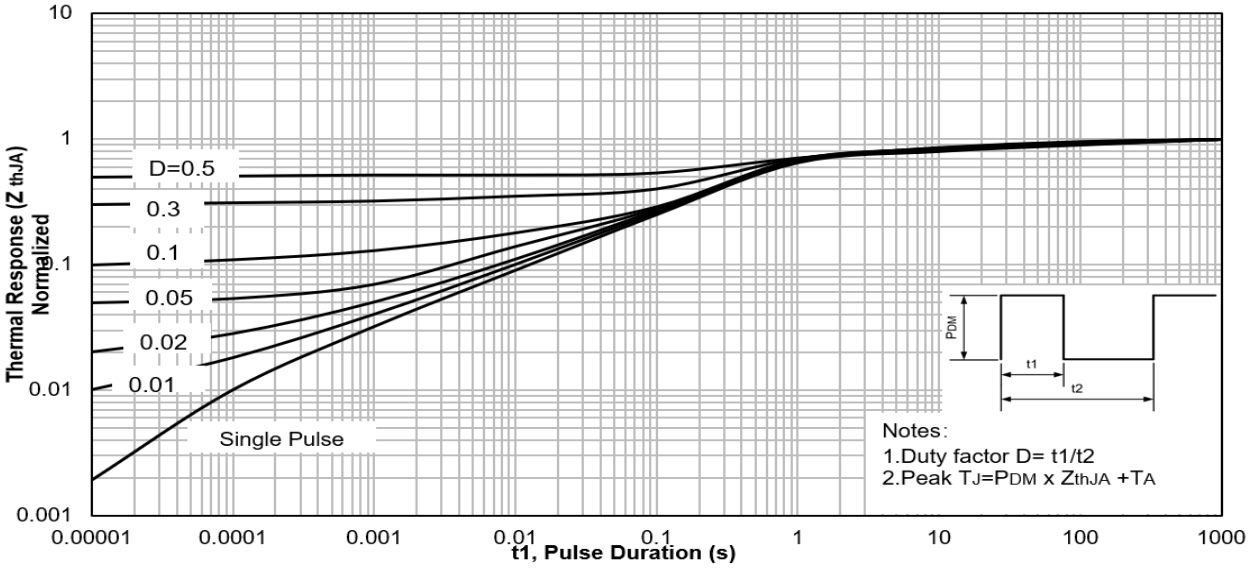


Figure 9. Maximum Effective Transient Thermal Impedance ,Junction-to-Ambient

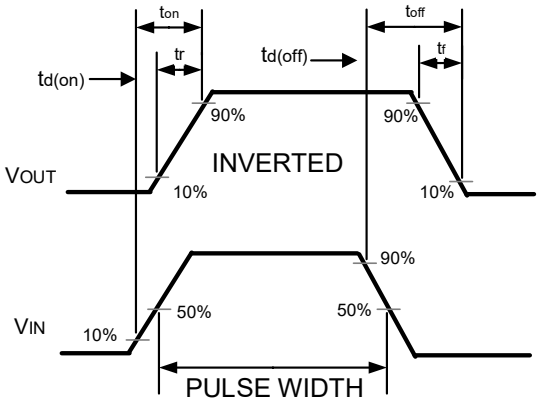
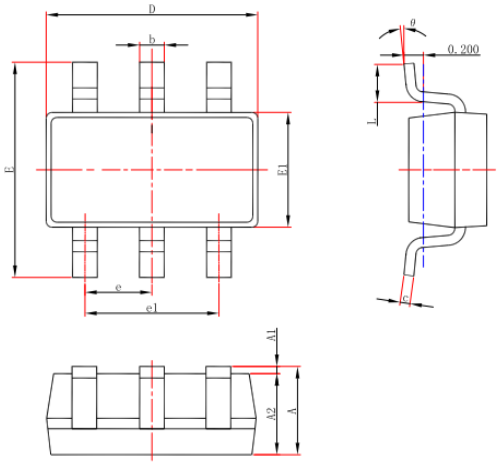


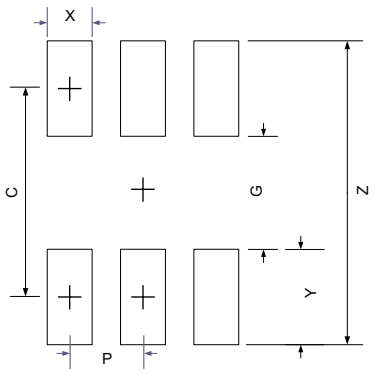
Figure 10. Switching wave

SOT23-6 Package Outline Drawing



SYM	DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.140	0.000	0.006
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	3.000	0.104	0.118
e	0.950 BSC		0.037 BSC	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
C	2.50	0.098
G	1.40	0.055
P	0.95	0.037
X	0.60	0.024
Y	1.10	0.043
Z	3.60	0.141

Contact Information

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