Description

CM2321LT is the P-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

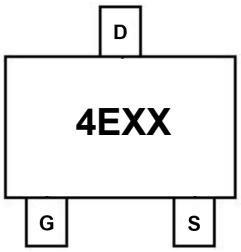
Applications

- Cellular Handsets and Accessories
- Personal Digital Assistants
- Portable Instrumentation
- Load switch

Features

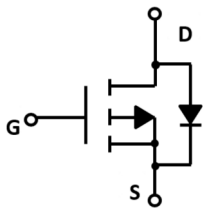
- V_{DS}: -20V
- I_D: -6.5A
- $R_{DS_{ON}}$ ($@V_{GS}$=-10V) : < 22mΩ
- $R_{DS_{ON}}$ ($@V_{GS}$=-4.5V) : < 30mΩ
- High density cell design for extremely low $R_{DS_{ON}}$
- Excellent on-resistance and DC current capability

Marking Information

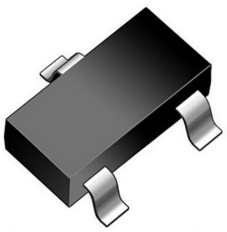


Marking Code = 4E
Date Code = XX

Equivalent Circuit and Pin Configuration



SOT-23-3L



Ordering Information

Part Number	Packaging	Reel Size
CM2321LT	3000/Tape & Reel	7 inch

Absolute Maximum Ratings (T_A=25 ℃ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	-20	V
Gate-source Voltage		V_{GS}	±10	V
Continuous Drain Current	T_A=25°C	I_D	-6.5	A
	T_A=70°C		-5.0	A
Pulsed Drain Current[1]		I_{DM}	-26	A
Total Power Dissipation @ T_A=25°C [2]		P_D	1.4	W
Thermal Resistance Junction-to-Ambient [2]		$R_{\theta JA}$	90	°C/W
Junction and Storage Temperature Range		T_J,T_{STG}	-55 to +150	°C

Electrical Characteristics (T_J=25 ℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=-250μA	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V,V_{GS}=0V,T_C=25°C			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±10V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-0.5		-1.1	V
Static Drain-Source on-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-6.5A		17	22	mΩ
		V_{GS}=-4.5V,I_D=-5A		22	30	
Diode Forward Voltage	V_{SD}	I_S=-6.5A,V_{GS}=0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I_S				-6.5	A
Dynamic Parameters						
Input Capacitance	Ciss	V_{DS}=-10V,V_{GS}=0V,f=1MHz		1720		pF
Output Capacitance	Coss			200		
Reverse Transfer Capacitance	Crss			170		
Switching Parameters						
Total Gate Charge	Qg	V_{GS}=-4.5V,V_{DS}=-10V,I_D=-3A		28		nC
Gate Source Charge	Qgs			3.4		
Gate Drain Charge	Qgd			3.7		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-4.5V,V_{DD}=-10V, I_D=-6A,R_{GEN}=2.5Ω		13.2		ns
Turn-on Rise Time	tr			8.6		
Turn-off Delay Time	$t_{D(off)}$			143		
Turn-off Fall Time	tf			47		

Noted: (1) Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

(2) Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. With 2oz Copper ,t≤10s

Typical Performance Characteristics

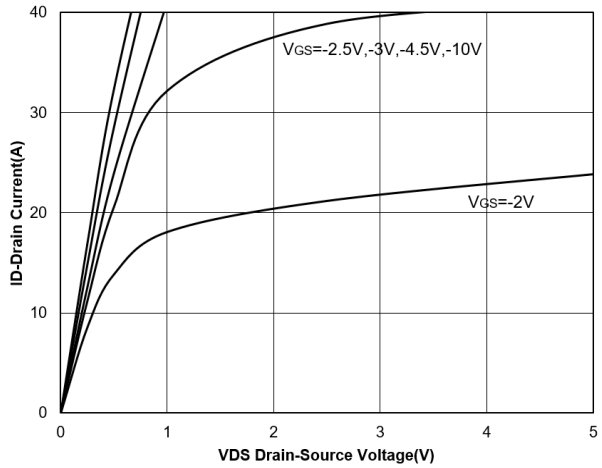


Figure 1. Output Characteristics

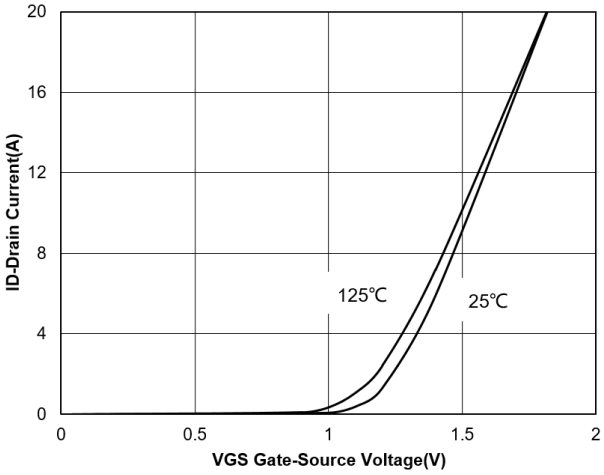


Figure 2. Transfer Characteristics

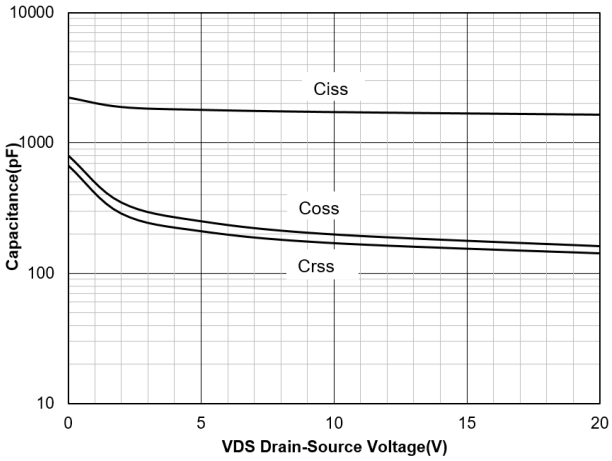


Figure 3. Capacitance Characteristics

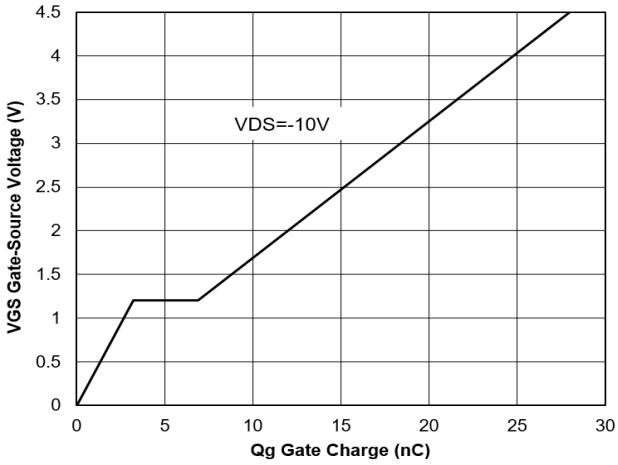


Figure 4. Gate Charge

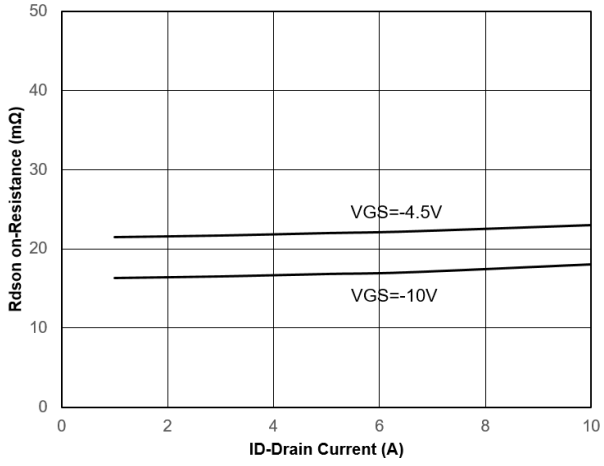


Figure 5. Drain-Source on Resistance

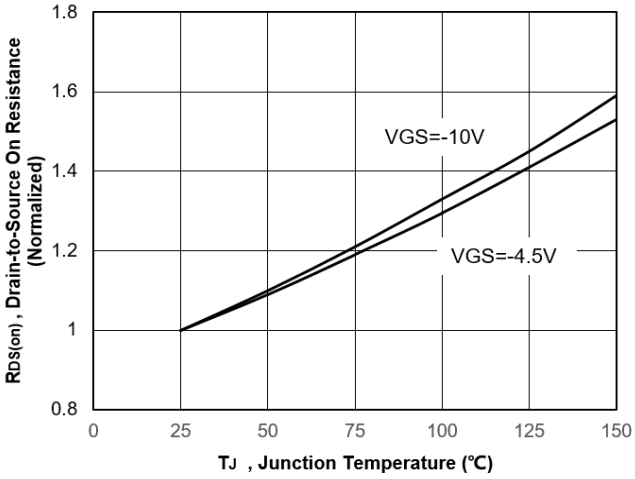


Figure 6. Normalized On-Resistance Vs. Temperature

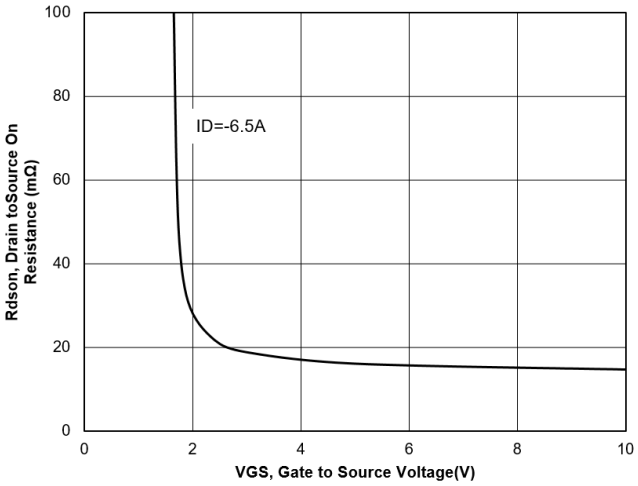


Figure 7. Typical Drain to Source ON Resistance

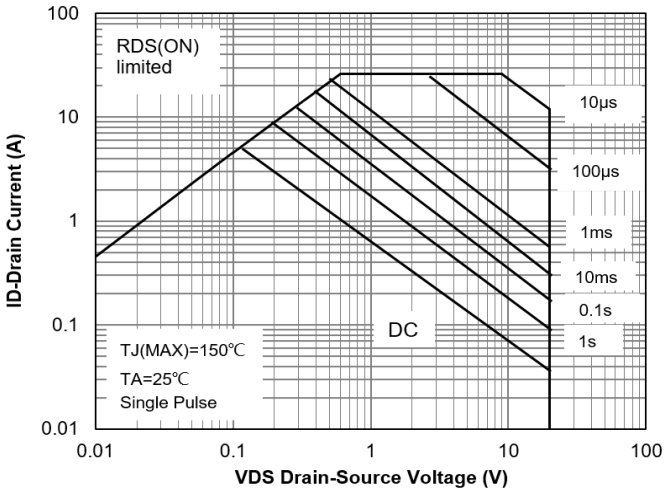


Figure 8. Safe Operation Area

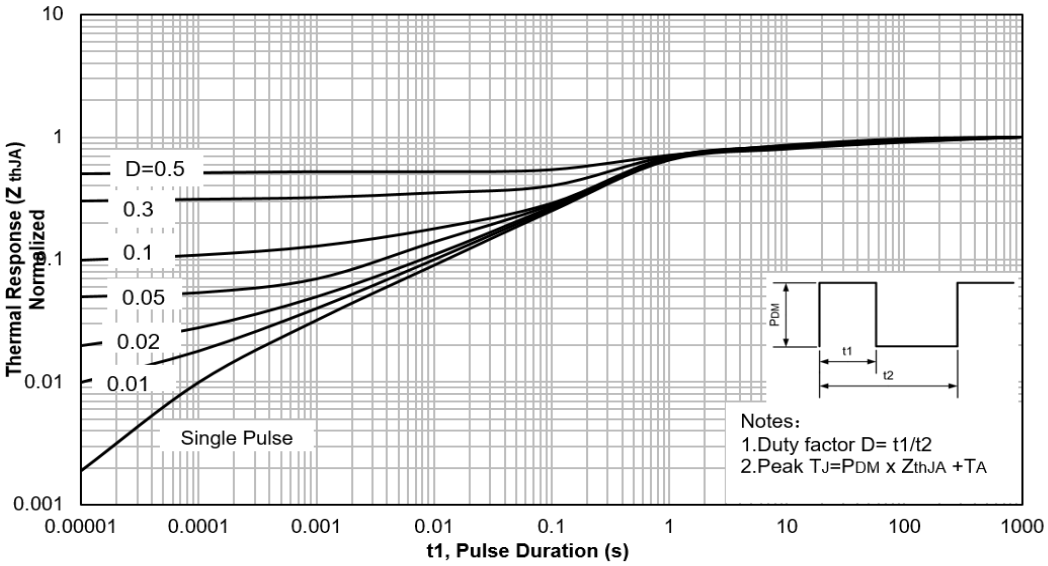


Figure 9. Maximum Effective Transient Thermal Impedance ,Junction-to-Ambient

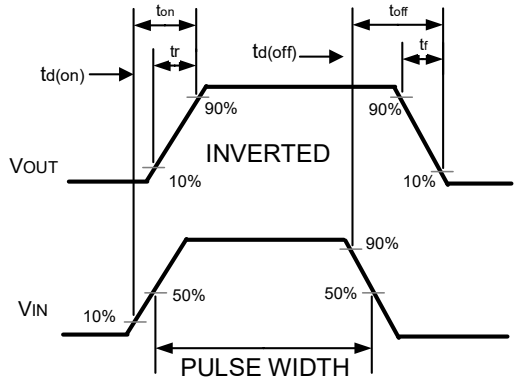
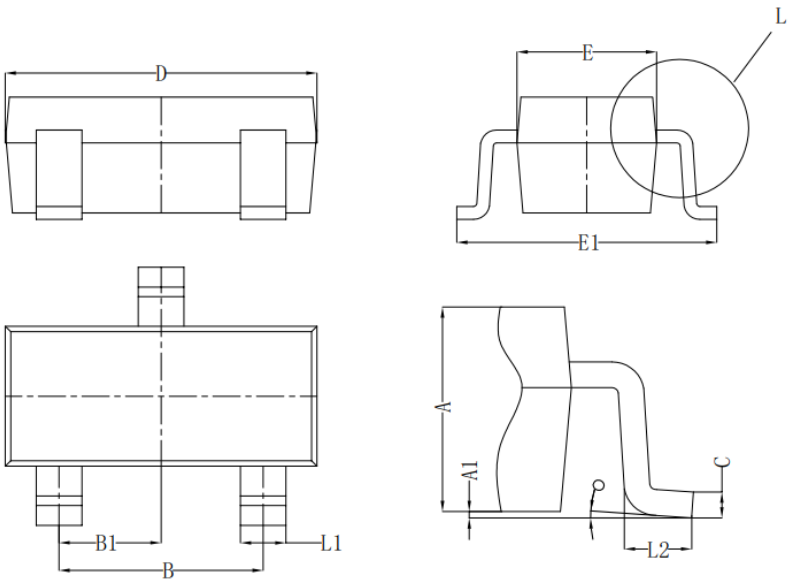


Figure 10. Switching wave

SOT-23-3L Package Outline Drawing



SYM	Dim in mm		
	MIN	NOM	MAX
A	1.050	1.100	1.150
A1	0.000	0.050	0.100
L1	0.300	0.400	0.500
C	0.100	0.150	0.200
D	2.820	2.920	3.020
E	1.500	1.600	1.700
E1	2.650	2.800	2.950
B	1.800	1.900	2.000
B1	0.950 TYP		
L2	0.300	0.450	0.600
O	0°	4°	8°