Description

CM2305N is the P-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

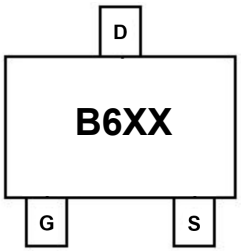
Features

- V_{DS}: -20V
- I_D: -4A
- $R_{DS_{ON}}$ (@V_{GS}=-4.5V) : < 55mΩ
- $R_{DS_{ON}}$ (@V_{GS}=-2.5V) : < 75mΩ
- High density cell design for extremely low $R_{DS_{ON}}$
- Excellent on-resistance and DC current capability

Applications

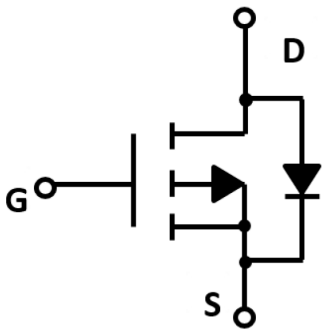
- Cellular Handsets and Accessories
- Personal Digital Assistants
- Portable Instrumentation
- Load switch

Marking Information

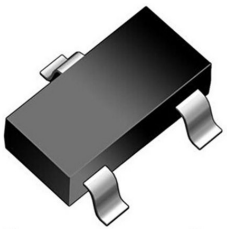


Device Code = B6
Date Code = XX

Equivalent Circuit and Pin Configuration



SOT-23 (Top View)



Ordering Information

Part Number	Packaging	Reel Size
CM2305N	3000/Tape & Reel	7 inch

Absolute Maximum Ratings (T_A=25 ℃ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	-20	V
Gate-source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A=25°C	I_D	-4	A
	T_A=70°C		-3	A
Pulsed Drain Current(1)		I_{DM}	-16	A
Total Power Dissipation @ T_A=25°C (2)		P_D	1.3	W
Thermal Resistance Junction-to-Ambient (2)		$R_{\theta JA}$	100	°C/W
Junction and Storage Temperature Range		T_J,T_{STG}	-55 to +150	°C

Electrical Characteristics (T_J=25 ℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=-250μA	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V,V_{GS}=0V,T_C=25°C			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±12V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-0.4		-1.0	V
Static Drain-Source on-Resistance	$R_{DS(on)}$	V_{GS}=-4.5V,I_D=-4.1A		45	55	mΩ
		V_{GS}=-2.5V,I_D=-3A		55	75	
Diode Forward Voltage	V_{SD}	I_S=-4A,V_{GS}=0V		-0.9	-1.2	V
Maximum Body-Diode Continuous Current	I_S				-4	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-10V,V_{GS}=0V,f=1MHz		850		pF
Output Capacitance	C_{oss}			120		
Reverse Transfer Capacitance	C_{rss}			116		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-4.5V,V_{DS}=-10V,I_D=-4A		16.3		nC
Gate Source Charge	Q_{gs}			1.6		
Gate Drain Charge	Q_{gd}			2.5		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-4.5V,V_{DD}=-10V, R_L=2.5Ω,R_{GEN}=2.5Ω		19		ns
Turn-on Rise Time	t_r			15.2		
Turn-off Delay Time	$t_{D(off)}$			52		
Turn-off Fall Time	t_f			20.1		

Noted: (1) Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

(2) Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. With 2oz Copper ,t≤10s

Typical Performance Characteristics

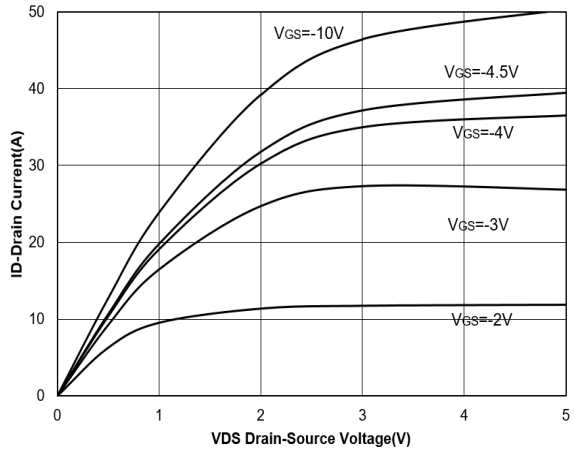


Figure 1. Output Characteristics

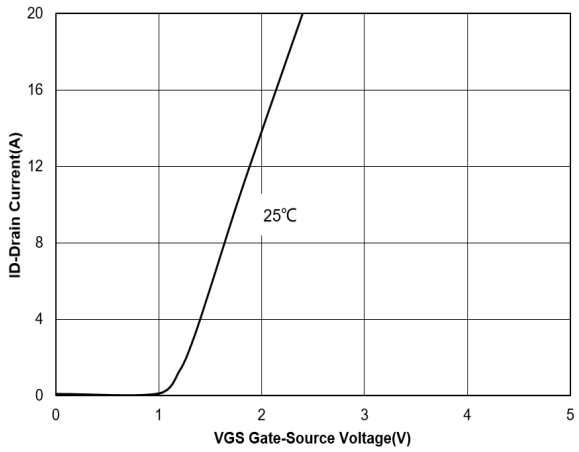


Figure 2. Transfer Characteristics

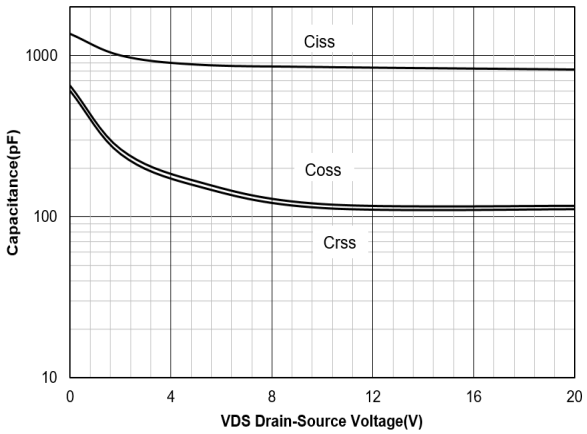


Figure 3. Capacitance Characteristics

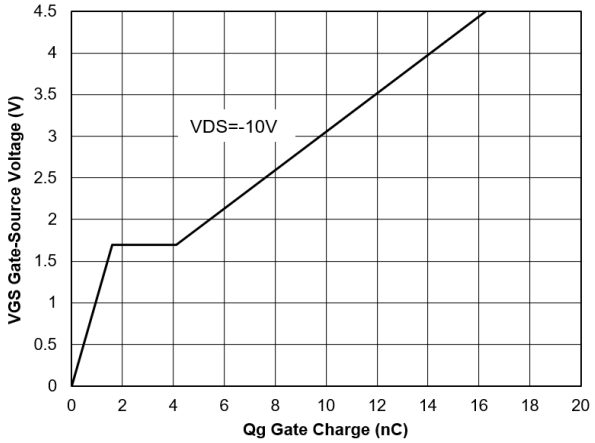


Figure 4. Gate Charge

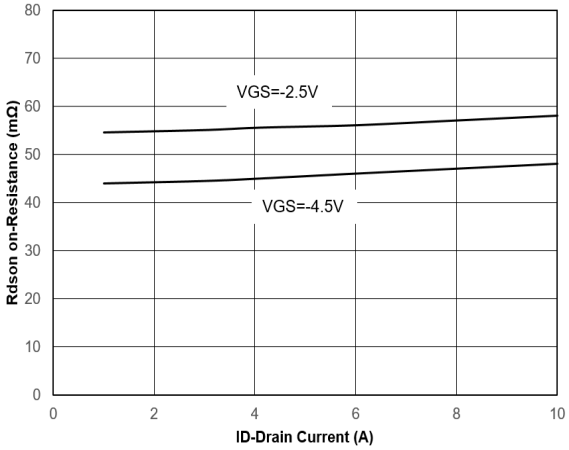


Figure 5. Drain-Source on Resistance

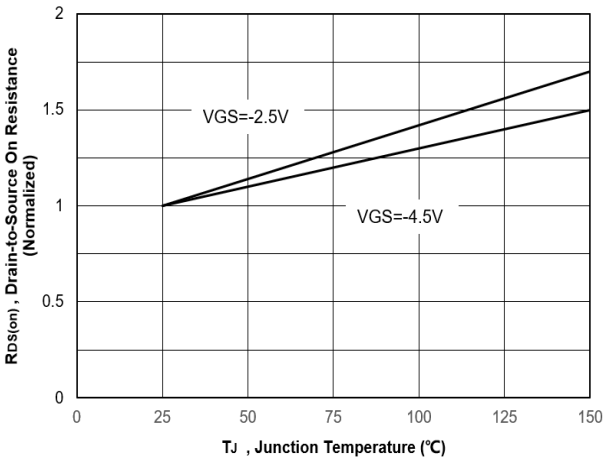


Figure 6. Normalized On-Resistance Vs. Temperature

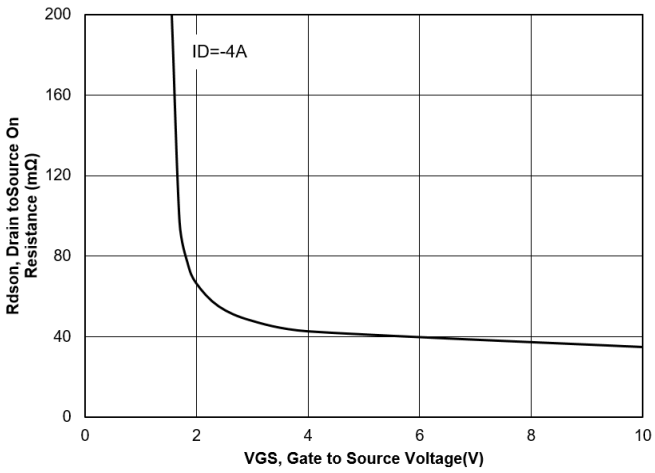


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

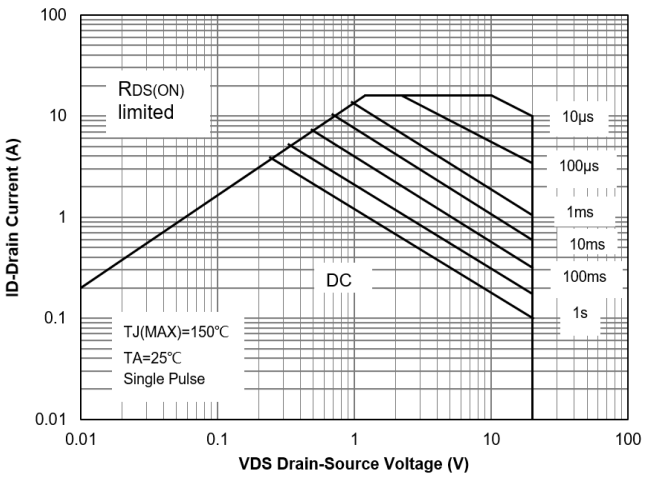


Figure 8. Safe Operation Area

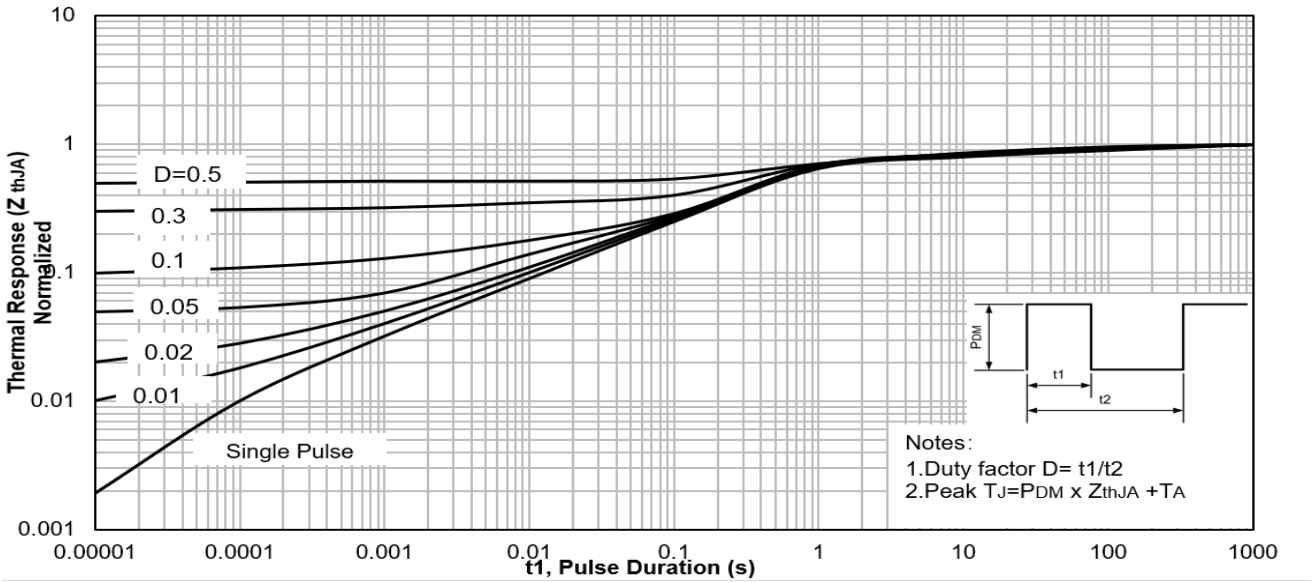


Figure 9. Maximum Effective Transient Thermal Impedance ,Junction-to-Ambient

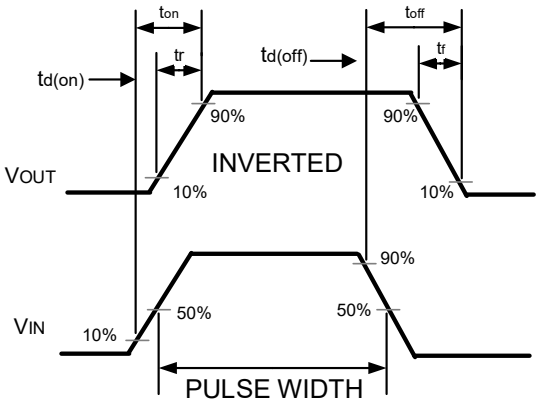
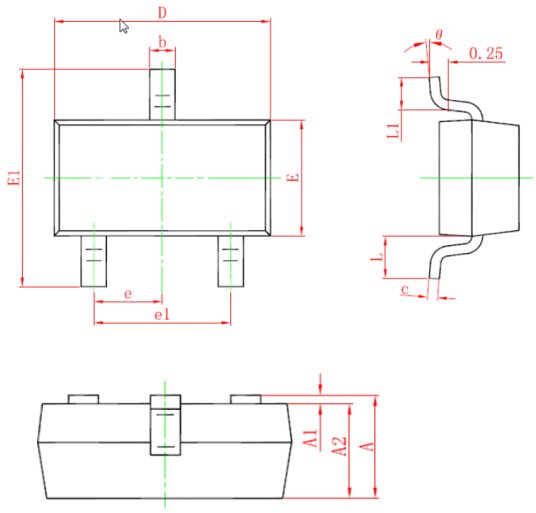


Figure 10. Switching wave

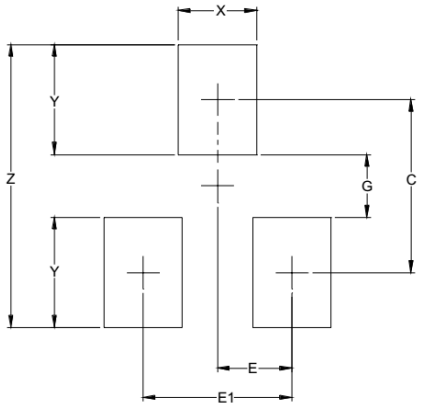
SOT-23 Package Outline Drawing



(Unit : mm)

SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	- -	1.15	0.035	- -	0.045
A1	0.00	- -	0.10	0.000	- -	0.004
A2	0.90	- -	1.05	0.035	- -	0.041
b	0.30	- -	0.50	0.012	- -	0.020
c	0.08	- -	0.15	0.003	- -	0.006
D	2.80	- -	3.00	0.110	- -	0.118
E	1.20	- -	1.40	0.047	- -	0.055
E1	2.25	- -	2.55	0.089		0.100
e	0.95TYP			0.037TYP		
e1	1.80	- -	2.00	0.071	- -	0.079
L	0.55REF			0.022REF		
L1	0.30	- -	0.50	0.012	- -	0.020
Θ	0°	- -	8°	0°	- -	8°

Suggested Land Pattern



SYM	DIMENSIONS	
	INCHES	MILLIMETERS
C	0.087	2.20
E	0.037	0.95
E1	0.075	1.90
G	0.031	0.80
X	0.039	1.00
Y	0.055	1.40
Z	0.141	3.60