

Description

The CM180N10GP is the N-Channel enhancement mode power field effect transistors with high cell density, high voltage planar technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance, .

Features

- VDS: 100V
- ID (@VGS=10V): 203A
- RDS_{ON} (@VGS=10V) : < 3.6mΩ
- High density cell design for extremely low RDS_{ON}
- Excellent on-resistance and DC current capability

Applications

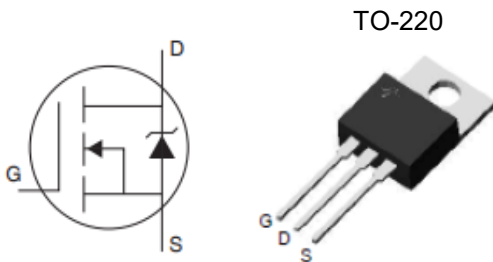
- AC/DC load switch
- SMPS
- LED power

Marking Information



180N10GP=Marking Code
 XXXX = Date Code

Equivalent Circuit and Pin Configuration



Ordering Information

P/N	Package Type	Packaging	Remark
CM180N10GP	TO-220	Tube	ROHS

Absolute Maximum Ratings (T_c=25 °C unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	V _{DS}	100	V
Gate-source Voltage	V _{GS}	±20	V
Continuous Drain Current ⁽¹⁾	I _D	T _c =25°C (Silicon Limit)	203
		T _c =25°C (Package Limit)	120
		T _c =100°C (Silicon Limit)	124
Pulsed Drain Current ⁽²⁾	I _{DM}	480	A
Total Power Dissipation ⁽³⁾	PD @ T _c =25°C	311	W
	Derating Factor above 25°C	2.5	W/°C
Thermal Resistance Junction-to-Case ⁽³⁾	R _{θJC}	0.402	°C/W
Junction and Storage Temperature Range	T _J ,T _{STG}	-55 to +150	°C

Electrical Characteristics (T_c=25 °C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BVDSS	V _{GS} =0V, I _D =250μA	100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V, T _C =25°C			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Static Drain-Source on-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =30A		2.8	3.6	mΩ
Diode Forward Voltage	V _{SD}	I _S =30A, V _{GS} =0V		0.8	1.2	V
Maximum Body-Diode Continuous Current	I _S				120	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHz		7750		pF
Output Capacitance	C _{oss}			1620		
Reverse Transfer Capacitance	C _{rss}			26		
Switching Parameters						
Total Gate Charge	Q _g	V _{DS} =50V, I _D =20A, V _{GS} =10V		135		nC
Gate Source Charge	Q _{gs}			28		
Gate Drain Charge	Q _{gd}			44		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _D =10A, R _{GEN} =2.2Ω		54		ns
Turn-on Rise Time	t _r			43.4		
Turn-off Delay Time	t _{D(off)}			186		
Turn-off Fall Time	t _f			86.6		

Noted: (1) Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%

(2) Pulse width limited by maximum junction temperature

(3) Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. With 2oz Copper, t ≤ 10s

Typical Performance Characteristics

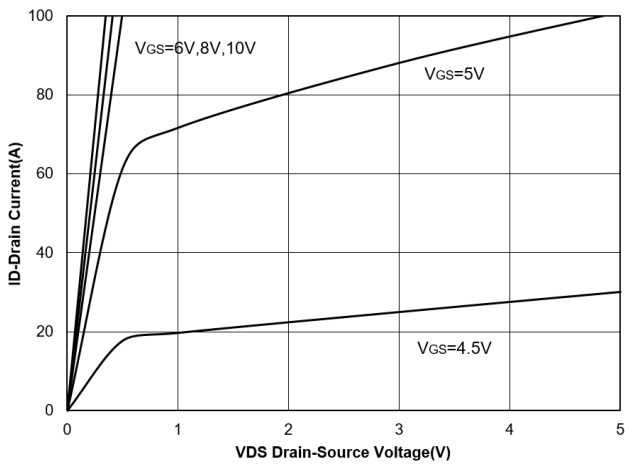


Figure 1. Output Characteristics

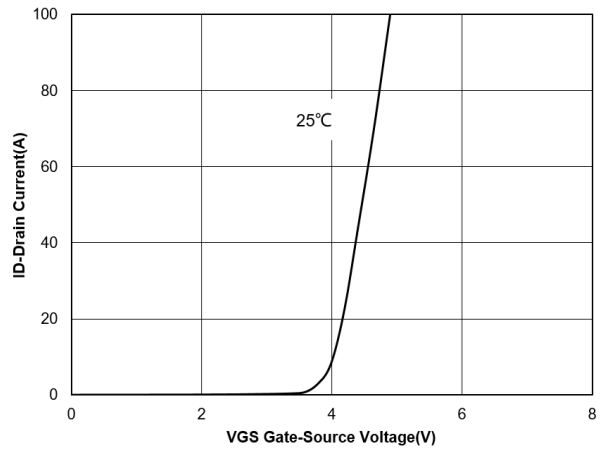


Figure 2. Transfer Characteristics

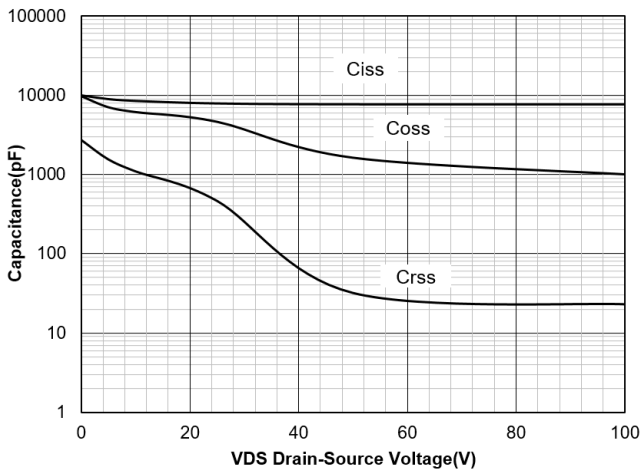


Figure 3. Capacitance Characteristics

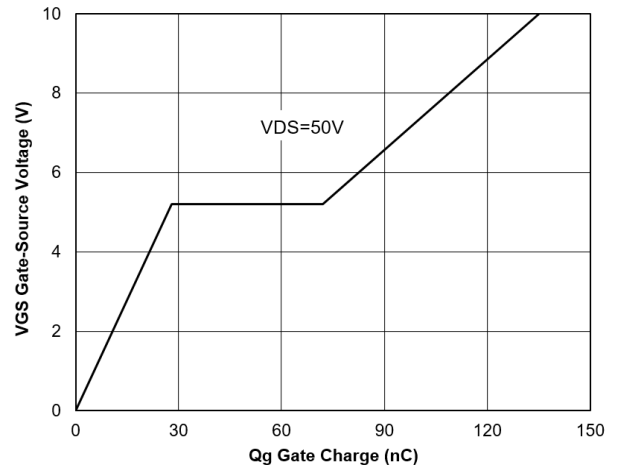


Figure 4. Gate Charge

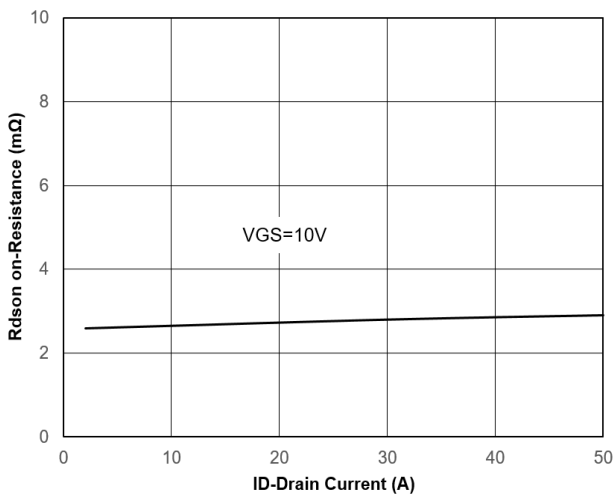


Figure 5. Drain-Source on Resistance

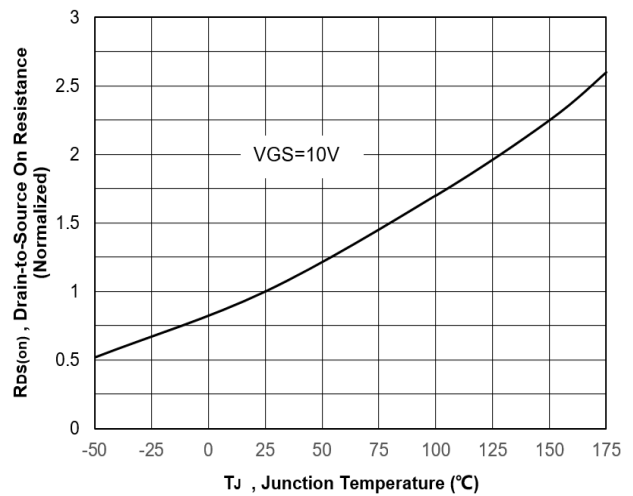


Figure 6. Normalized On-Resistance Vs. Temperature

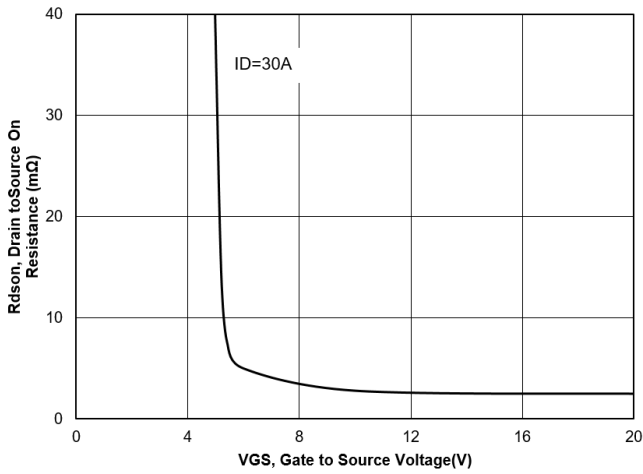


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

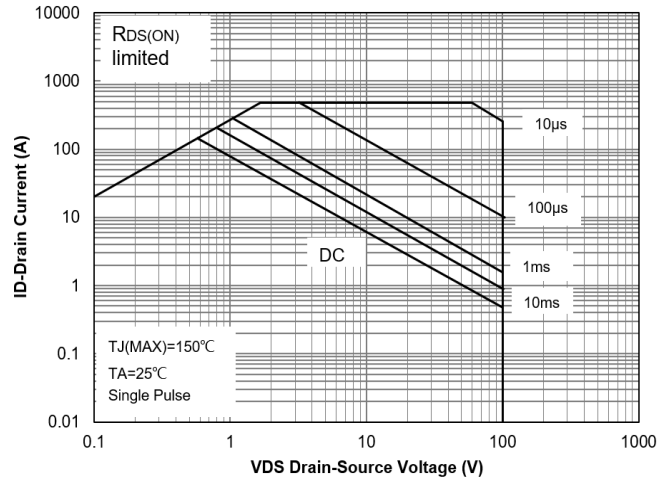


Figure 8. Safe Operation Area

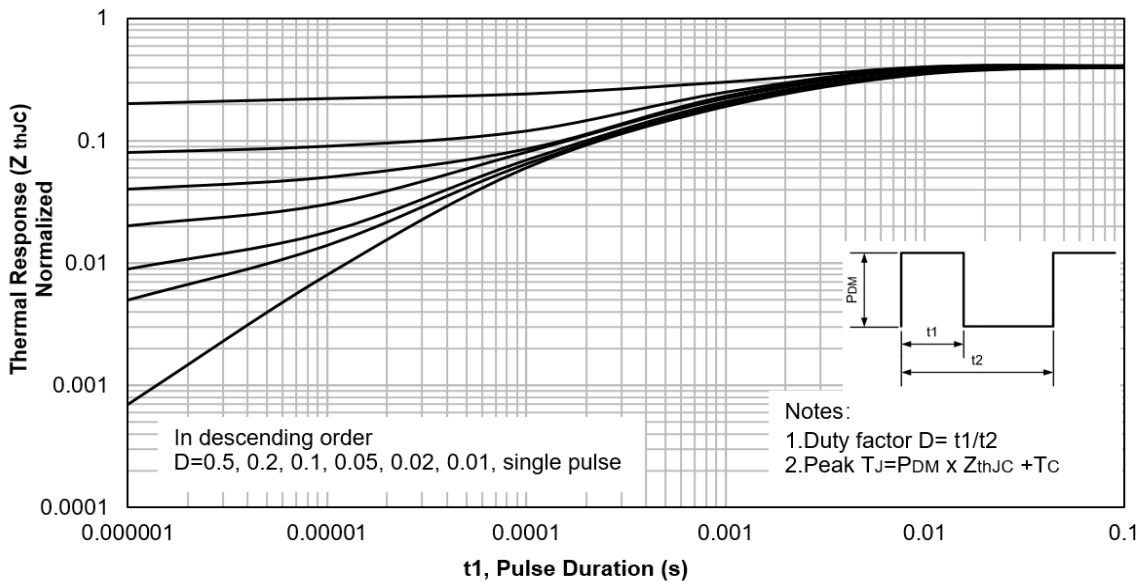


Figure 9. Maximum Effective Transient Thermal Impedance, Junction-to-Case

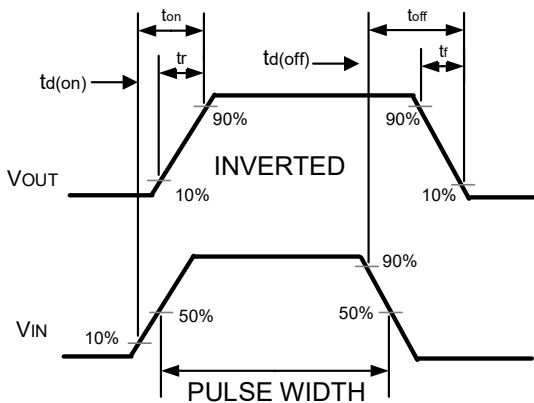
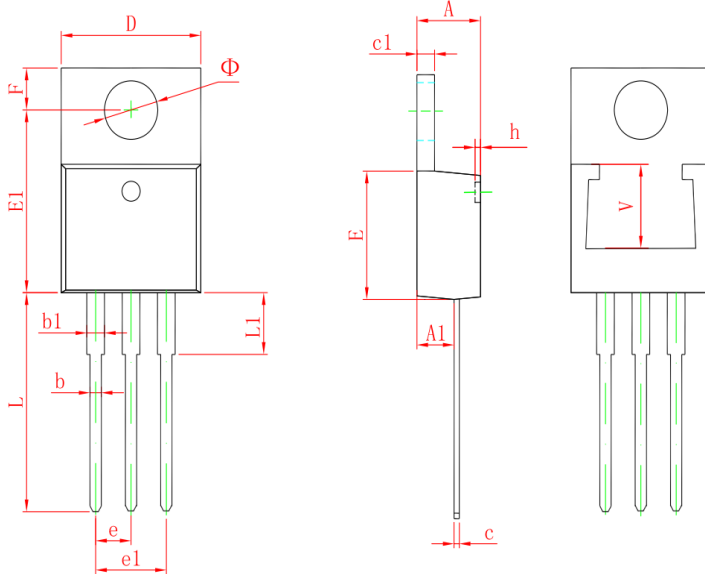


Figure 10. Switching wave

TO-220 Package Outline Drawing


Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.470	4.670	0.176	0.184
A1	2.520	2.820	0.099	0.111
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
E1	12.060	12.460	0.475	0.491
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.590	2.890	0.102	0.114
h	0.000	0.300	0.000	0.012
L	13.400	13.800	0.528	0.543
L1	3.560	3.960	0.140	0.156
Φ	3.735	3.935	0.147	0.155
V	5.600 REF.		0.220 REF.	