Description

The CM170N10GP is the N-Channel enhancement mode power field effect transistors with high cell density, high voltage planar technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

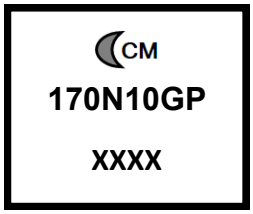
Applications

- AC/DC load switch
- SMPS
- Notebooks and Handhelds adapter
- UPS Power

Features

- V_{DS}: 100V
- I_D (@V_{GS}=10V): 211A
- RDS_{ON} (@V_{GS}=10V) : < 3.9mΩ
- High density cell design for extremely low RDS_{ON}
- Excellent on-resistance and DC current capability

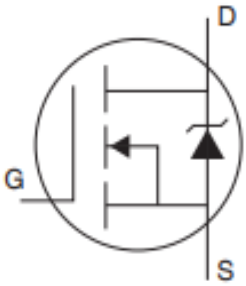
Marking Information



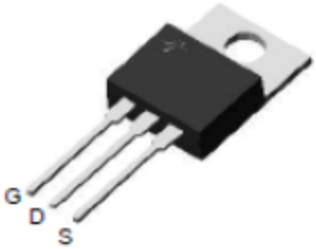
Marking Code = CM170N10GP

Date Code = XXXX

Equivalent Circuit and Pin Configuration



TO-220C



Ordering Information

P/N	Package Type	Packaging
CM170N10GP	TO-220C	Tube

Absolute Maximum Ratings (Tc=25 ℃ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		VDS	100	V
Gate-source Voltage		VGS	±20	V
Continuous Drain Current (1)	Tc=25°C(Silicon Limit)	ID	211	A
	Tc=25°C(Package Limit)		120	
	Tc=100°C (Silicon Limit)		116	
Pulsed Drain Current(2)		IDM	480	A
Total Power Dissipation (3)		PD @ Tc=25°C	416	W
		Derating Factor above 25°C	2.78	W/°C
Sungle Puls Avalanche Energy(4)		EAS	540	mJ
Thermal Resistance Junction-to-Case (3)		RθJC	0.63	°C/W
Junction and Storage Temperature Range		TJ,TSTG	-55 to +150	°C

Electrical Characteristics (T_C=25 ℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V,T_C=25°C			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2.0		4.0	V
Static Drain-Source on-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=30A		3.0	3.9	mΩ
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V			1.2	V
Maximum Body-Diode Continuous Current	I_S				211	A
Dynamic Parameters						
Input Capacitance	Ciss	V_{DS}=50V,V_{GS}=0V,f=100KHz		9050		pF
Output Capacitance	Coss			1300		
Reverse Transfer Capacitance	Crss			20		
Switching Parameters						
Total Gate Charge	Qg	V_{DS}=50V,I_D=20A,V_{GS}=10V		126		nC
Gate Source Charge	Qgs			38		
Gate Drain Charge	Qgd			22		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=50V, I_D=20A,R_G=2Ω		44		ns
Turn-on Rise Time	tr			20		
Turn-off Delay Time	$t_{D(off)}$			102		
Turn-off Fall Time	tf			23		

Noted: (1) Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

(2) Pulse width limited by maximum junction temperature.

(3) Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. With 2oz Copper, t≤10s.

(4) E_{AS} is tested at starting T_j = 25°C, L=0.5mH,I_{AS}=46.5A,V_{GS}=10V.

Typical Performance Characteristics

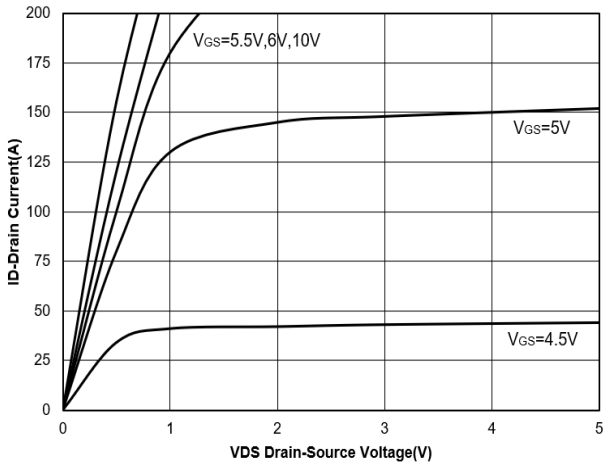


Figure 1. Output Characteristics

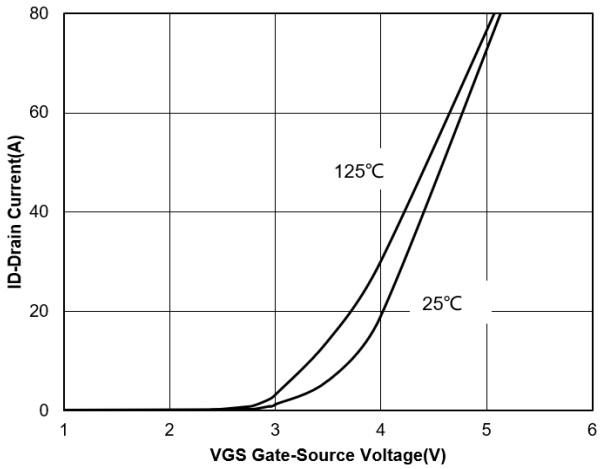


Figure 2. Transfer Characteristics

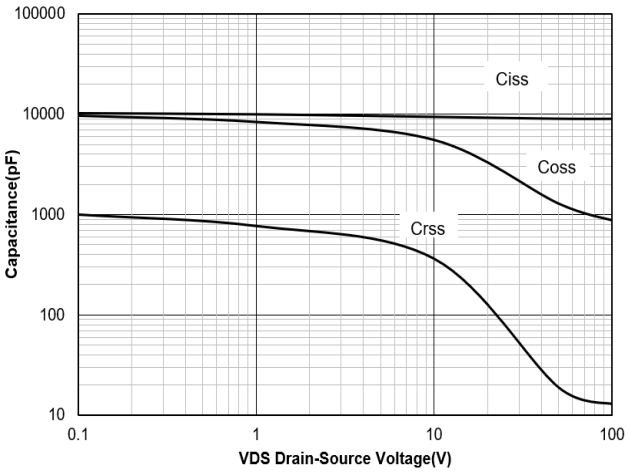


Figure 3. Capacitance Characteristics

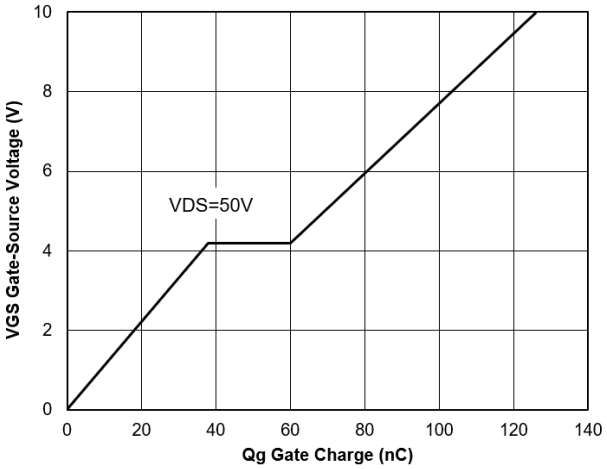


Figure 4. Gate Charge

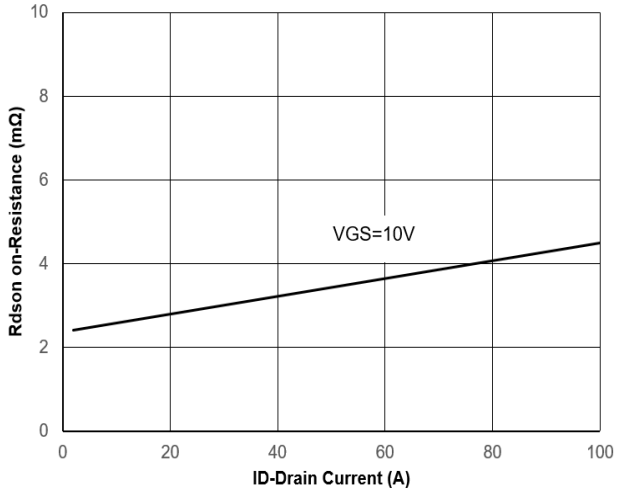


Figure 5. Drain-Source on Resistance

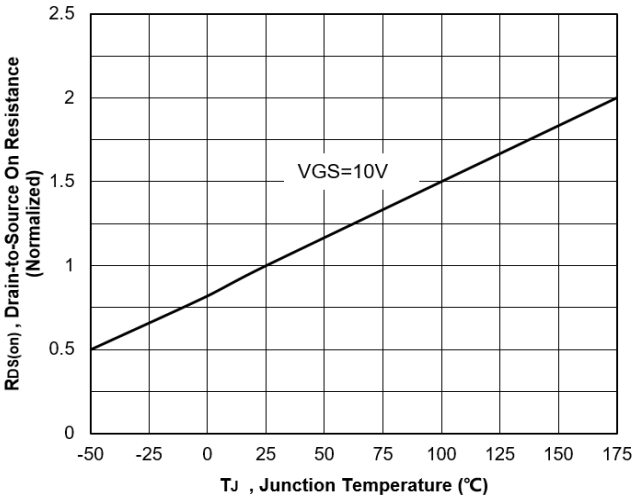


Figure 6. Normalized On-Resistance Vs. Temperature

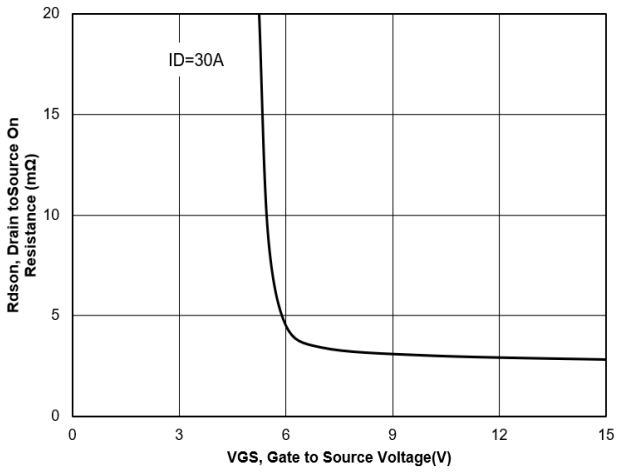


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

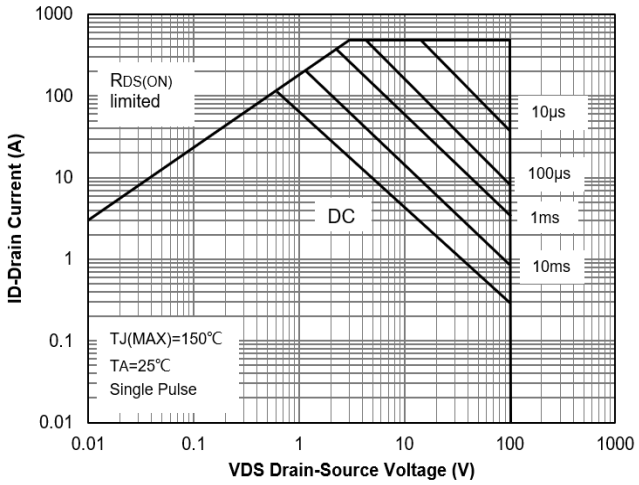


Figure 8. Safe Operation Area

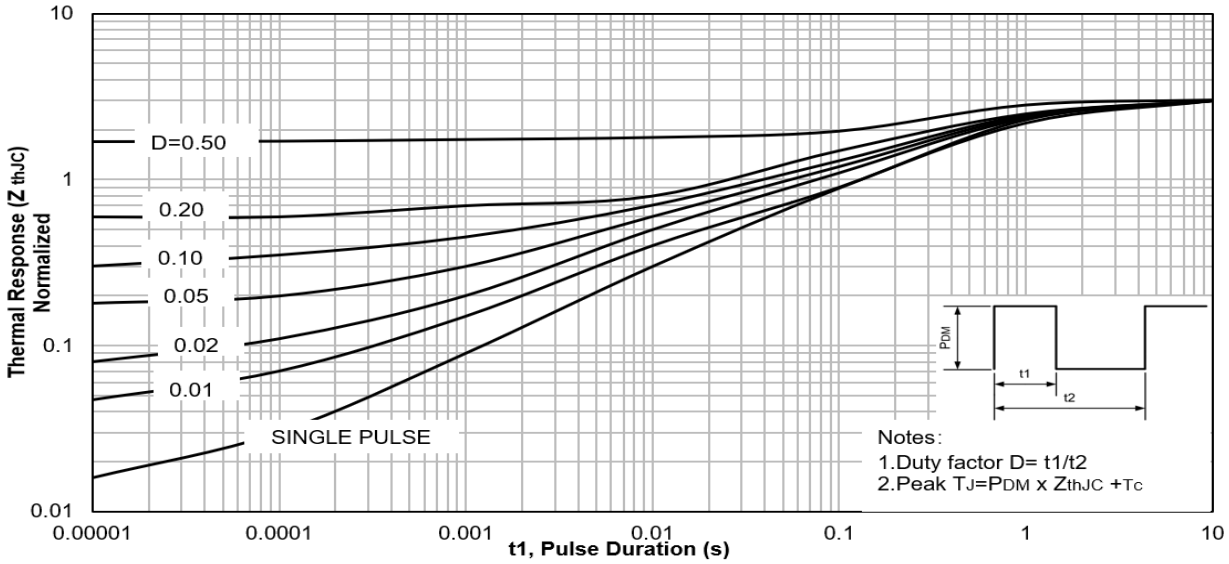


Figure 9. Maximum Effective Transient Thermal Impedance ,Junction-to-Case

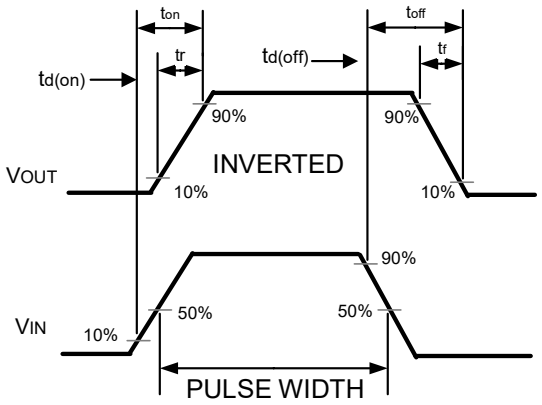
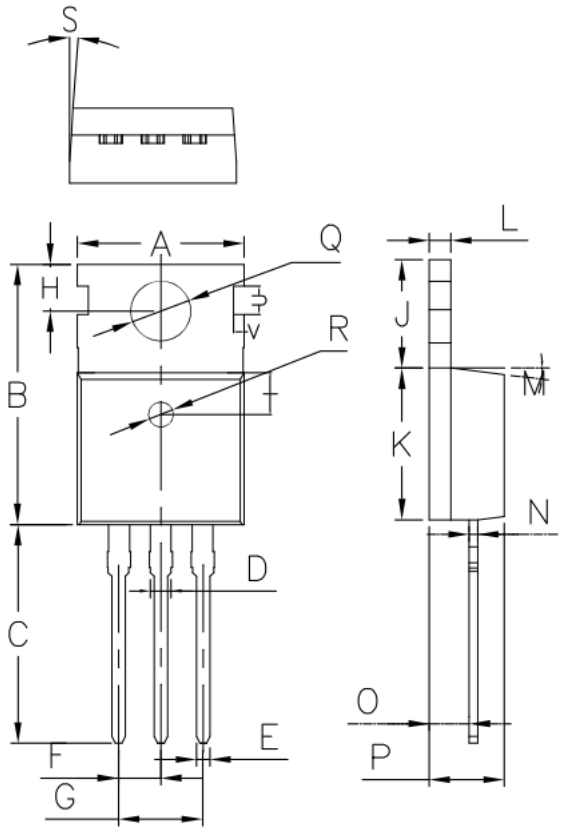


Figure 10. Switching wave

TO-220C Package Outline Drawing



Sym-bol	Millimeters		
	Min.	Nom.	Max.
A	9.80	10.00	10.20
B	15.40	15.60	15.80
C	13.02	13.37	13.72
D	1.18	1.31	1.44
E	0.70	0.80	0.90
F	2.42	2.54	2.66
G	4.84	5.08	5.32
H	2.73	2.80	2.87
I	2.40	2.50	2.60
J	6.40	6.50	6.60
K	9.00	9.10	9.20
L	1.29	1.30	1.32
M	6.5°	7.0°	7.5°
N	0.48	0.50	0.56
O	2.35	2.40	2.50
P	4.40	4.50	4.70
Q	3.50	3.60	3.70
R	1.30	1.40	1.50
S	2°	2.5°	3°
U	1.65	1.75	1.85
V	0.58	0.68	0.78

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