

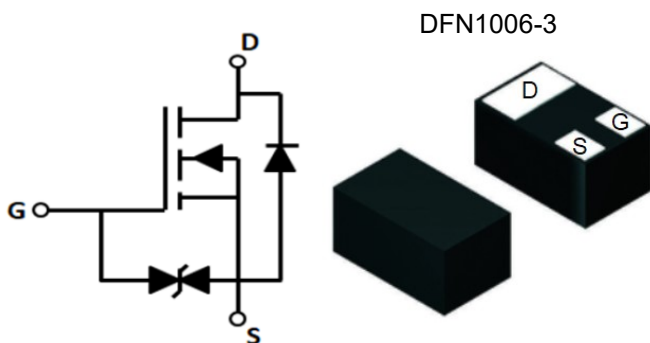
## Description

CM1602A is the N-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

## Features

- $V_{DS}$ : 20V
- $I_D$ : 0.9A
- $R_{DS(on)}$  (@ $V_{GS}=4.5V$ ) : < 250m $\Omega$
- $R_{DS(on)}$  (@ $V_{GS}=2.5V$ ) : < 350m $\Omega$
- High density cell design for extremely low  $R_{DS(on)}$
- Excellent on-resistance and DC current capability

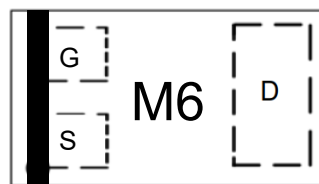
## Equivalent Circuit and Pin Configuration



## Applications

- Cellular Handsets and Accessories
- Personal Digital Assistants
- Portable Instrumentation
- Load switch

## Marking Information



Device Code = M6

## Ordering Information

Part Number	Packaging	Reel Size
CM1602A	10000/Tape & Reel	7 inch

## Absolute Maximum Ratings (TA=25 °C unless otherwise noted)

Parameter	Symbol	Maximum	Unit	
Drain-source Voltage	$V_{DS}$	20	V	
Gate-source Voltage	$V_{GS}$	$\pm 10$	V	
Continuous Drain Current	$I_D$	$T_A=25^\circ\text{C}$ , $t \leq 5\text{s}$	1	A
		$T_A=25^\circ\text{C}$ , Steady State	0.9	A
		$T_A=75^\circ\text{C}$ , Steady State	0.69	A
Pulsed Drain Current <sup>(1)</sup>	$I_{DM}$	4.0	A	
Total Power Dissipation @ $T_A=25^\circ\text{C}$ <sup>(2)</sup>	$P_D$	$t \leq 5\text{s}$	430	mW
		Steady State	340	
Thermal Resistance Junction-to-Ambient <sup>(2)</sup> @ $t \leq 5\text{s}$	$R_{\theta JA}$	294	$^\circ\text{C/W}$	
Thermal Resistance Junction-to-Ambient <sup>(2)</sup> @Steady State		366		
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$	

**Electrical Characteristics (T<sub>J</sub>=25 °C unless otherwise noted)**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, T <sub>C</sub> =25°C			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±10V, V <sub>DS</sub> =0V			±10	uA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.35	0.75	1.1	V
Static Drain-Source on-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =0.5A		190	250	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =0.45A		270	350	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =0.6A, V <sub>GS</sub> =0V			1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				0.9	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =16V, V <sub>GS</sub> =0V, f=1MHz		26		pF
Output Capacitance	C <sub>oss</sub>			9		
Reverse Transfer Capacitance	C <sub>rss</sub>			5		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =10V, I <sub>D</sub> =0.5A		0.84		nC
Gate Source Charge	Q <sub>gs</sub>			0.25		
Gate Drain Charge	Q <sub>gd</sub>			0.10		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =4.5V, V <sub>DD</sub> =10V, I <sub>D</sub> =0.5A, R <sub>GEN</sub> =10Ω		2		ns
Turn-on Rise Time	t <sub>r</sub>			18.8		
Turn-off Delay Time	t <sub>D(off)</sub>			10		
Turn-off Fall Time	t <sub>f</sub>			23		

Noted: (1) Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

(2) Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6cm<sup>2</sup>.

**Typical Performance Characteristics**

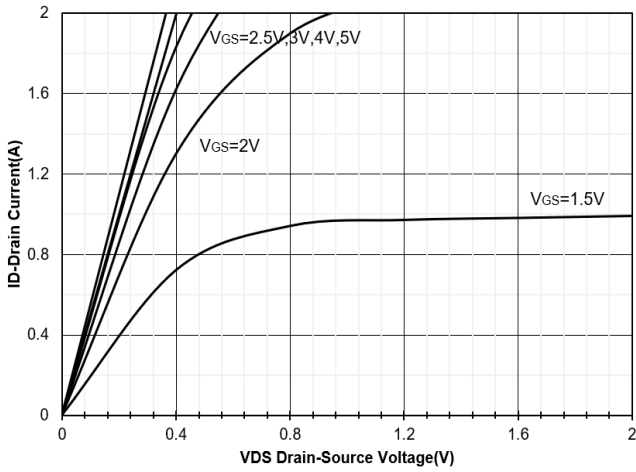


Figure 1. Output Characteristics

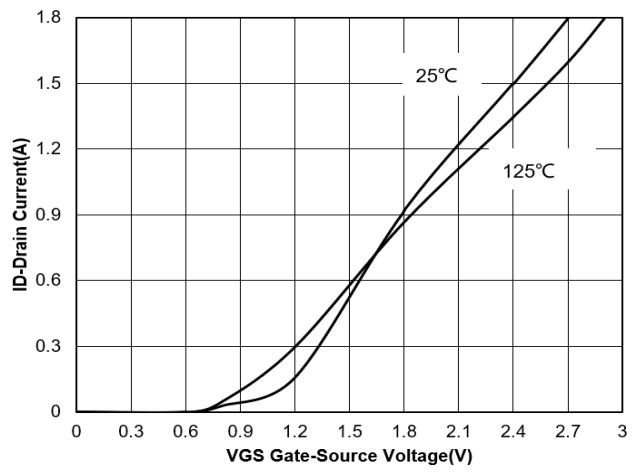


Figure 2. Transfer Characteristics

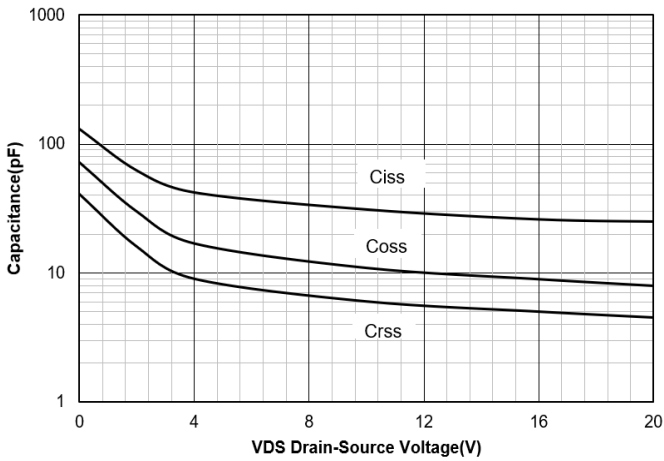


Figure 3. Capacitance Characteristics

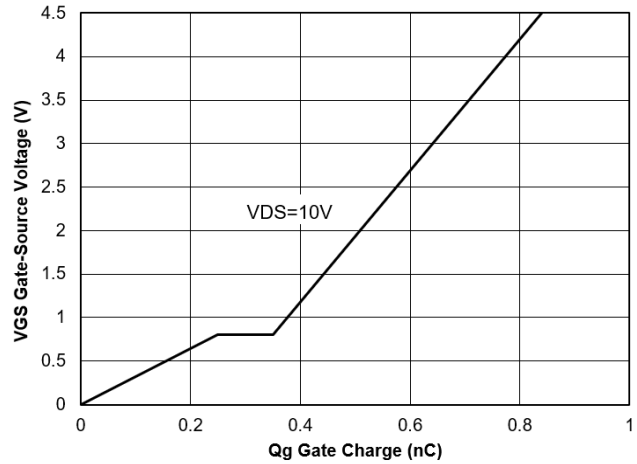


Figure 4. Gate Charge

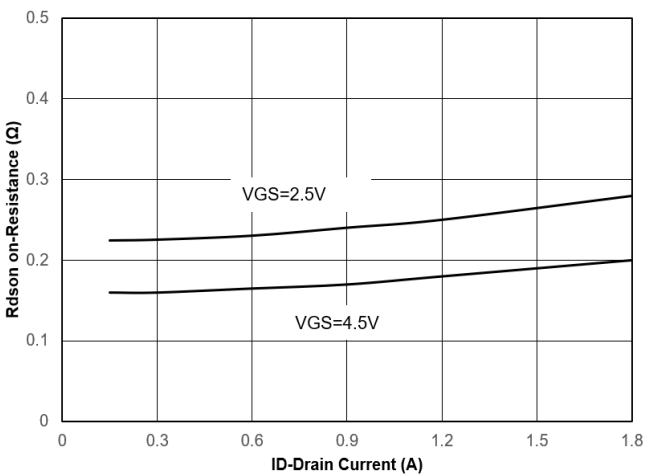


Figure 5. Drain-Source on Resistance

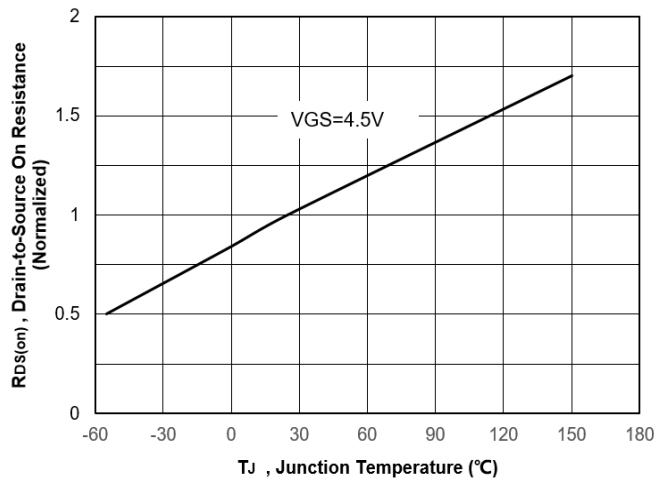


Figure 6. Normalized On-Resistance Vs. Temperature

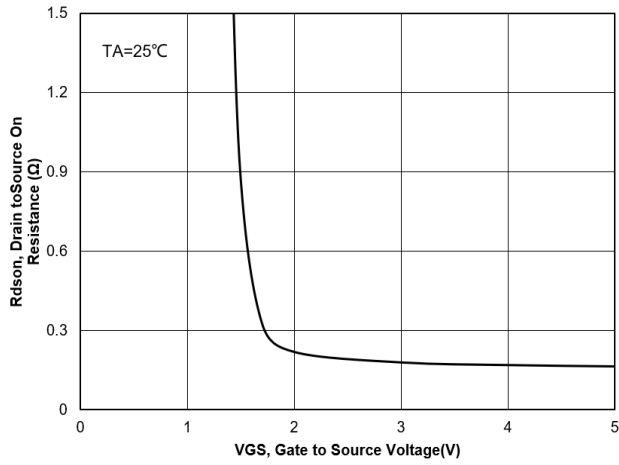


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

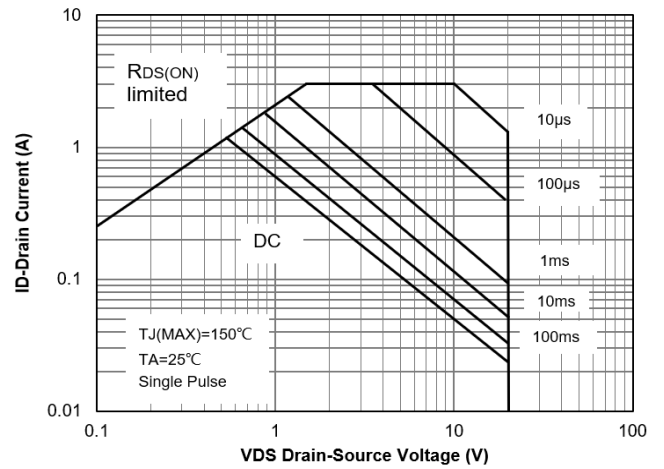


Figure 8. Safe Operation Area

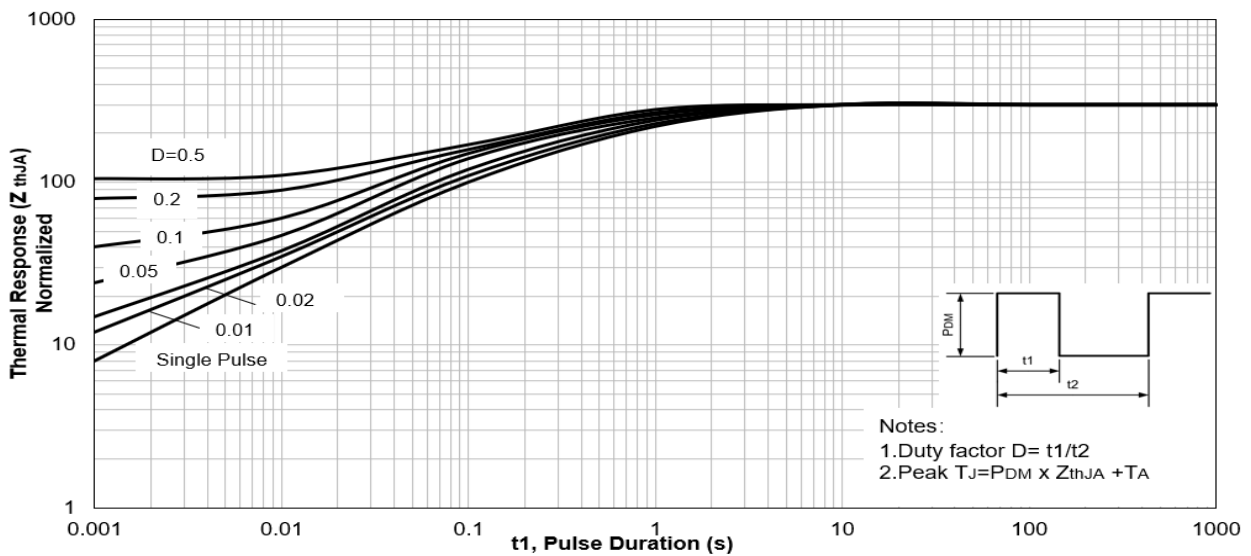


Figure 9. Maximum Effective Transient Thermal Impedance ,Junction-to-Ambient

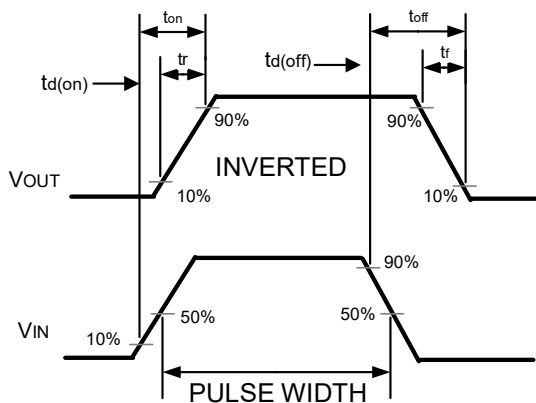
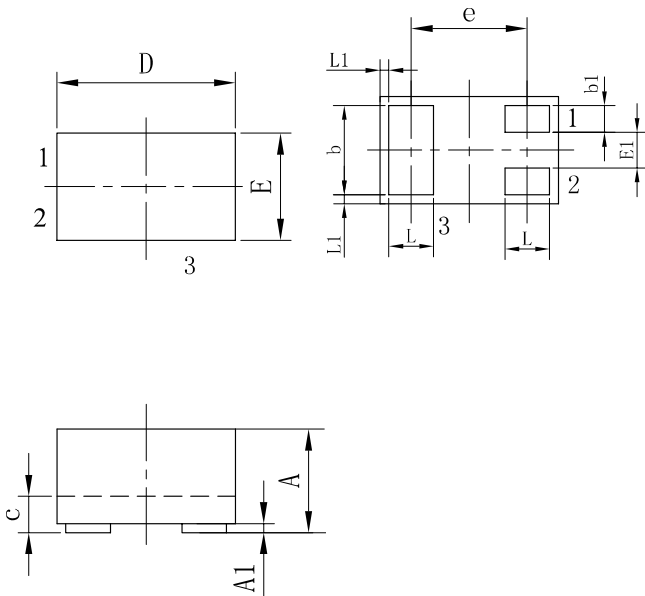


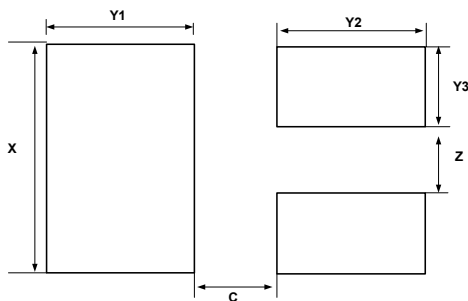
Figure 10. Switching wave

### DFN1006-3 Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.45	0.50	0.55	0.018	0.020	0.022
b1	0.10	0.15	0.20	0.004	0.006	0.008
c	0.12	0.15	0.18	0.005	0.006	0.007
D	0.95	1.00	1.05	0.037	0.039	0.041
e	0.65 BSC			0.026 BSC		
E	0.55	0.60	0.65	0.022	0.024	0.026
E1	0.15	0.20	0.25	0.006	0.008	0.010
L	0.20	0.25	0.30	0.008	0.010	0.012
L1	0.05 REF			0.0002 REF		

### Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
C	0.25	0.010
X	0.65	0.024
Y1	0.50	0.020
Y2	0.50	0.020
Y3	0.25	0.010
Z	0.20	0.008

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