Description

CM1202 is the N-Channel enhancement mode power field effect transistors with high cell density, trench technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

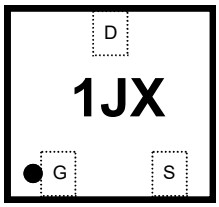
Applications

- Cellular Handsets and Accessories
- Personal Digital Assistants
- Portable Instrumentation
- Load switch

Features

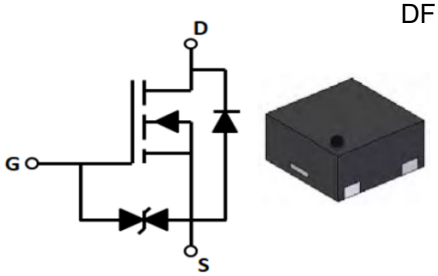
- V_{DS}: 20V
- I_D: 0.8A
- $R_{DS_{ON}}$ ($@V_{GS}$=4.5V) : < 250mΩ
- $R_{DS_{ON}}$ ($@V_{GS}$=2.5V) : < 358mΩ
- High density cell design for extremely low $R_{DS_{ON}}$
- Excellent on-resistance and DC current capability

Marking Information

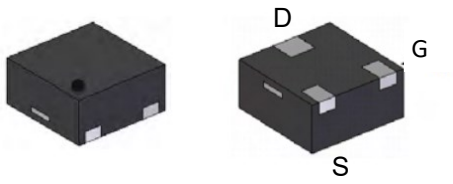


Device Code = 1J
Data Code =X

Equivalent Circuit and Pin Configuration



DFN1.2*1.2-3L



Ordering Information

Part Number	Packaging	Reel Size
CM1202	5000/Tape & Reel	7 inch

Absolute Maximum Ratings (T_A=25 ℃ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	20	V
Gate-source Voltage		V_{GS}	±10	V
Continuous Drain Current	T_A=25°C , Steady State	I_D	0.8	A
	T_A=75°C ,Steady State		0.6	A
Pulsed Drain Current[1]		I_{DM}	3.0	A
Total Power Dissipation @ T_A=25°C [2]	@Steady State	P_D	310	mW
Thermal Resistance Junction-to-Ambient [2]	@Steady State	$R_{\theta JA}$	400	°C/W
Junction and Storage Temperature Range		T_J,T_{STG}	-55 to +150	°C

Electrical Characteristics (T_J=25 ℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V,V_{GS}=0V,T_C=25°C			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±10V,V_{DS}=0V			±10	uA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	0.35	0.75	1.1	V
Static Drain-Source on-Resistance	$R_{DS(on)}$	V_{GS}=4.5V,I_D=0.5A		190	250	mΩ
		V_{GS}=2.5V,I_D=0.3A		275	358	
Diode Forward Voltage	V_{SD}	I_S=0.8A,V_{GS}=0V			1.2	V
Maximum Body-Diode Continuous Current	I_S				0.8	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=16V,V_{GS}=0V,f=1MHz		25		pF
Output Capacitance	C_{oss}			8.1		
Reverse Transfer Capacitance	C_{rss}			3.8		
Switching Parameters						
Total Gate Charge	Qg	V_{GS}=4.5V,V_{DS}=10V,I_D=0.5A		3.8		nC
Gate Source Charge	Qgs			1.4		
Gate Drain Charge	Qgd			0.3		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=4.5V,V_{DD}=10V, I_D=0.5A,R_{GEN}=10Ω		5.4		ns
Turn-on Rise Time	tr			3.2		
Turn-off Delay Time	$t_{D(off)}$			17.8		
Turn-off Fall Time	tf			3.1		

Noted: (1) Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

(2) Surface mounted on FR4 board using the minimum recommended pad size.

Typical Performance Characteristics

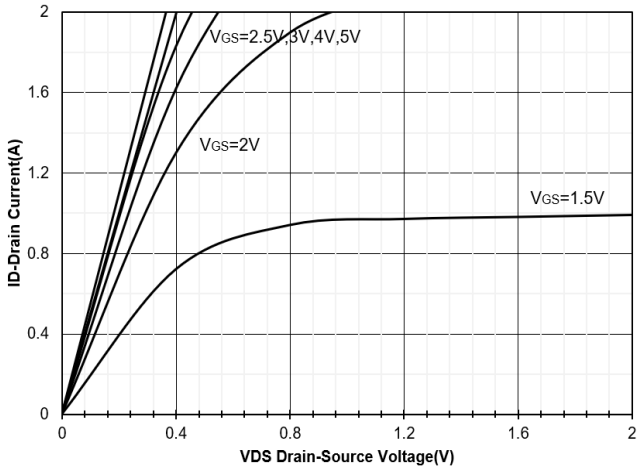


Figure 1. Output Characteristics

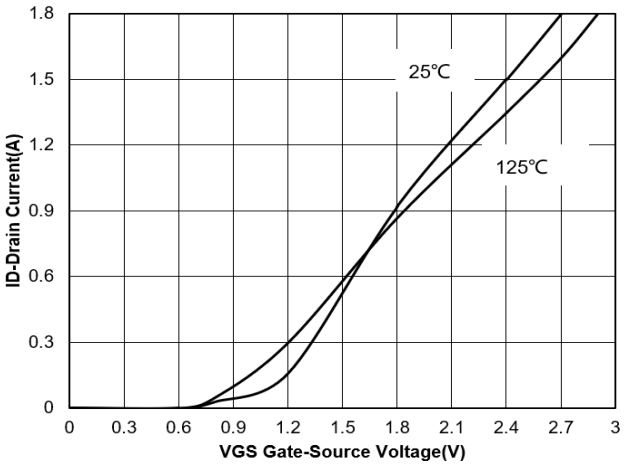


Figure 2. Transfer Characteristics

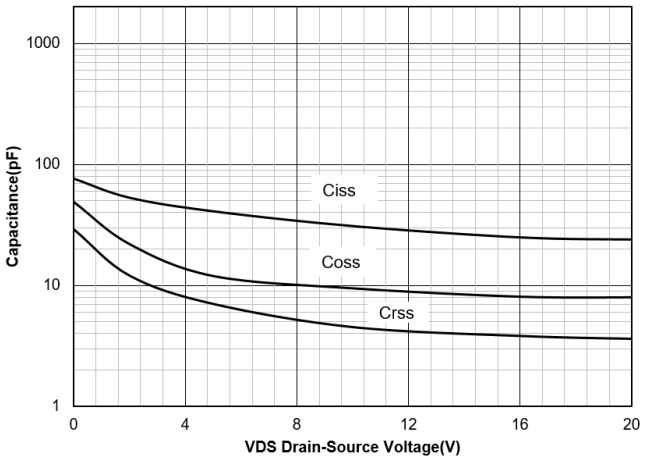


Figure 3. Capacitance Characteristics

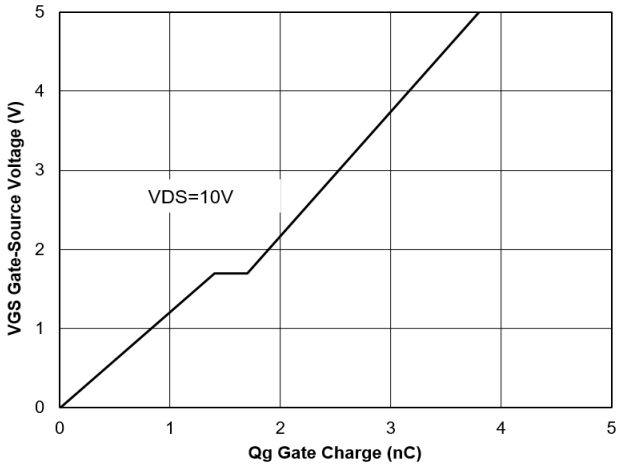


Figure 4. Gate Charge

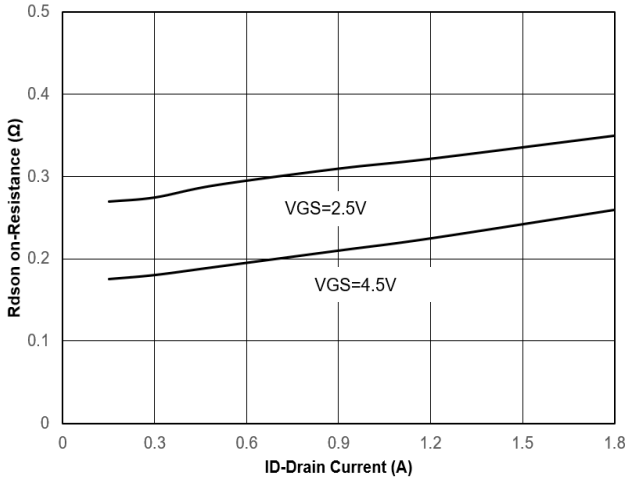


Figure 5. Drain-Source on Resistance

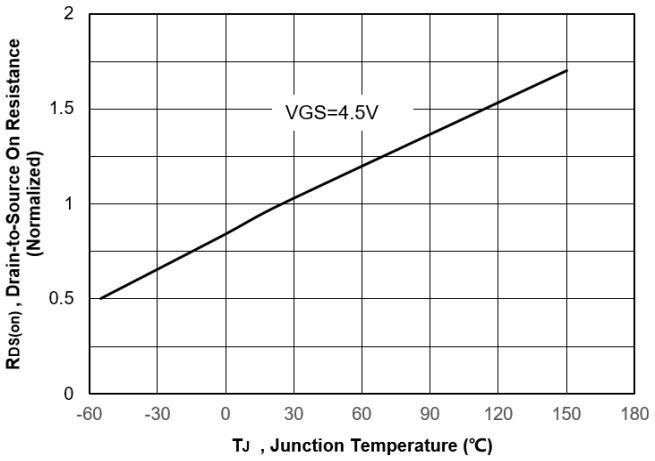


Figure 6. Normalized On-Resistance Vs. Temperature

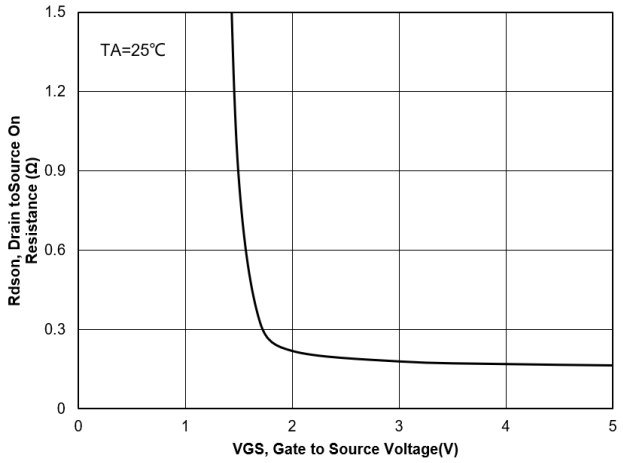


Figure 6. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

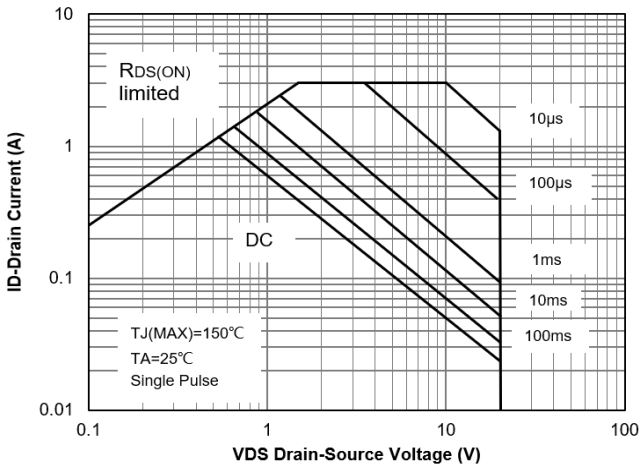


Figure 7. Safe Operation Area

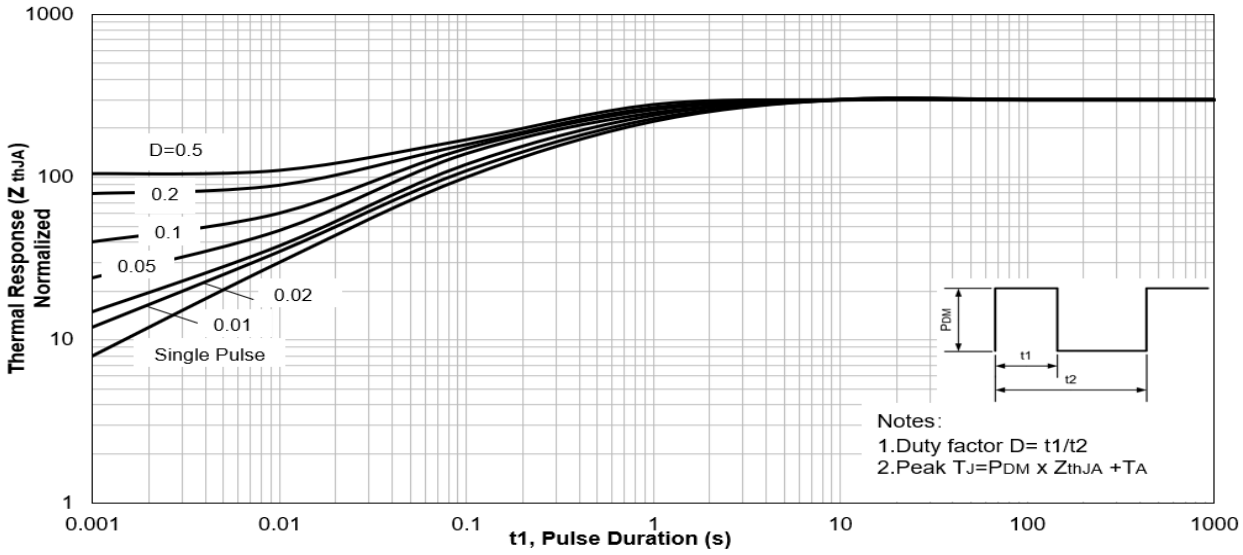


Figure 8. Maximum Effective Transient Thermal Impedance ,Junction-to-Ambient

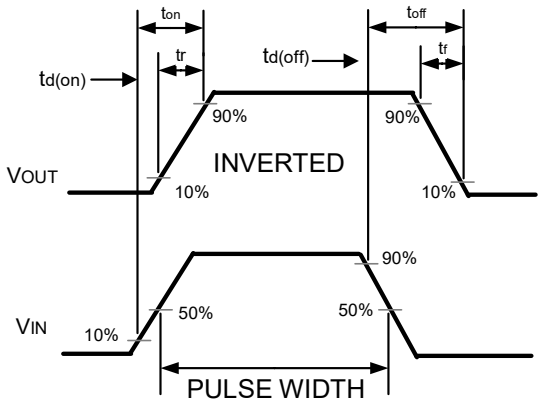
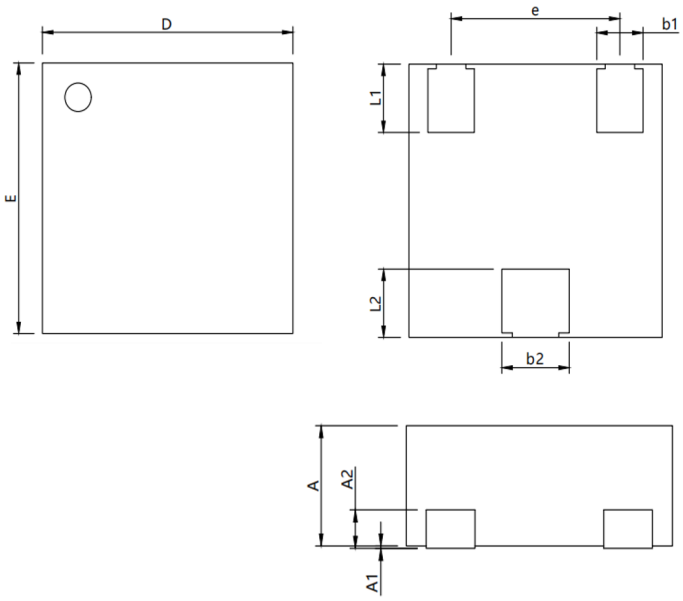


Figure 9. Switching wave

DFN1.2*1.2-3L Package Outline Drawing



SYM	DIMENSIONS		
	MILLIMETERS		
	MIN	TYP	MAX
D	1.15	1.20	1.25
E	1.15	1.20	1.25
e	0.80bsc		
L1	0.25	0.30	0.35
L2	0.25	0.30	0.35
b1	0.17	0.22	0.27
b2	0.28	0.32	0.37
A	0.45	0.50	0.55
A1	-	0.00	0.05
A2	0.152bsc		

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