

### Description

The CM07N65AHP/F is the N-Channel enhancement mode power field effect transistors with high cell density, high voltage planar technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance, .

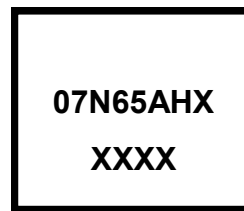
### Features

- VDS: 650V
- ID (@VGS=10V): 7A
- RDS<sub>ON</sub> (@VGS=10V) : < 1.4Ω
- High density cell design for extremely low RDS<sub>ON</sub>
- Excellent on-resistance and DC current capability

### Applications

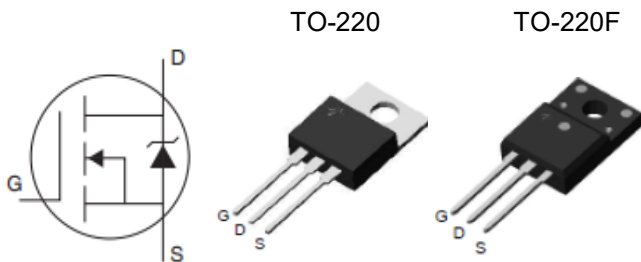
- AC/DC load switch
- SMPS
- LED power

### Marking Information



X=Package type  
 XXXX = Marking Code

### Equivalent Circuit and Pin Configuration



### Ordering Information

P/N	Package Type	Packaging
CM07N65AHP	TO-220	Tube
CM07N65AHF	TO-220F	Tube

### Absolute Maximum Ratings (T<sub>c</sub>=25 °C unless otherwise noted)

Parameter	Symbol	Maximum		Unit	
		CM07N65AHP	CM07N65AHF		
Drain-source Voltage	V <sub>DS</sub>	650		V	
Gate-source Voltage	V <sub>GS</sub>	±30		V	
Continuous Drain Current <sup>(1)</sup>	I <sub>D</sub>	T <sub>c</sub> =25°C	7	7 <sup>(4)</sup>	A
		T <sub>c</sub> =100°C	4.1	4.1 <sup>(4)</sup>	A
Pulsed Drain Current <sup>(2)</sup>	I <sub>DM</sub>	28	28	A	
Total Power Dissipation <sup>(3)</sup>	P <sub>D</sub> @ T <sub>c</sub> =25°C	144	85	W	
	Derating Factor above 25°C	1.1	0.7	W/°C	
Thermal Resistance Junction-to-Case <sup>(3)</sup>	R <sub>θJC</sub>	0.87	1.47	°C/W	
Junction and Storage Temperature Range	T <sub>J</sub> ,T <sub>STG</sub>	-55 to +150		°C	

**Electrical Characteristics (T<sub>c</sub>=25 °C unless otherwise noted)**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BVDSS	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	650			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =650V, V <sub>GS</sub> =0V, T <sub>C</sub> =25°C			5	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±30V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2.0		4.0	V
Static Drain-Source on-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =3.5A		1.2	1.4	Ω
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =7A, V <sub>GS</sub> =0V		0.8	1.2	V
Maximum Body-Diode Continuous Current	I <sub>S</sub>				7	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz		1190		pF
Output Capacitance	C <sub>oss</sub>			90		
Reverse Transfer Capacitance	C <sub>rss</sub>			2.9		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =520V, I <sub>D</sub> =7A, V <sub>GS</sub> =10V		26.5		nC
Gate Source Charge	Q <sub>gs</sub>			4.9		
Gate Drain Charge	Q <sub>gd</sub>			8.6		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =50V, I <sub>D</sub> =7A, R <sub>GEN</sub> =25Ω		37.6		ns
Turn-on Rise Time	t <sub>r</sub>			17.7		
Turn-off Delay Time	t <sub>D(off)</sub>			77.2		
Turn-off Fall Time	t <sub>f</sub>			24.3		

Noted: (1) Pulse Test: Pulse Width ≤ 300μs, Duty cycle ≤ 2%

(2) Pulse width limited by maximum junction temperature

(3) Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. With 2oz Copper, t ≤ 10s

(4) Drain current limited by maximum junction temperature

**Typical Performance Characteristics**

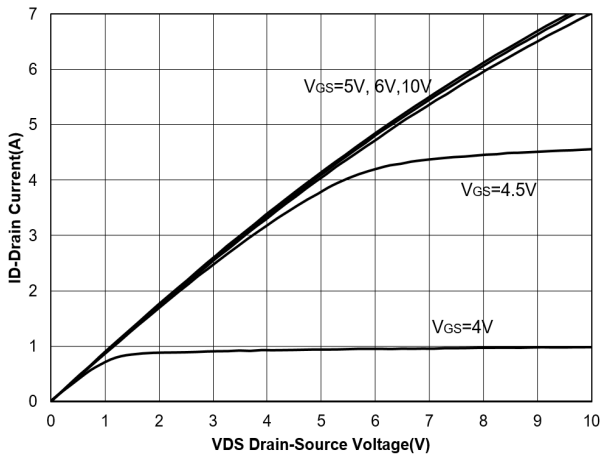


Figure 1. Output Characteristics

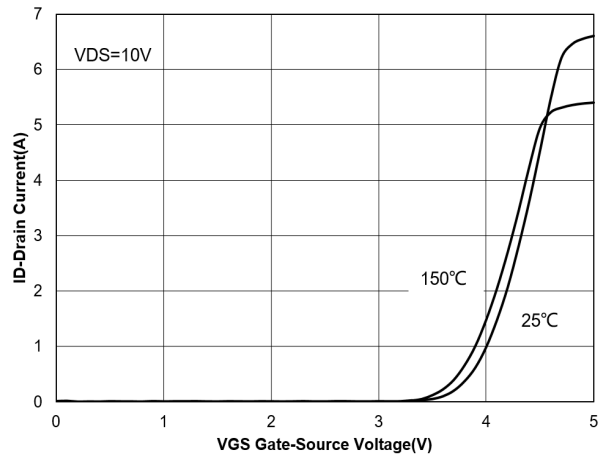


Figure 2. Transfer Characteristics

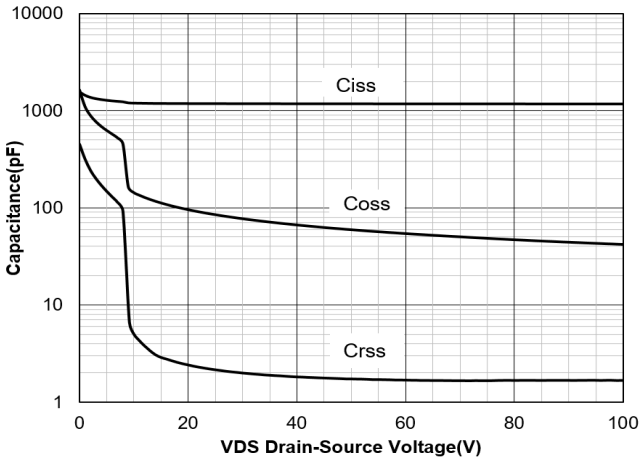


Figure 3. Capacitance Characteristics

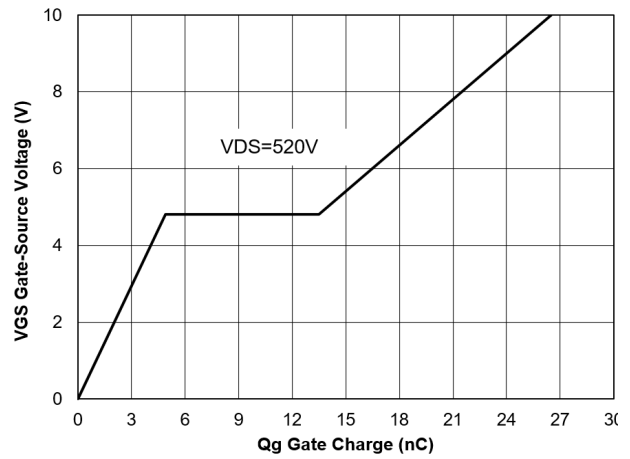


Figure 4. Gate Charge

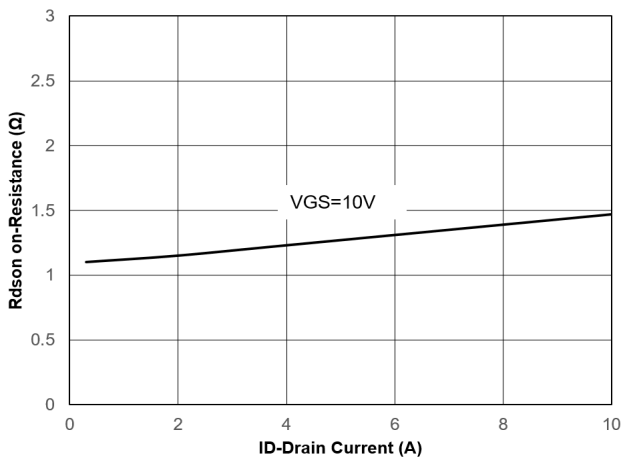


Figure 5. Drain-Source on Resistance

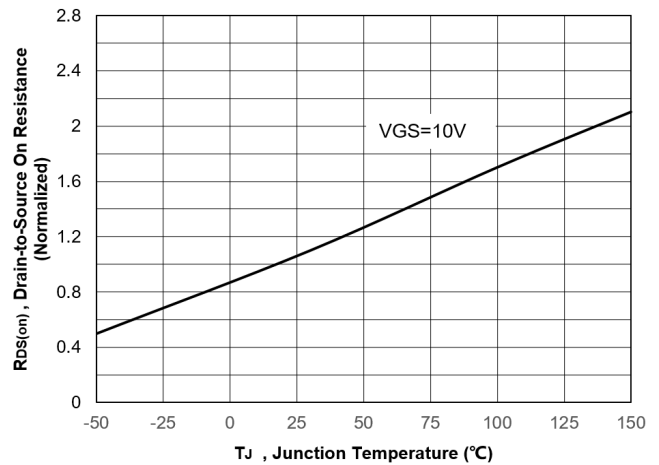


Figure 6. Normalized On-Resistance Vs. Temperature

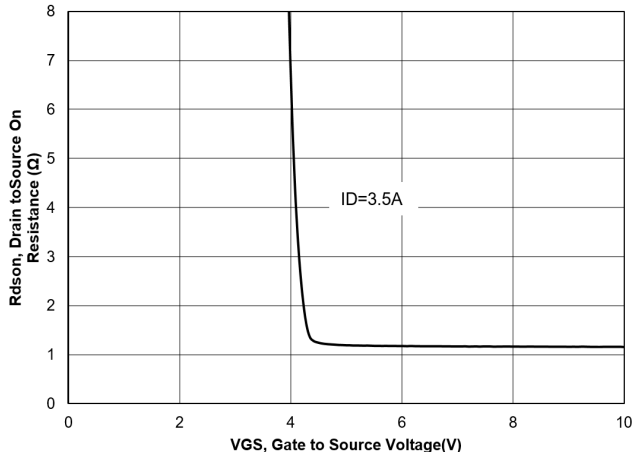


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

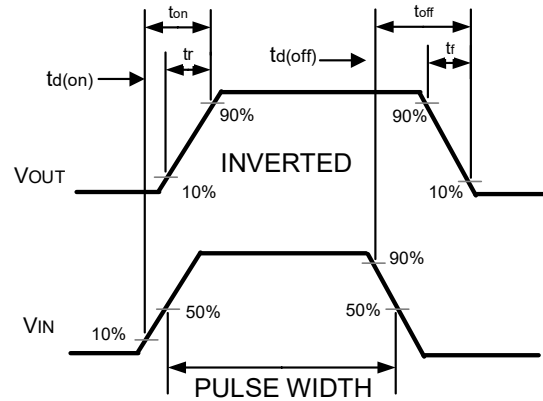


Figure 8. Switching wave

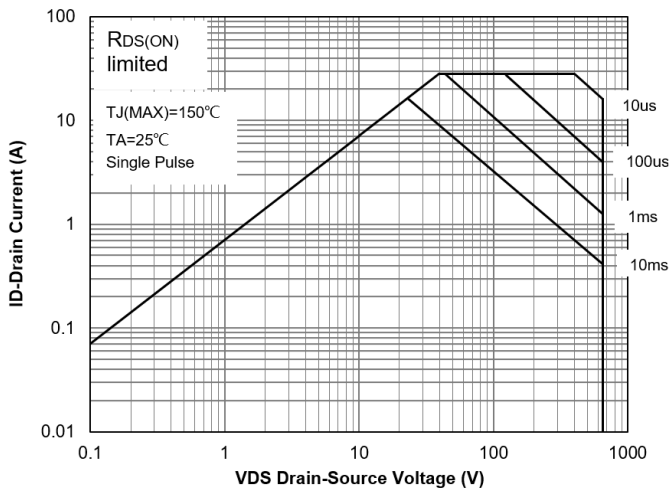


Figure 9. Safe Operation Area (TO-220)

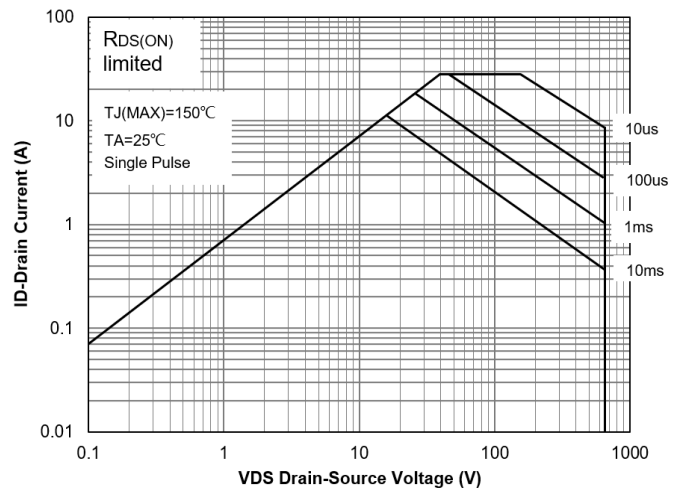


Figure 10. Safe Operation Area (TO-220F)

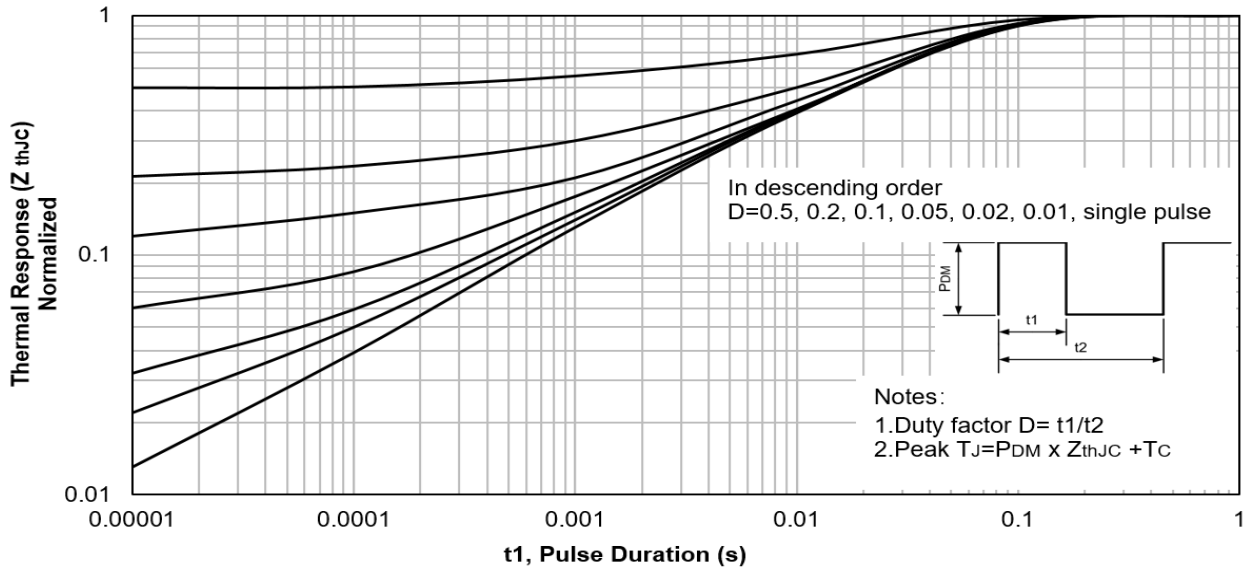


Figure 11. Maximum Effective Transient Thermal Impedance ,Junction-to-Case (TO-220)

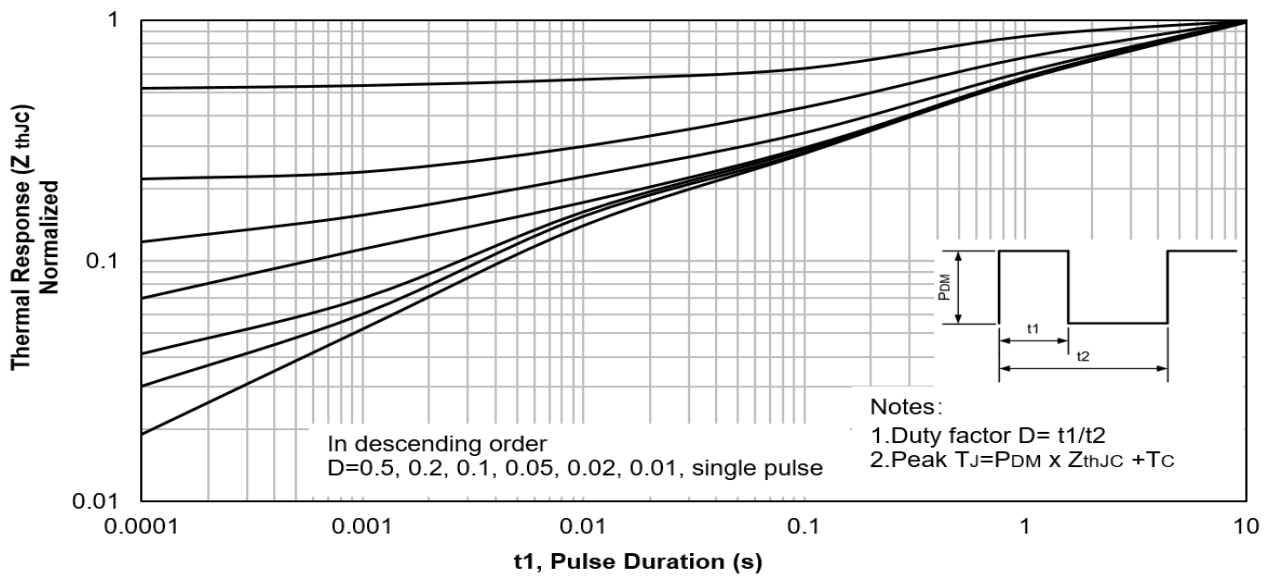
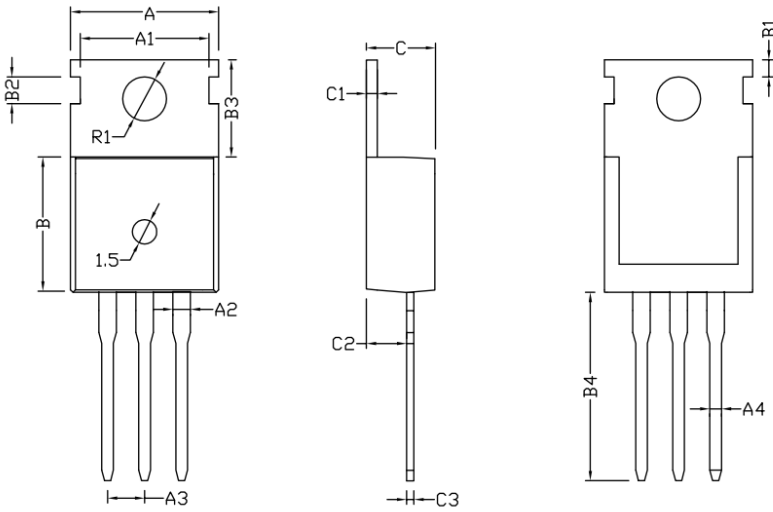
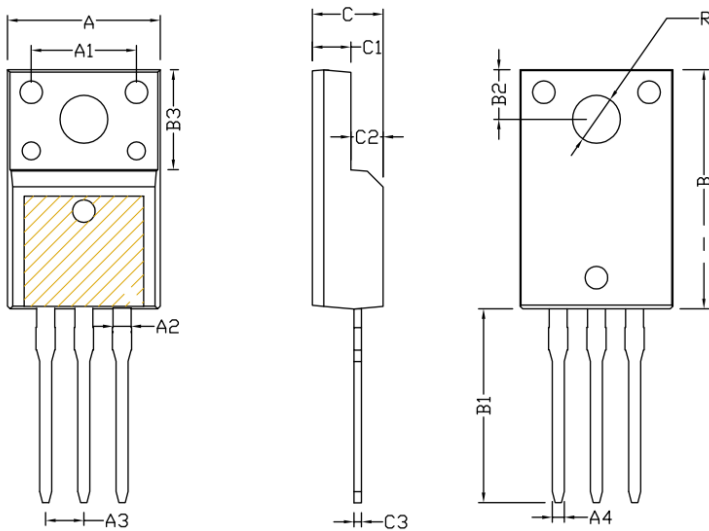


Figure 12. Maximum Effective Transient Thermal Impedance ,Junction-to-Case (TO-220F)

**TO-220 Package Outline Drawing**


SYMBOL	MM		
	MIN	NOM	MAX
A	9.78	9.88	9.98
A1	8.65	8.70	8.75
A2	1.22	1.27	1.35
A3	2.50	2.54	2.59
A4	0.77	0.80	0.83
B	8.70	9.20	9.70
B1	1.25	1.30	1.35
B2	1.65	1.70	1.75
B3	6.50	6.60	6.70
B4	12.90	13.08	13.18
C	4.42	4.50	4.58
C1	1.27	1.30	1.33
C2	2.37	2.40	2.43
C3	0.48	0.50	0.52
R	3.60	3.65	3.70

**TO-220F Package Outline Drawing**


SYMBOL	MM		
	MIN	NOM	MAX
A	10.03	10.13	10.23
A1	6.50	7.00	7.50
A2	1.20	1.28	1.36
A3		2.54	
A4	0.70	0.80	0.90
B	15.81	15.91	16.01
B1	12.79	12.89	12.99
B2	3.00	3.30	3.60
B3	6.60	6.65	6.70
C	4.62	4.70	4.78
C1	2.50	2.55	2.60
C2	2.10	2.15	2.20
C3		0.50	
R		3.18	