

Description

The CM05N65CHU/D is the N-Channel enhancement mode power field effect transistors with high cell density, high voltage planar technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

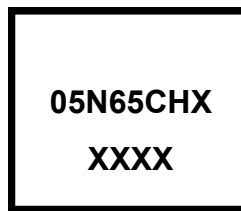
Features

- VDS: 650V
- ID (@VGS=10V): 5A
- RDS_{ON} (@VGS=10V) : < 2.2Ω
- High density cell design for extremely low RDS_{ON}
- Excellent on-resistance and DC current capability

Applications

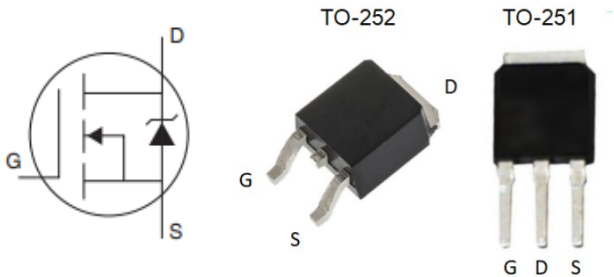
- AC/DC load switch
- SMPS
- LED power

Marking Information



X=Package type
 XXXX = Marking Code

Equivalent Circuit and Pin Configuration



Ordering Information

P/N	Package Type	Packaging	Remark
CM05N65CHU	TO-252	Tape and reel	ROHS
CM05N65CHD	TO-251	Tube	ROHS

Absolute Maximum Ratings (T_c=25 °C unless otherwise noted)

Parameter	Symbol	Maximum		Unit
		CM05N65CHU	CM05N65CHD	
Drain-source Voltage	V _{DS}	650		V
Gate-source Voltage	V _{GS}	±30		V
Continuous Drain Current ⁽¹⁾	I _D	T _c =25°C	5	A
		T _c =100°C	3	A
Pulsed Drain Current ⁽²⁾	I _{DM}	20		A
Total Power Dissipation ⁽³⁾	PD @ T _c =25°C	114		W
	Derating Factor above 25°C	0.91		W/°C
Thermal Resistance Junction-to-Case ⁽³⁾	R _{θJC}	1.1		°C/W
Junction and Storage Temperature Range	T _J ,T _{STG}	-55 to +150		°C

Electrical Characteristics (T_c=25 °C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	650			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =650V, V _{GS} =0V, T _c =25°C			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Static Drain-Source on-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =2.5A		1.9	2.2	Ω
Diode Forward Voltage	V _{SD}	I _S =5A, V _{GS} =0V		0.85	1.2	V
Maximum Body-Diode Continuous Current	I _S				5	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =100V, V _{GS} =0V, f=1MHz		620		pF
Output Capacitance	C _{oss}			28		
Reverse Transfer Capacitance	C _{rss}			3.3		
Switching Parameters						
Total Gate Charge	Q _g	V _{DS} =520V, I _D =5A, V _{GS} =10V		18		nC
Gate Source Charge	Q _{gs}			3.3		
Gate Drain Charge	Q _{gd}			9.2		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =50V, I _D =5A, R _{GEN} =25Ω		35		ns
Turn-on Rise Time	t _r			20		
Turn-off Delay Time	t _{D(off)}			49		
Turn-off Fall Time	t _f			21		

- Noted: (1) Pulse Test: Pulse Width ≤ 300μs, Duty cycle ≤ 2%
 (2) Pulse width limited by maximum junction temperature
 (3) Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. With 2oz Copper, t ≤ 10s

Typical Performance Characteristics

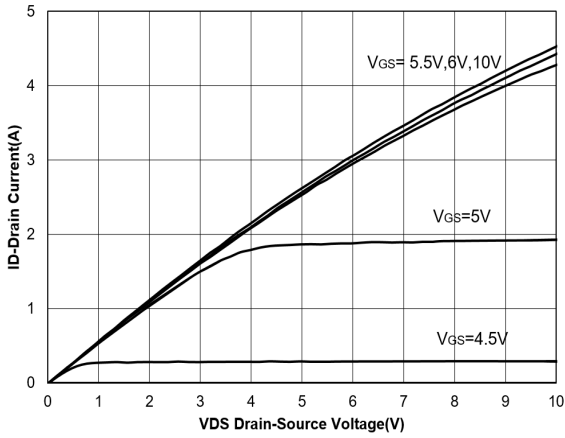


Figure 1. Output Characteristics

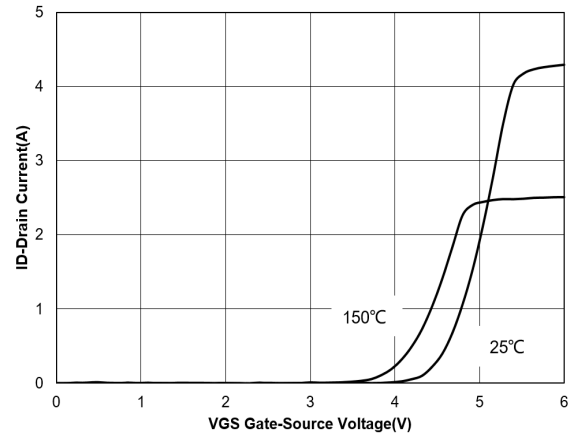


Figure 2. Transfer Characteristics

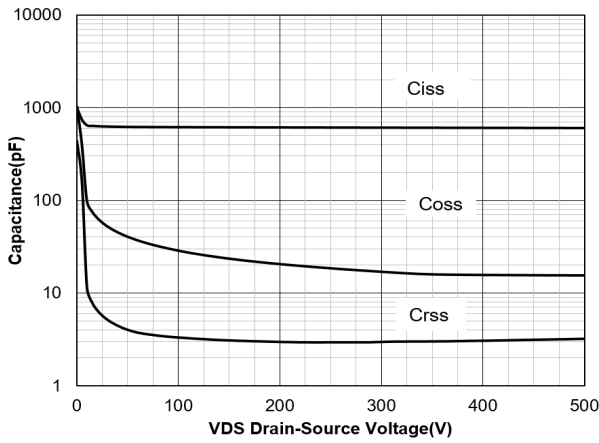


Figure 3. Capacitance Characteristics

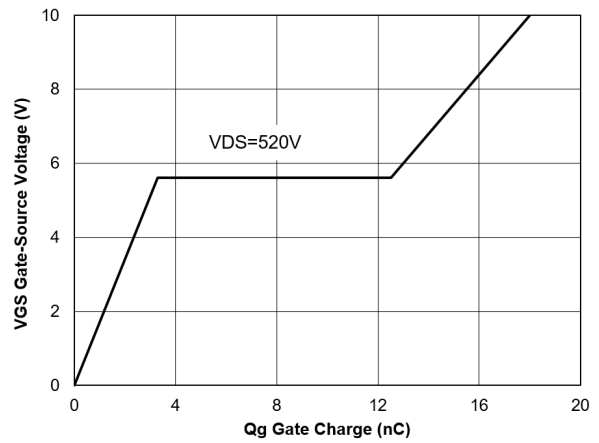


Figure 4. Gate Charge

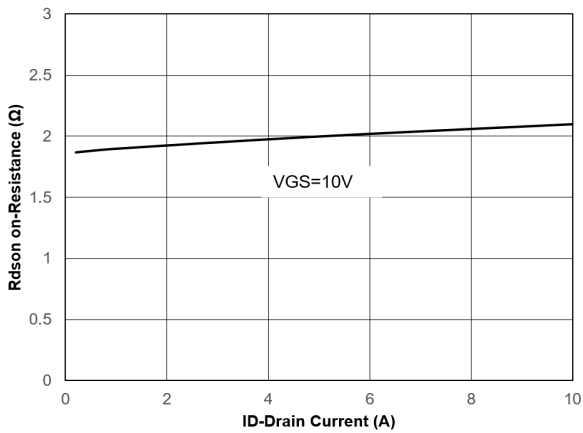


Figure 5. Drain-Source on Resistance

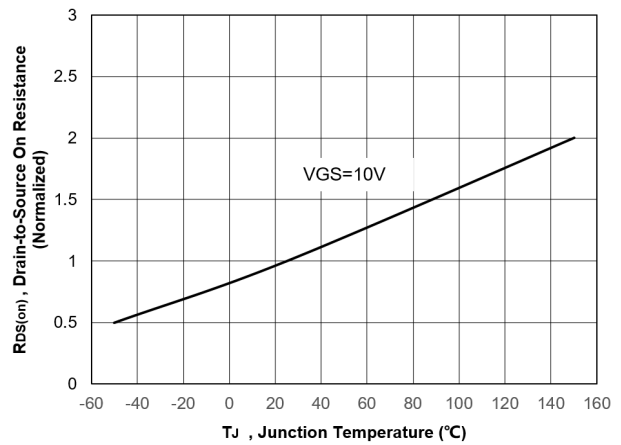


Figure 6. Normalized On-Resistance Vs. Temperature

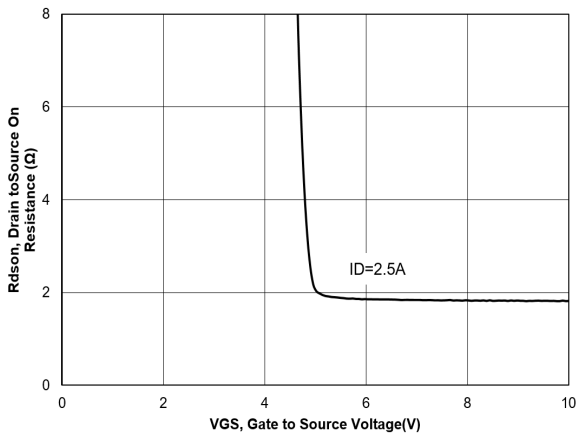


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

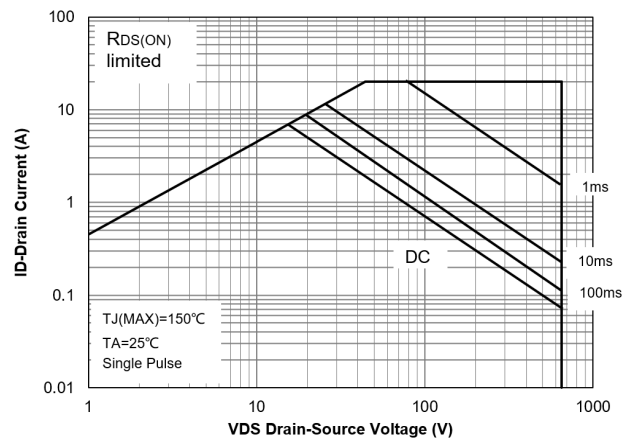


Figure 8. Safe Operation Area

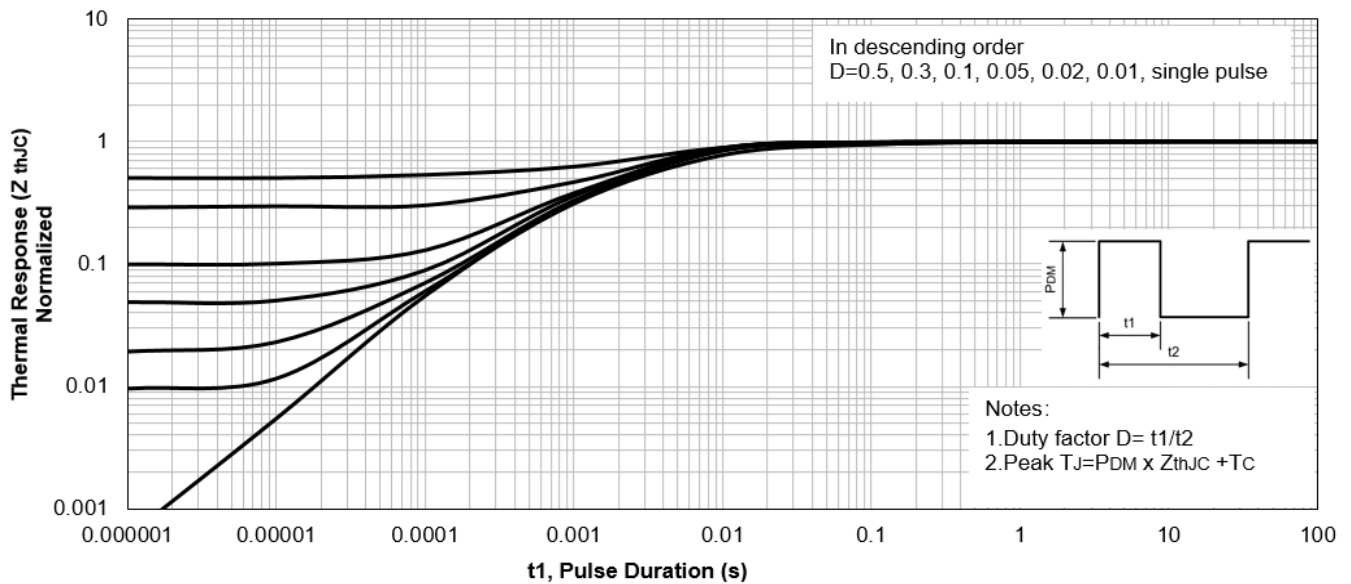


Figure 9. Maximum Effective Transient Thermal Impedance, Junction-to-Case

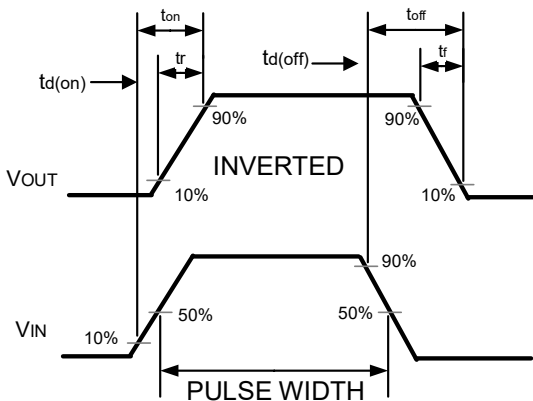
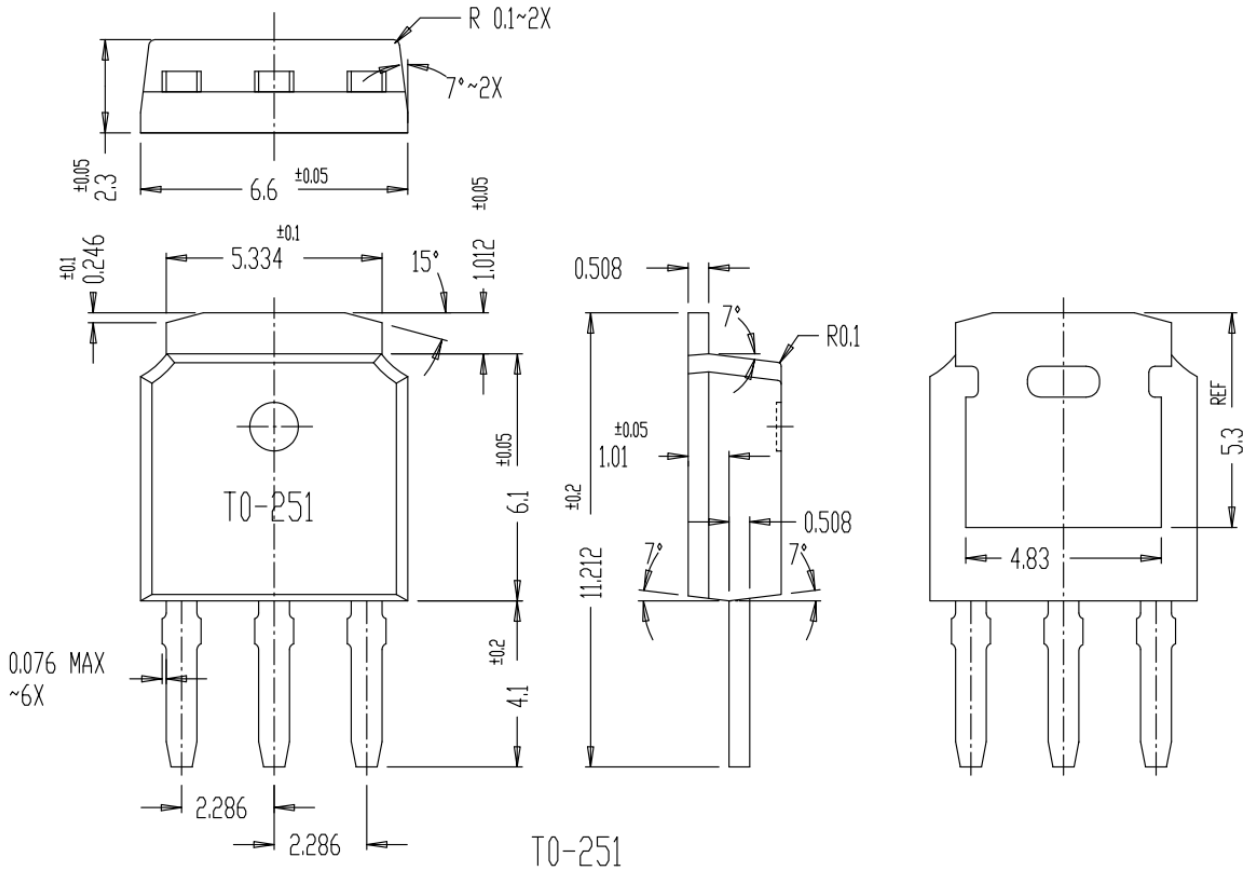
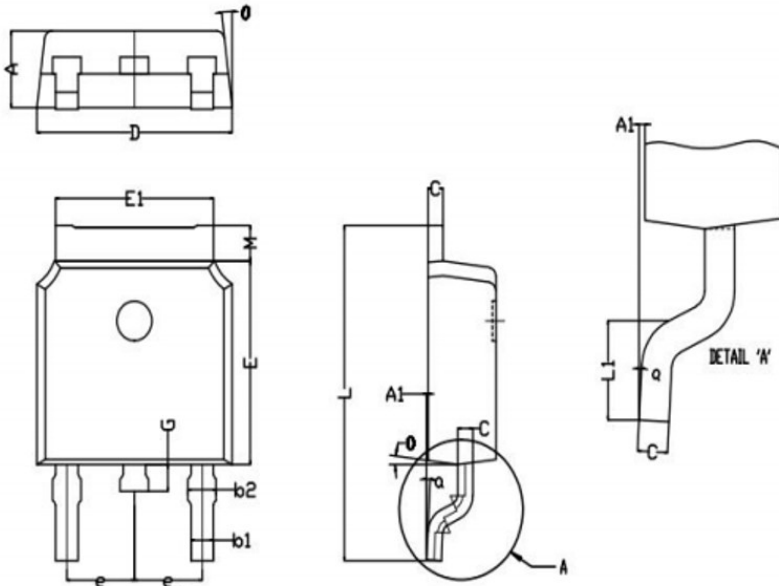


Figure 10. Switching wave

TO-251 Package Outline Drawing



TO-252 Package Outline Drawing



Symbol	Dim in mm		
	Min	Nom	Max
A	2.25	2.30	2.35
L1	2.90	3.00	3.10
b1	0.71	0.76	0.81
b2	0.91	0.96	1.01
C	0.46	0.51	0.56
D	6.55	6.60	6.65
e	2.29 BSC		
E	6.05	6.10	6.15
E1	5.23	5.33	5.43
L	9.84	10.04	10.24
A1	0.00	0.05	0.10
M	1.01	1.06	1.11
G	0.70	0.80	0.90
O	0°	5°	10°
Q	0°	3°	6°

Contact Information

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