Description

The CM05N50AHU/D is the N-Channel enhancement mode power field effect transistors with high cell density, high voltage planar technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance, .

Applications

- AC/DC load switch
- SMPS
- LED power

Features

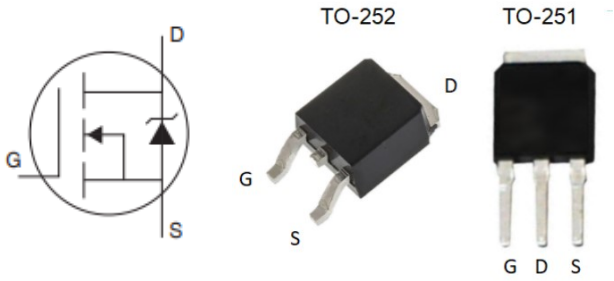
- VDS: 500V
- ID (@VGS=10V): 5A
- RDS_{ON} (@VGS=10V) : < 1.5Ω
- High density cell design for extremely low RDS_{ON}
- Excellent on-resistance and DC current capability

Marking Information

X=Package type

XXXX = Marking Code

Equivalent Circuit and Pin Configuration



Ordering Information

P/N	Package Type	Packaging	Remark
CM05N50AHU	TO-252	Tape and reel	ROHS
CM05N50AHD	TO-251	Tube	ROHS

Absolute Maximum Ratings (T_C=25 ℃ unless otherwise noted)

Parameter		Symbol	Maximum		Unit
			CM05N50AHU	CM05N50AHD	
Drain-source Voltage		V_{DS}	500		V
Gate-source Voltage		V_{GS}	±30		V
Continuous Drain Current (1)	T_C=25°C	I_D	5		A
	T_C=100°C		3		A
Pulsed Drain Current(2)		I_{DM}	20		A
Total Power Dissipation (3)		P_D @ T_C=25°C	76		W
		Derating Factor above 25°C	0.61		W/°C
Thermal Resistance Junction-to-Case (3)		$R_{\theta JC}$	1.65		°C/W
Junction and Storage Temperature Range		T_J,T_{STG}	-55 to +150		°C

Electrical Characteristics (T_C=25 ℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	500			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=500V,V_{GS}=0V,T_C=25°C			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±30V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2.0		4.0	V
Static Drain-Source on-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=2.5A		1.2	1.5	Ω
Diode Forward Voltage	V_{SD}	I_S=5A,V_{GS}=0V		0.9	1.2	V
Maximum Body-Diode Continuous Current	I_S				5	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V,f=1MHz		490		pF
Output Capacitance	C_{oss}			60		
Reverse Transfer Capacitance	C_{rss}			8		
Switching Parameters						
Total Gate Charge	Q_g	V_{DS}=400V,I_D=5A,V_{GS}=10V		17		nC
Gate Source Charge	Q_{gs}			2.1		
Gate Drain Charge	Q_{gd}			8.3		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=50V, I_D=5A,R_{GEN}=10Ω		8		ns
Turn-on Rise Time	t_r			11		
Turn-off Delay Time	$t_{D(off)}$			18.8		
Turn-off Fall Time	t_f			13.5		
Reverse Recovery Time	trr	V_R=400V,I_F=5A, di/dt=100A/μs		328		ns
Reverse Recovery Charge	Qrr			1.6		μC

Noted: (1) Pulse Test: Pulse Width≤300us,Duty cycle ≤2%
(2) Pulse width limited by maximum junction temperature
(3) Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. With 2oz Copper, t≤10s

Typical Performance Characteristics

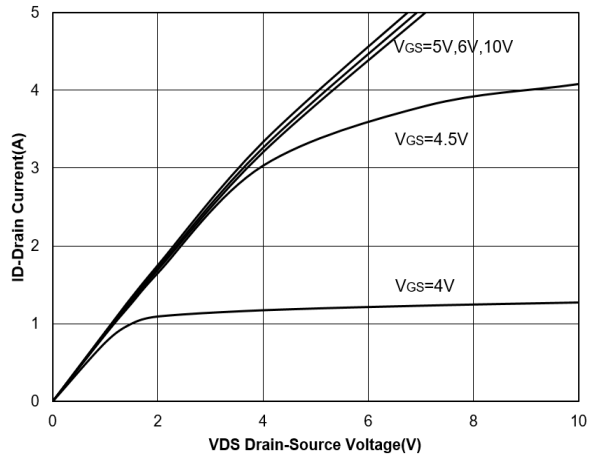


Figure 1. Output Characteristics

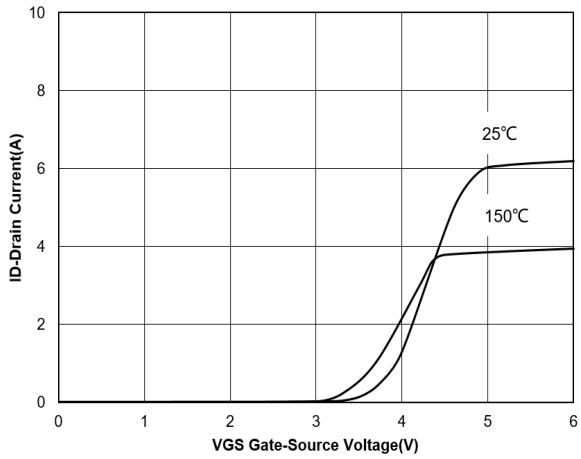


Figure 2. Transfer Characteristics

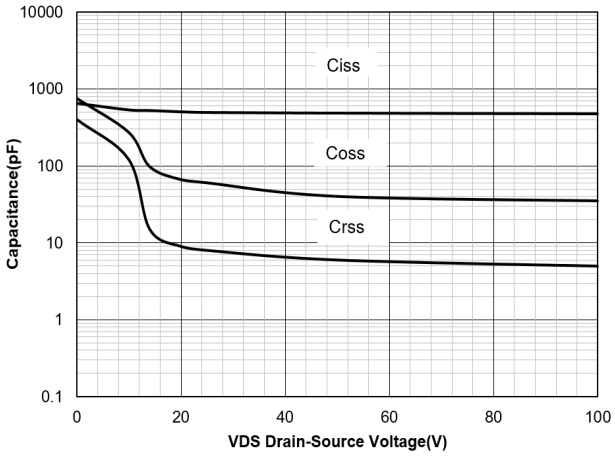


Figure 3. Capacitance Characteristics

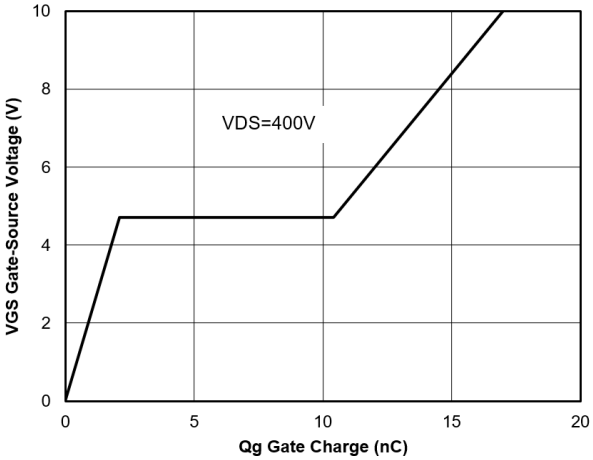


Figure 4. Gate Charge

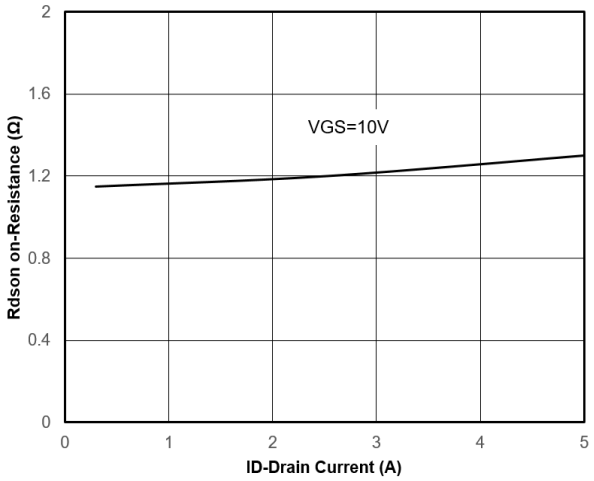


Figure 5. Drain-Source on Resistance

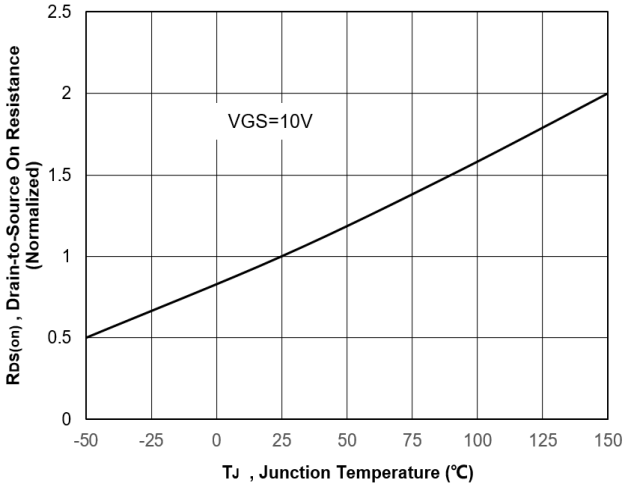


Figure 6. Normalized On-Resistance Vs. Temperature

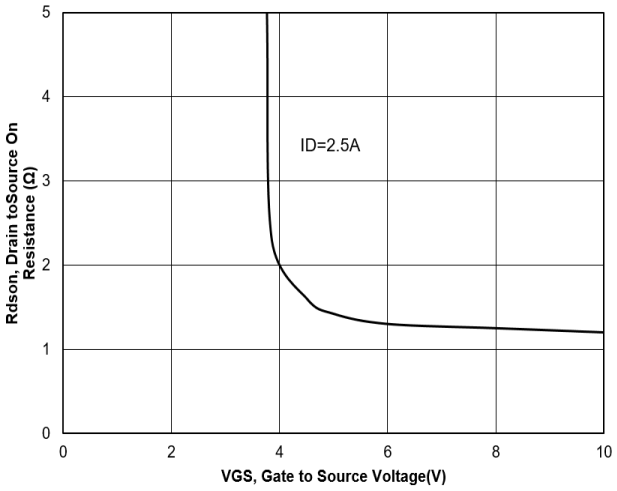


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

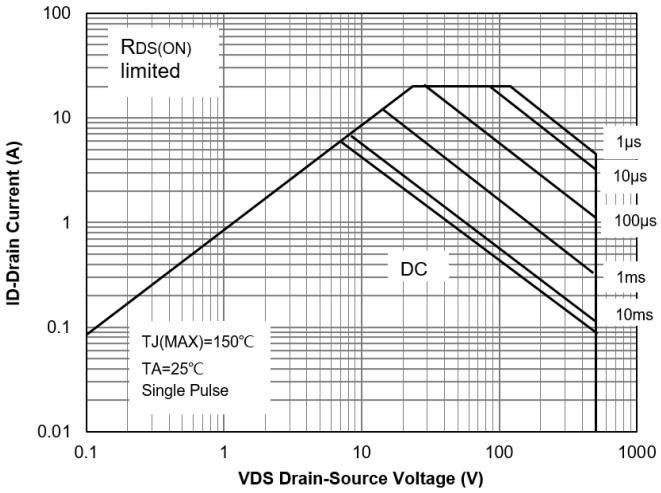


Figure 8. Safe Operation Area

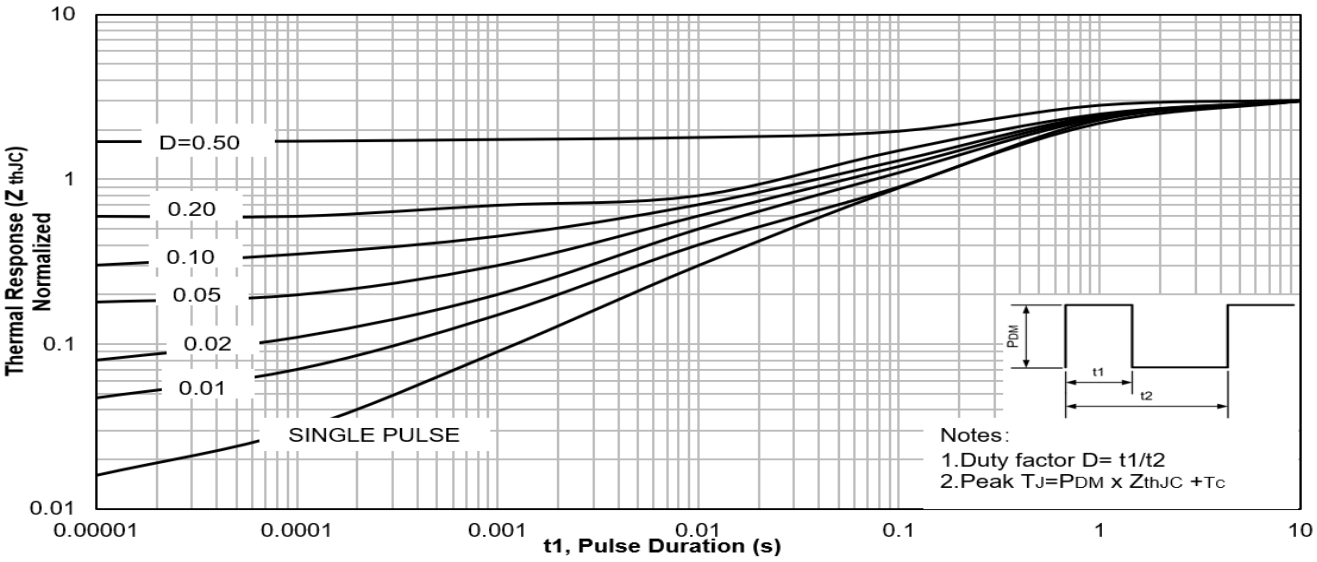


Figure 9. Maximum Effective Transient Thermal Impedance ,Junction-to-Case

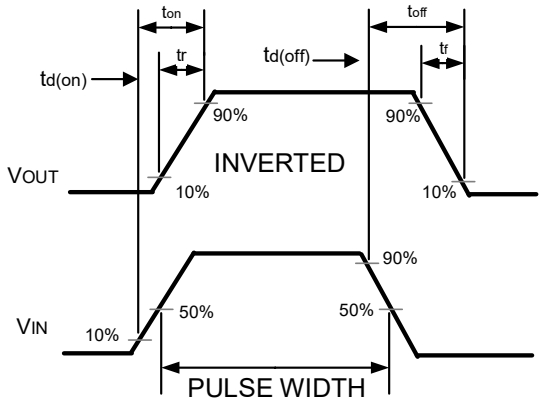
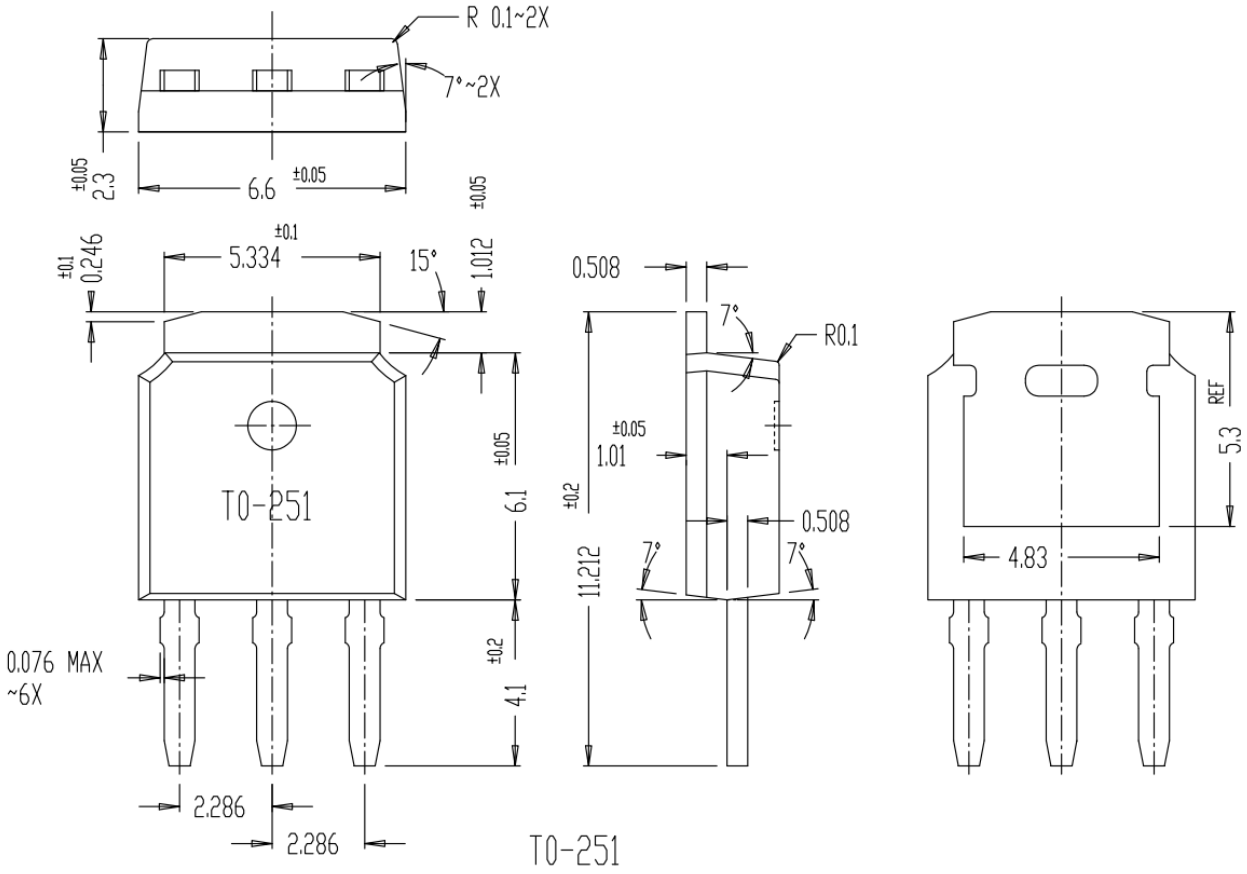
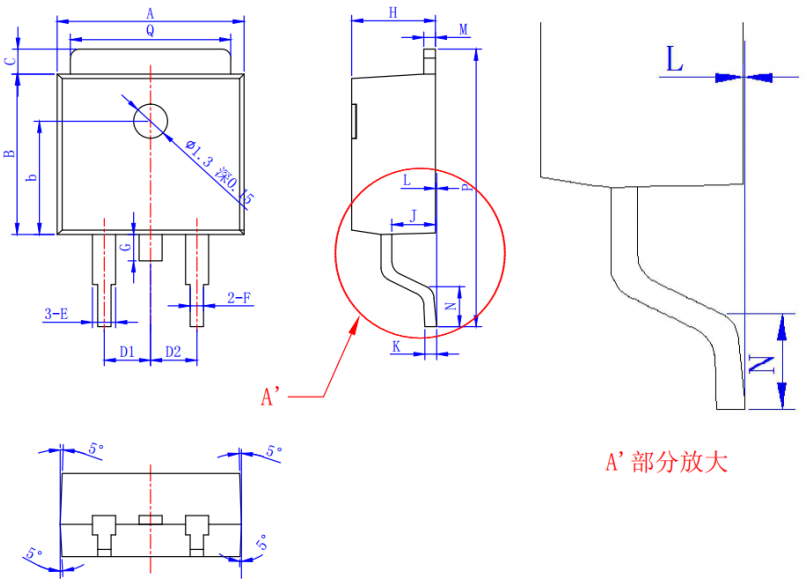


Figure 10. Switching wave

TO-251 Package Outline Drawing



TO-252 Package Outline Drawing



Symbol	MM		
	Min	Nom	Max
A	6.30	6.55	6.90
B	5.90	6.10	6.30
b	4.10	4.30	4.50
C	0.90	1.00	1.10
D1		2.29BSC	
D2		2.29BSC	
E	0.61	0.76	0.91
F	0.50	0.60	0.70
G	0.60	0.80	1.00
H	2.10	2.30	2.50
J	0.90	1.00	1.10
K	0.40	0.50	0.60
L	0.00	0.05	0.127
M	0.45	0.50	0.55
N	1.39	—	1.77
P	9.60	9.90	10.30
Q	5.10	5.30	5.50

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