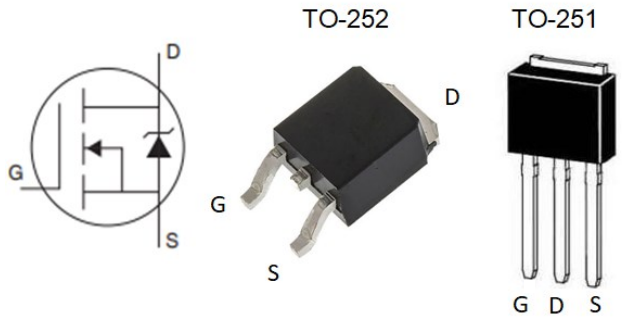
Description

The CM04N80AU/D is the N-Channel enhancement mode power field effect transistors with high cell density, high voltage planar technology. This high density process and design have been optimized switching performance and especially tailored to minimize on-state resistance.

Features

- V_{DS}: 800V
- I_D (@V_{GS}=10V): 3.7A
- RDS_{ON} (@V_{GS}=10V) : < 3.8Ω
- High density cell design for extremely low RDS_{ON}
- Excellent on-resistance and DC current capability

Equivalent Circuit and Pin Configuration



Applications

- AC/DC load switch
- SMPS
- Notebooks and Handhelds adapter
- UPS Power

Marking Information

X = Package type

XXXX = Date Code

Ordering Information

P/N	Package Type	Packaging	Remark
CM04N80AU	TO-252	Tape and reel	ROHS
CM04N80AD	TO-251	Tube	ROHS

Absolute Maximum Ratings (T_C=25 ℃ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	800	V
Gate-source Voltage		V_{GS}	±20	V
Continuous Drain Current [1]	T_C=25°C	I_D	3.7[4]	A
	T_C=100°C		3[4]	A
Pulsed Drain Current[2]		I_{DM}	14.8[4]	A
Total Power Dissipation [3]		P_D @ T_C=25°C	100	W
		Derating Factor above 25°C	0.8	W/°C
Thermal Resistance Junction-to-Case [3]		$R_{\theta JC}$	1.25	°C/W
Junction and Storage Temperature Range		T_J,T_{STG}	-55 to +150	°C

Electrical Characteristics (T_C=25 ℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250μA	800			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=800V,V_{GS}=0V,T_C=25°C			2	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	3.0		5.0	V
Static Drain-Source on-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=2A		3.2	3.8	Ω
Diode Forward Voltage	V_{SD}	I_S=3.7A,V_{GS}=0V			1.2	V
Maximum Body-Diode Continuous Current	I_S				3.7	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V,f=1.0MHz		780		pF
Output Capacitance	C_{oss}			58		
Reverse Transfer Capacitance	C_{rss}			5		
Switching Parameters						
Total Gate Charge	Q_g	V_{DS}=640V,I_D=3.7A,V_{GS}=10V		23		nC
Gate Source Charge	Q_{gs}			5		
Gate Drain Charge	Q_{gd}			14		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=50V, I_D=3A,R_{GEN}=25Ω		62		ns
Turn-on Rise Time	t_r			37.2		
Turn-off Delay Time	$t_{D(off)}$			48		
Turn-off Fall Time	t_f			21		

Noted: (1) Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

(2) Pulse width limited by maximum junction temperature

(3) Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch. With 2oz Copper, t≤10s

(4) Drain current limited by maximum junction temperature

Typical Performance Characteristics

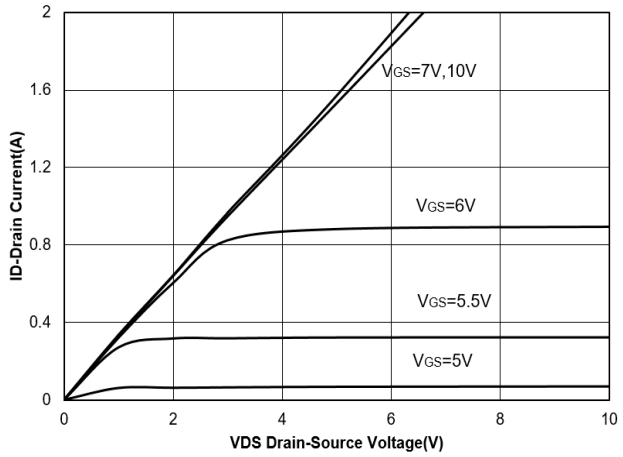


Figure 1. Output Characteristics

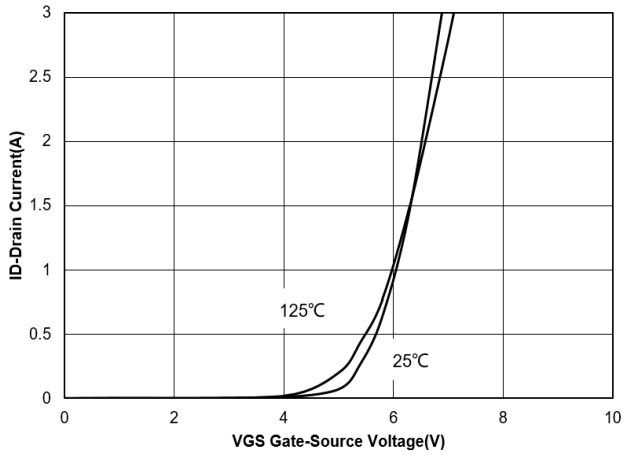


Figure 2. Transfer Characteristics

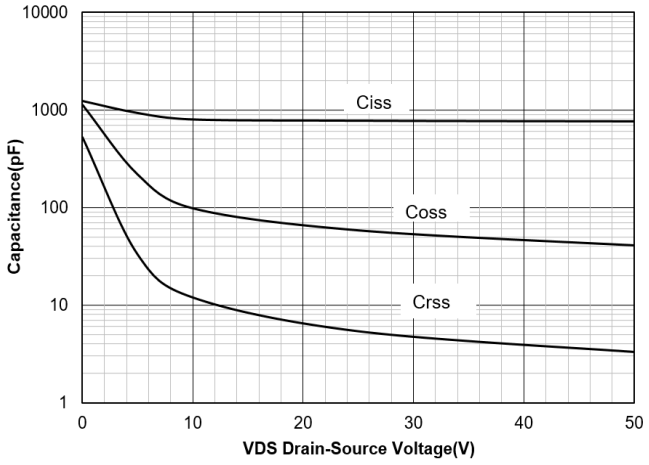


Figure 3. Capacitance Characteristics

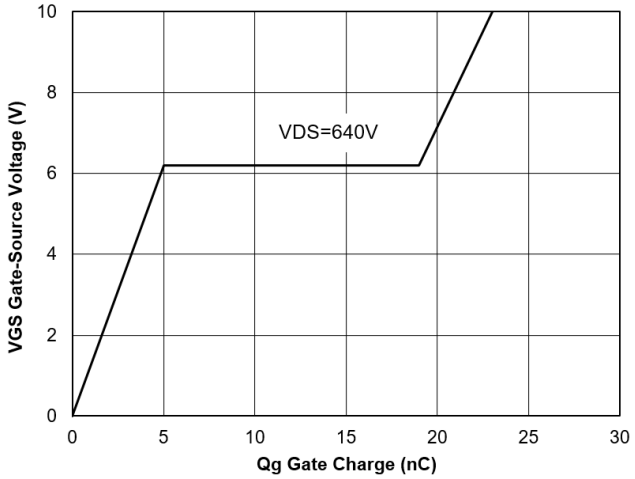


Figure 4. Gate Charge

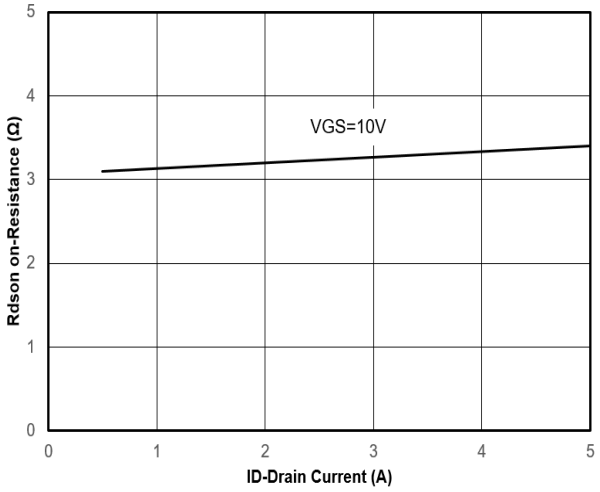


Figure 5. Drain-Source on Resistance

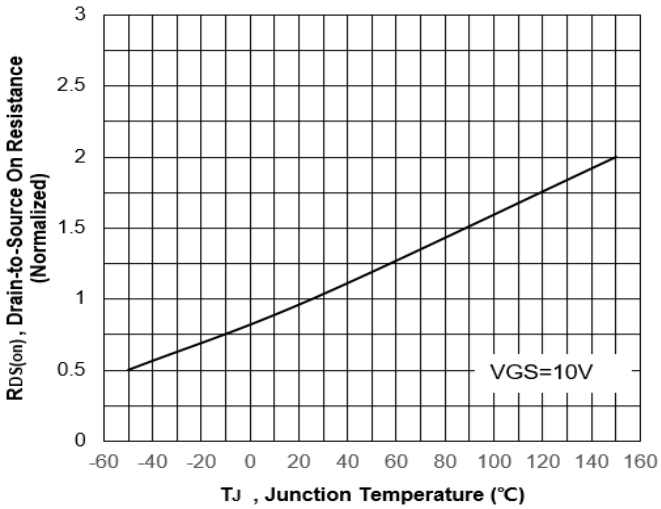


Figure 6. Normalized On-Resistance Vs. Temperature

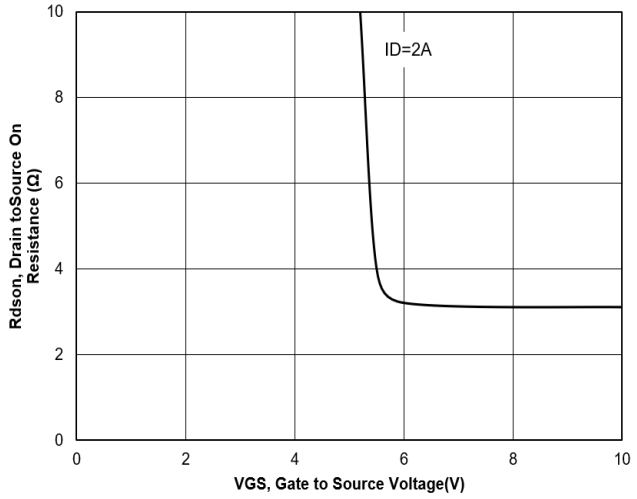


Figure 7. Typical Drain to Source ON Resistance VS Gate Voltage and Drain Current

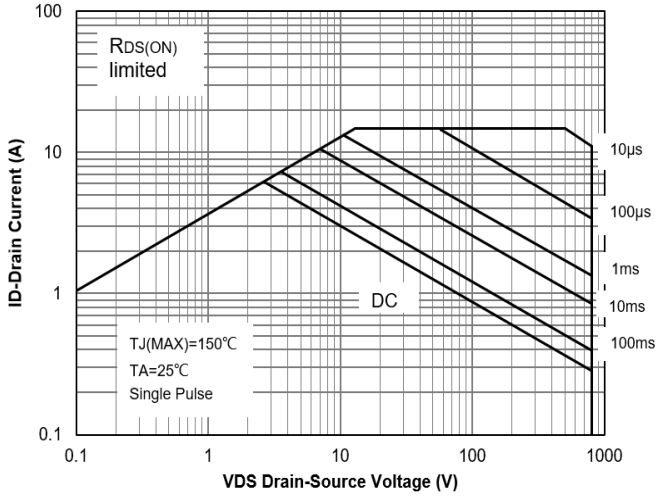


Figure 8. Safe Operation Area

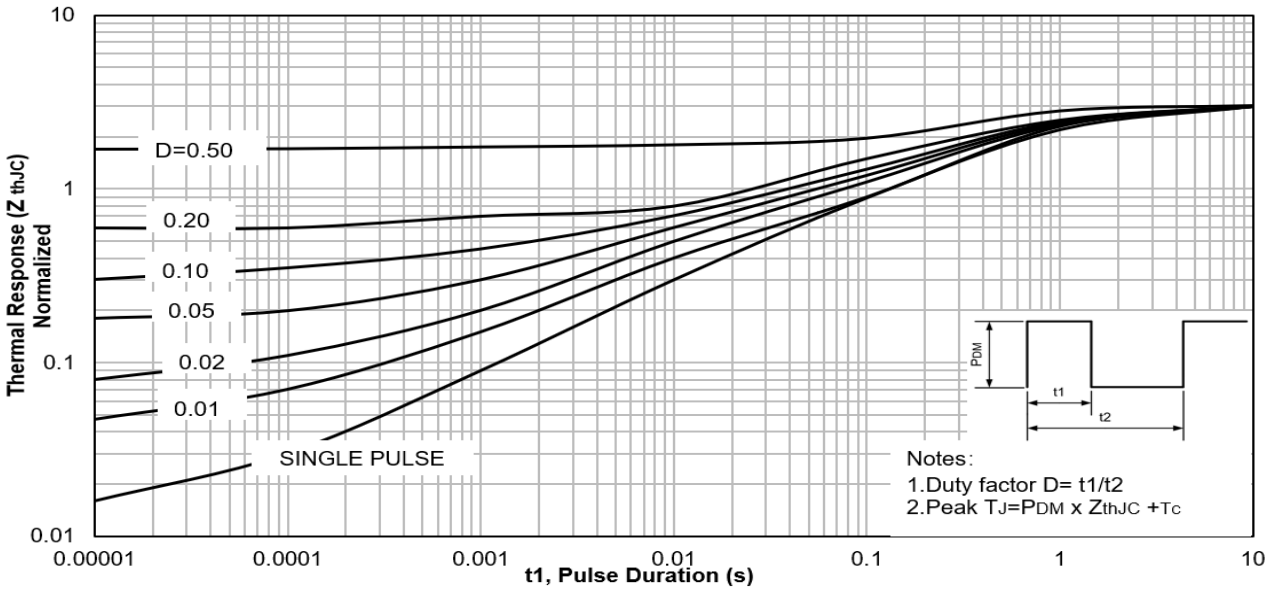


Figure 9. Maximum Effective Transient Thermal Impedance ,Junction-to-Case

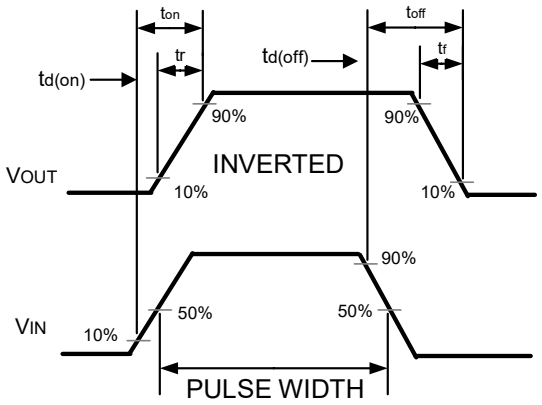
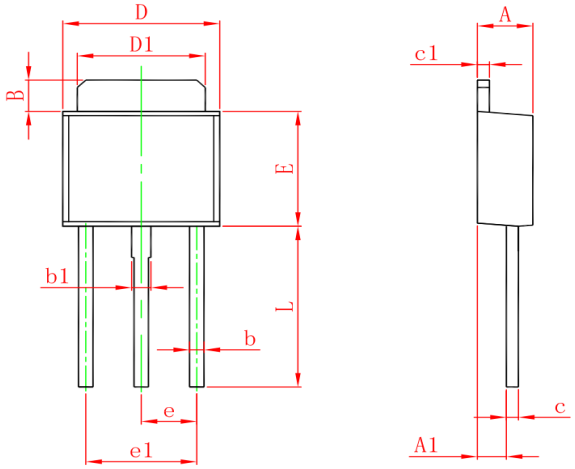


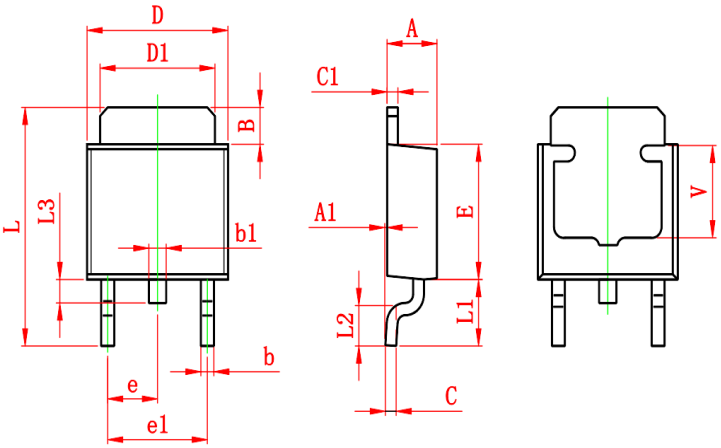
Figure 10. Switching wave

TO-251 Package Outline Drawing



Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	1.050	1.350	0.042	0.054
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP.		0.091 TYP.	
e1	4.500	4.700	0.177	0.185
L	7.500	7.900	0.295	0.311

TO-252 Package Outline Drawing



Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP.		0.091 TYP.	
e1	4.500	4.700	0.177	0.185
L	9.500	9.900	0.374	0.390
L1	2.550	2.900	0.100	0.114
L2	1.400	1.780	0.055	0.070
L3	0.600	0.900	0.024	0.035
V	3.800 REF.		0.150 REF.	

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