Description

The AR7061P1 is a Bi-directional TVS diode, utilizing leading monolithic silicon technology to provide fast response time and low ESD clamping voltage, making this device an ideal solution for protecting voltage sensitive high-speed data lines. The AR7061P1 complies with the IEC 61000-4-2 (ESD) with ±10kV air and ±10kV contact discharge. The small size, low capacitance and high ESD surge protection make AR7061P1 an ideal choice to protect cell phone, digital video interfaces and other high speed ports.

Features

- Ultra low leakage: nA level
- Operating voltage: 70V
- Low clamping voltage
- Complies with following standards:
  - IEC 61000-4-2 (ESD) immunity test
    - Air discharge: ±10kV
    - Contact discharge: ±10kV
- RoHS Compliant

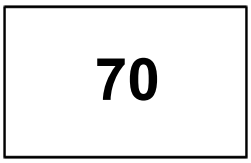
Mechanical Characteristics

- Package: DFN1006-2
- Case Material: “Green” Molding Compound.
- Terminal Connections: See Diagram Below
- Marking Information: See Below

Applications

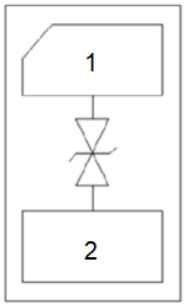
- Cellular Handsets and Accessories
- Display Ports
- MDDI Ports
- USB Ports
- Digital Visual Interface (DVI)
- PCI Express and Serial SATA Ports

Marking Information



70 = Device Marking Code

Equivalent Circuit and Pin Configuration



Circuit and Pin Schematic

Ordering Information

Part Number	Packaging	Reel Size
AR7061P1	10000/Tape & Reel	7 inch

Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

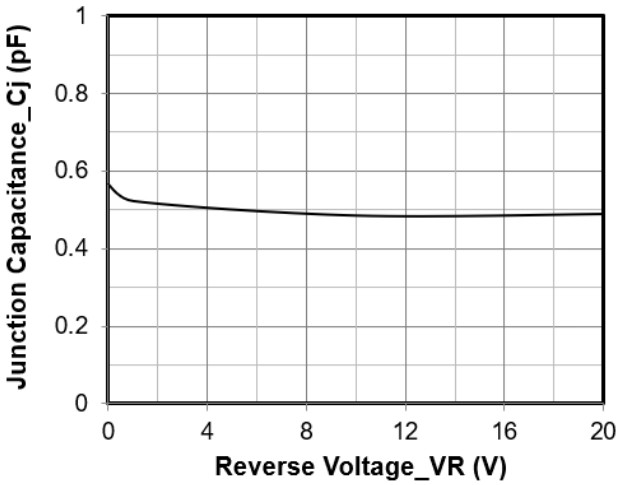
Parameter	Symbol	Value	Unit
ESD per IEC 61000−4−2 (Air) ESD per IEC 61000−4−2 (Contact)	V_{ESD}	±10 ±10	kV
Operating Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	Tstg	−55 to +150	°C

Electrical Characteristics (T_A=25°C unless otherwise specified)

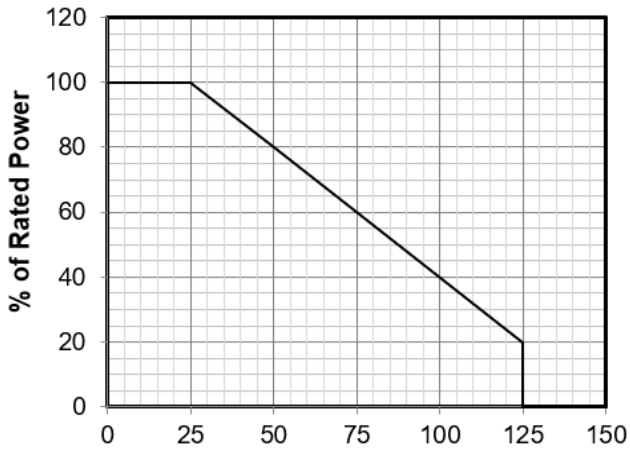
Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	V_{RWM}			70	V	
Breakdown Voltage	V_{BR}	80			V	I_T = 1mA
Reverse Leakage Current	I_R			0.5	μA	V_{RWM} = 70V
ESD Clamping Voltage(1)	V_C		75		V	I_{PP} = 4A, tp = 0.2/100ns (TLP)
ESD Clamping Voltage(1)	V_C		100		V	I_{PP} = 16A, tp = 0.2/100ns (TLP)
Junction Capacitance	C_J		0.6		pF	VR = 0V, f = 1MHz

(1) Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns.

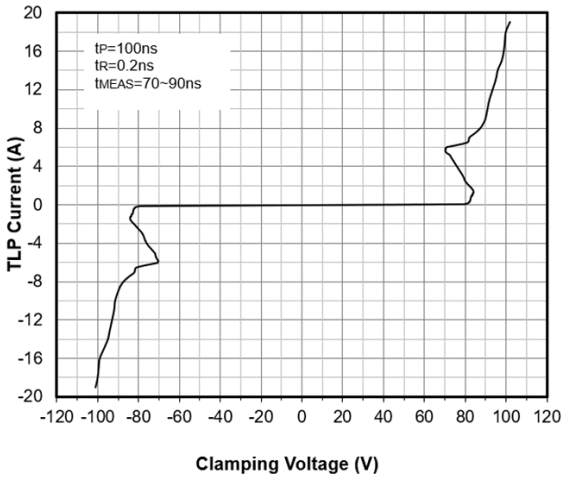
Typical Performance Characteristics (TA=25°C unless otherwise Specified)



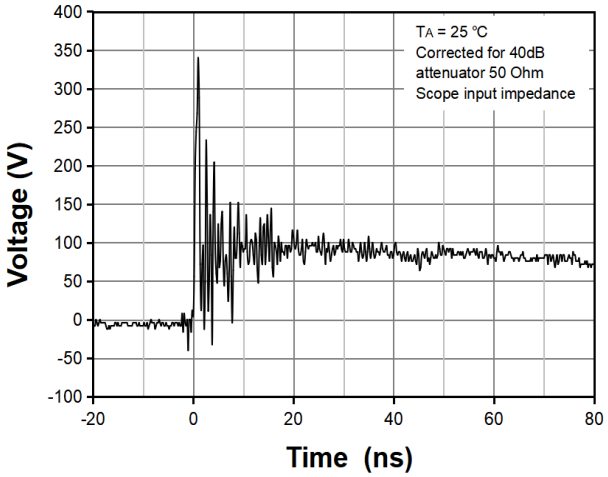
Junction Capacitance vs. Reverse Voltage



Peak Pulse Power vs. Pulse Time



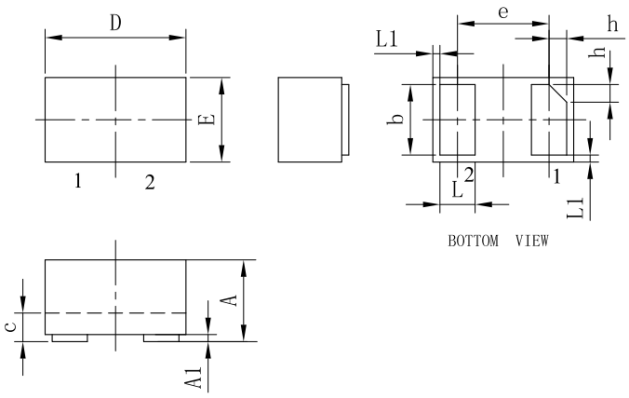
TLP Measurement



ESD Clamping Voltage

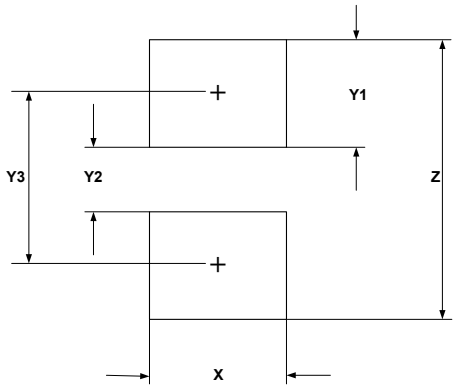
8 kV Contact per IEC61000−4−2

DFN1006-2 Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.45	0.50	0.55	0.018	0.020	0.022
c	0.12	0.15	0.18	0.005	0.006	0.007
D	0.95	1.00	1.05	0.037	0.039	0.041
e	0.65 BSC			0.026 BSC		
E	0.55	0.60	0.65	0.022	0.024	0.026
L	0.20	0.25	0.30	0.008	0.010	0.012
L1	0.05REF			0.002REF		
h	0.07	0.12	0.17	0.003	0.005	0.007

Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
X	0.60	0.024
Y1	0.50	0.020
Y2	0.30	0.012
Y3	0.80	0.032
Z	1.30	0.052

Contact Information

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