Description

The APO2003DF provides robust protection for load and source during overvoltage and overcurrent events. The device continuously monitors the input voltage, the input current, and environmental temperature. In the event that an incorrect voltage is applied at input, the output will clamp to 5.5V to protect the load. If the input voltage exceeds over-voltage threshold, the device disconnects the load to prevent damage to the device and/or load. In the case of an overcurrent condition, it limits the system current at the threshold value, and if the overcurrent persists, switches off the pass FET after blanking time. Both input over-voltage and input overcurrent threshold are user-programmable. The device also monitors environmental temperature with Negative Temperature Coefficient (NTC) thermistor as well as die temperature, and switches off when either of them exceeds pre-determined threshold. When the device is controlled by a processor, the status information about fault conditions can be provided to the host.

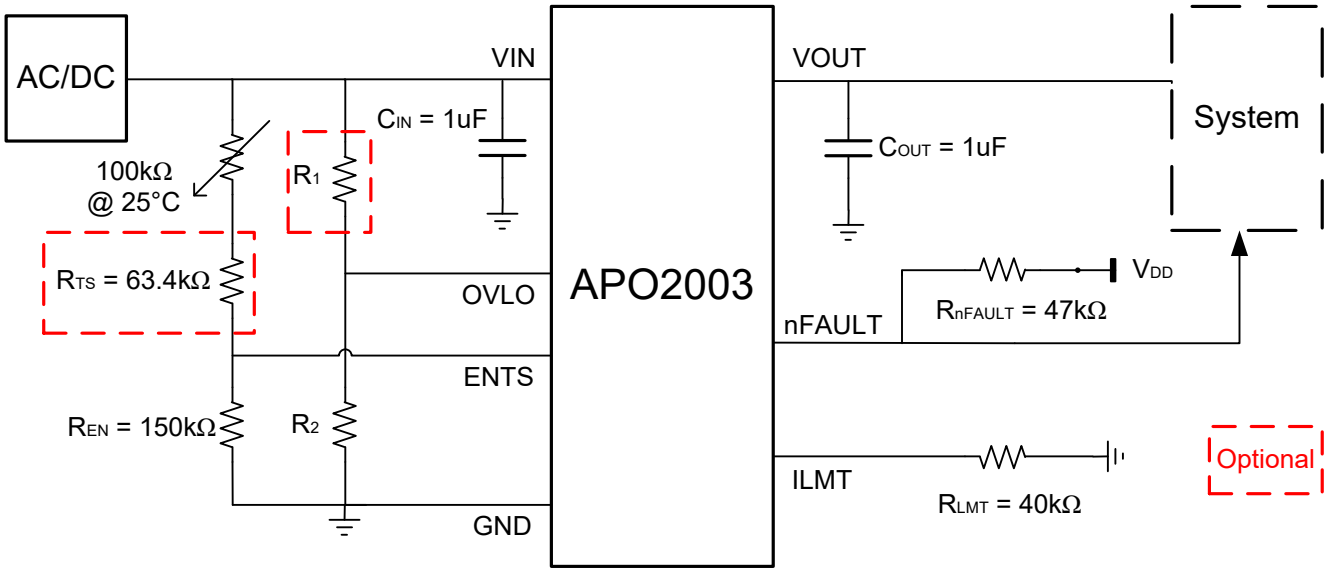
Applications

- E-cigarette
- Mobile Handsets
- Tablets
- Wearable Devices
- Charging Ports

Features

- Environmental temperature sense with NTC thermistor
- Input overvoltage with user-programmable threshold
- Output voltage clamp
- Input current clamp with user-programmable threshold
- 28V maximum input voltage
- 2.5A maximum continuous input current
- OTG functionality from VOUT to VIN
- Enable control
- Under voltage lockout
- Output short-circuit protection
- Thermal shutdown
- Fault status indication
- Very low shut-down and stand-by current
- -40°C ~ 125°C operating junction temperature
- RoHS compliant and Lead(Pb)-free DFN2x2-8L package

Typical Application Circuit



Package and Order Information

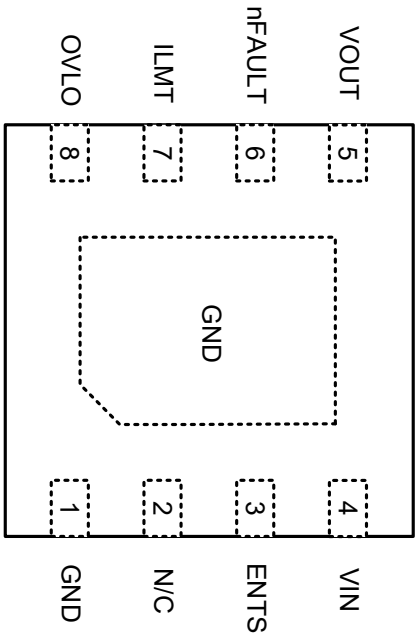
Part number	Package Description	Temperature Range	Packaging Option	Marking Information
APO2003DF	DFN-2x2-8L	-40°C ~ 125°C	3000/Tape & Reel	2003XXXX

Pin Assignments

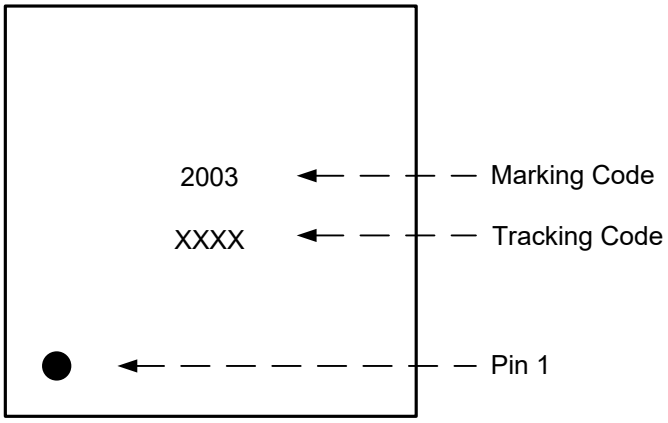
Pin	Name	I/O (1)	Description
4	VIN	P	Input power, connect to external DC supply. Connect minimum 1μF ceramic capacitor to ground.
3	ENTS	DI / AI	Chip enable input. Active high. Also serve as ambient temperature qualification voltage input. Program temperature threshold with a NTC thermistor from VIN to ENTS, and a resistor from ENTS to GND. Switch shuts off when ENTS pin is out of range. Recommend 104AT-2 thermistor.
8	OVLO	AI	OVP threshold adjustment. Connect a resistor-divider to set a threshold between 4V and 16V. Internal OVP threshold is used if OVLO < 0.5V.
7	ILMT	AI	Input overcurrent threshold programming. Connect a resistor to ground to set the overcurrent threshold.
6	nFAULT	DO	Open-drain output device status. nFAULT = Low indicates that the pass FET has been turned off due to input overvoltage, input overcurrent, or thermal shutdown.
1	GND	G	Ground.
2	N/C	N/A	No connection.
5	VOUT	P	Output terminal to the charging system. Connect minimum 1μF ceramic capacitor to ground.
9	Exposed Pad	P	The exposed thermal pad is internally connected to the AGND pin. The thermal pad must be connected to the same potential as the AGND pin on the printed PCB. Do not use the thermal pad as the primary ground input for the device.

(1) DI - Digital Input, DI - Digital Input, AI - Analog Input, AO - Analog Output, P - Power, G - Ground

Pin Configuration and Top Mark

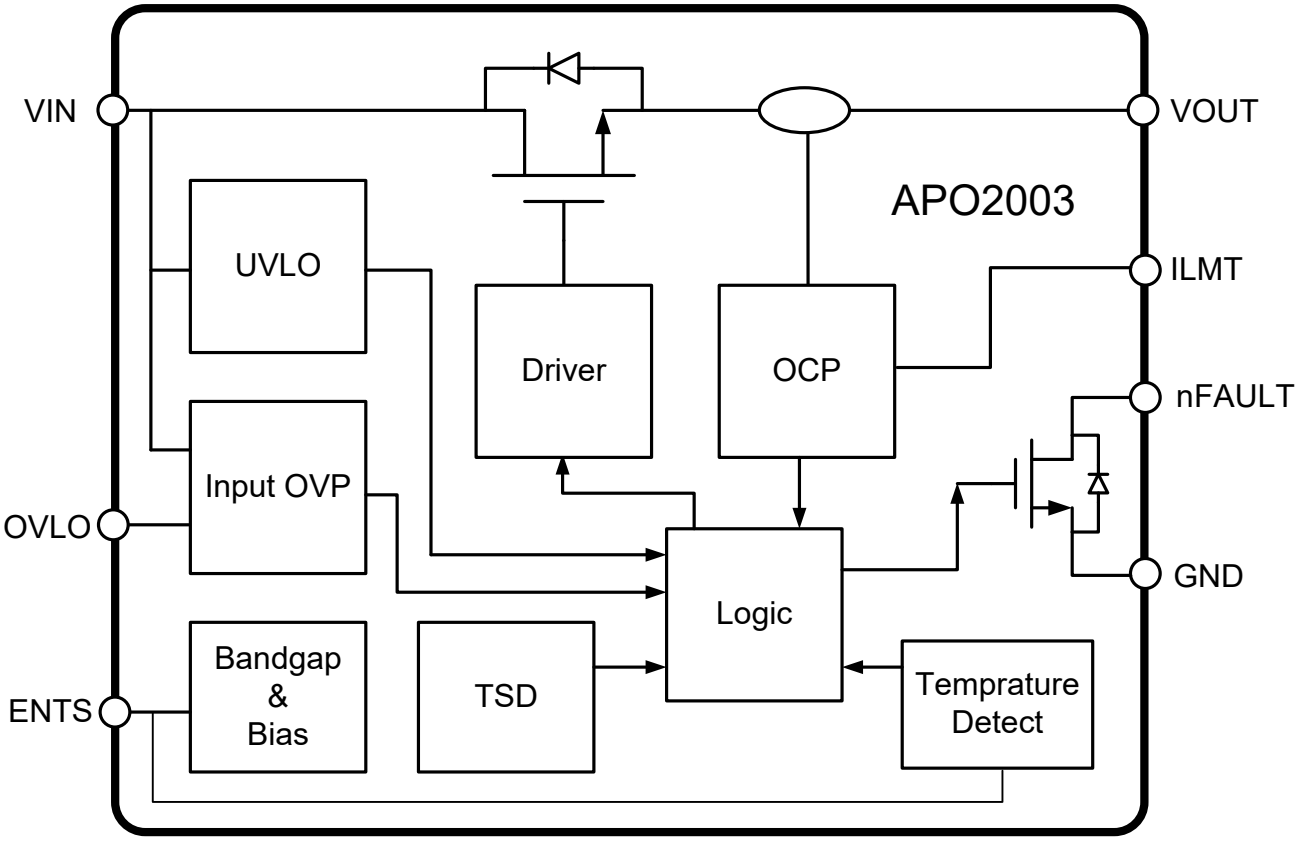


Top View



Top Mark

Operational Diagram



Absolute Maximum Ratings (2) (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Min	Max	Unit
Input DC voltage	V_{IN}	-0.3	28	V
Output voltage	V_{OUT}	-0.3	15	V
ENTS, ILMT, OVLO, nFAULT voltage	V_{LV}	-0.3	6	V
Ambient temperature	T_A	-40	85	°C
Continuous output current	I_{OUT}	Thermally Limited		A
Junction temperature	T_J	-40	150	°C
Storage temperature	T_{STG}	-55	150	°C
Soldering temperature (At leads，10 seconds)	T_{LEAD}		260	°C

(2) Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

ESD & Latch-up

Parameter	Symbol	Min	Max	Unit
Human Body Model	V_{HBM}	-4	4	kV
Charged Device Model	V_{CDM}	-1	1	kV
Latch-up	$I_{Latch-up}$	-200	200	mA

Thermal Information (3)

Parameter	Symbol	Value	Unit
Thermal resistance from junction to ambient (In free air)	$R_{\Theta JA}$	150	°C/W

(3) Thermal resistance from junction to ambient is highly dependent on PCB layout.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Input DC voltage	V_{IN}	2.8	5.5	V
Output voltage	V_{OUT}	0	5.5	V
ENTS, ILMT, OVLO, nFAULT voltage	V_{LV}	0	5	V
Current limit resistor	R_{LMT}	40		kΩ
Fault resistor	R_{nFAULT}	10		kΩ
Junction temperature	T_J	-40	125	°C

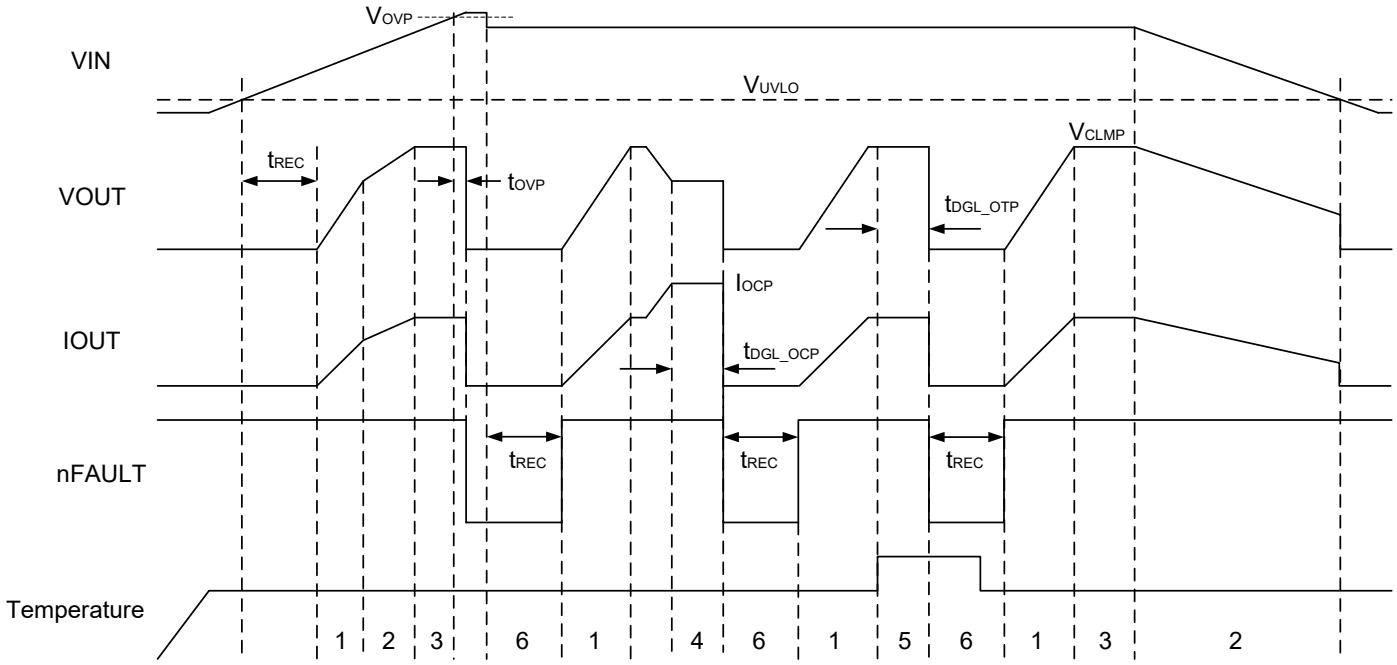
Electrical Characteristics (V_{IN} = 5V, C_{IN} = 1μF, C_{OUT} = 1μF, R_{ILMT} = 40kΩ, R_1 = Open, R_2 = Short, R_{nFAULT} = 47kΩ, R_{EN} = 150kΩ, R_{TS} = 63.4kΩ, NTC Thermistor = 100kΩ, T_A = 25°C, unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Input						
V_{UVLO}	Input voltage UVLO on rising		2.4	2.7	2.9	V
V_{UVLO_HYS}	Input voltage UVLO hysteresis			0.2		V
I_{MAX}	MAX continuous output current				2.5	A
I_{OFF}	Shutdown current	V_{ENTS} = 0V		3	5	uA
I_{ON}	Quiescent current	V_{ENTS} = 1.2V, I_{OUT} = 0A		120	145	uA
Input Overvoltage Protection (OVP)						
V_{CLMP}	Output clamp voltage	5.5V < V_{IN} < V_{OVP}	5	5.5	5.7	V
V_{OVP_INT}	Internal OVP threshold		6.45	6.65	6.85	V
V_{OVP_HYS}	Internal OVP hysteresis			0.15		V
V_{OVLO_SEL}	External OVP select threshold		0.4	0.5	0.6	V
V_{OVLO_TH}	External OVP set threshold		1.1	1.2	1.3	V
V_{OVLO_RNG}	OVP set range		4		10	V

Electrical Characteristics (Continued)

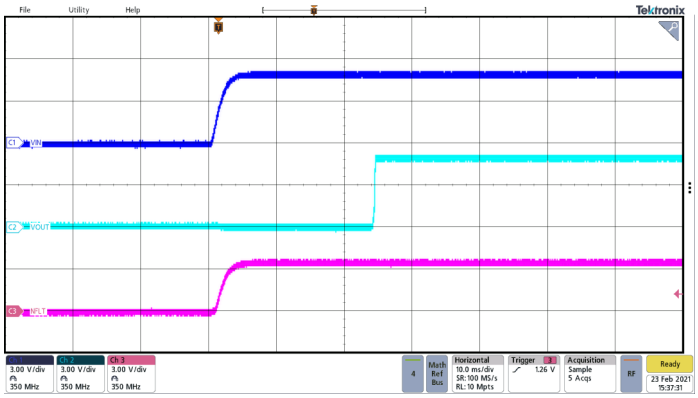
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Timing						
t_{OVP}	OVP propagation delay	V_{IN} rises at 10V/uS		45		nS
t_{REC}	Recovery delay from UVLO, OVP, ILMT, TSD			20		mS
Current Limit Protection (ILMT)						
K	I_{OCP} = K / R_{LMT}	R_{LMT} = 200kΩ	79	93	107	A·kΩ
t_{DGL_OCP}	Deglitch time on I_{OCP}			360		uS
Thermal Protection						
T_{OTP}	Over temperature protection			71		°C
	NTC trip point	V_{ENTS} / V_{IN}	64.3	65.7	67.1	%
t_{DGL_OTP}	Deglitch time on OTP			310		uS
T_{TSD}	Thermal shutdown temperature			125		°C
T_{TSD_HYS}	Thermal shutdown hysteresis			15		°C
MOSFET						
R_{ON}	ON resistance		52	60	78	mΩ
V_{BR}	Breakdown voltage		28			V
Logic Input (ENTS)						
V_{IH}	ENTS high input voltage		1.2			V
V_{IL}	ENTS low input voltage				0.4	V
Logic Output (nFAULT)						
V_{OL}	nFAULT pull-down voltage	I_{nFAULT} = 1mA		150		mV
I_{HI_Z}	Leakage current, nFAULT HI-Z	V_{nFAULT} = 5V			1	uA

Timing Diagram

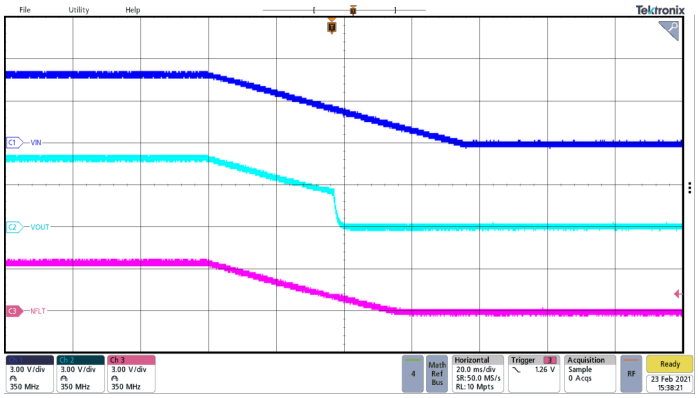


1. Normal start-up
2. V_{UVLO} < VIN < V_{CLMP}, VOUT tracks VIN
3. Input overvoltage
4. Input current limit
5. Thermal protection
6. Stand-by

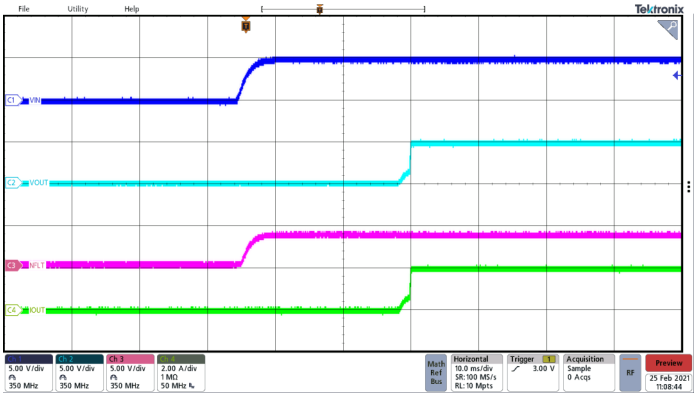
Typical Performance Characteristics (V_{IN} = 5V, C_{IN} = 1μF, C_{OUT} = 1μF, R_{ILMT} = 40kΩ, R_1 = Open, R_2 = Short, R_{nFAULT} = 47kΩ, R_{EN} = 150kΩ, R_{TS} = 63.4kΩ, 104AT-2, T_A = 25°C, unless otherwise specified)



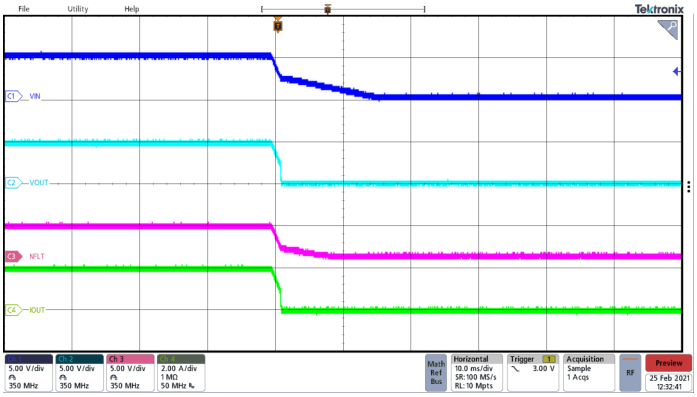
UVLO rising



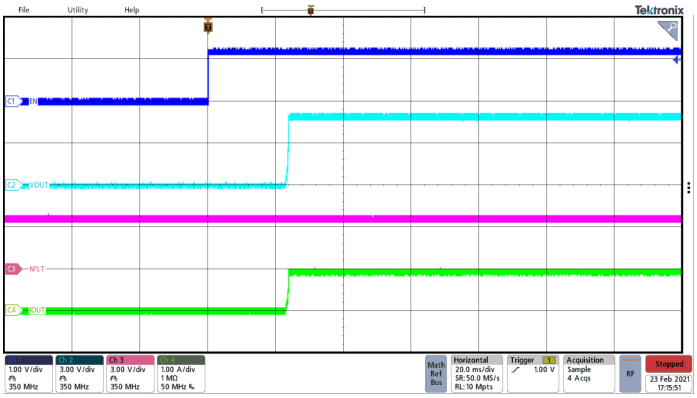
UVLO falling



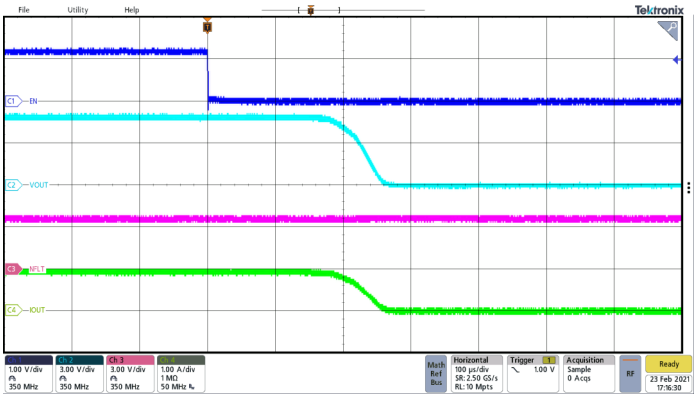
Power on with 2.5Ω Load



Power OFF with 2.5Ω Load

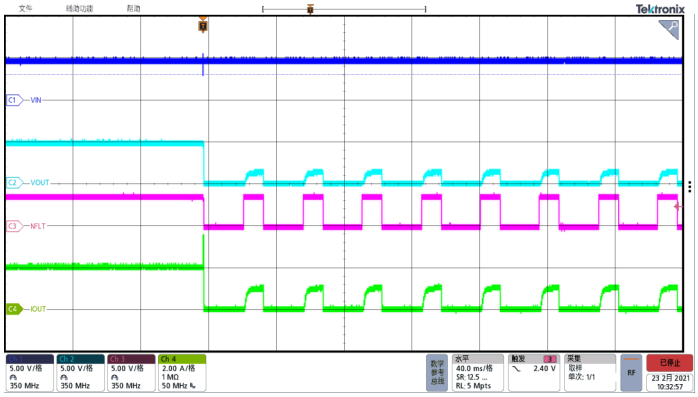


EN ON with 5Ω Load

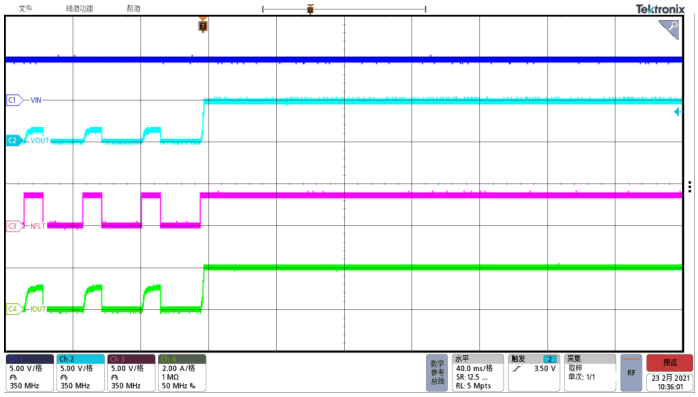


EN OFF with 5Ω Load

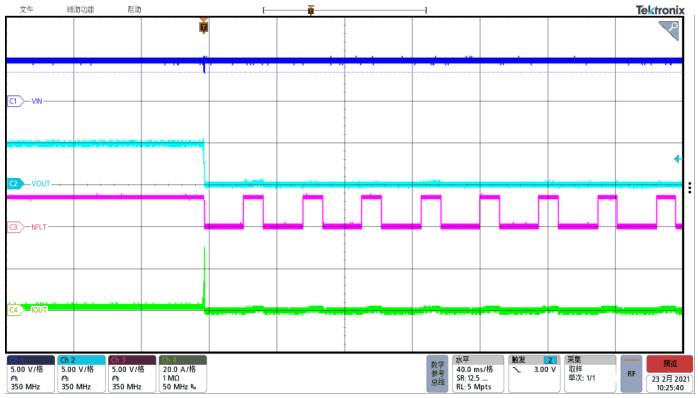
Typical Performance Characteristics (Continued)



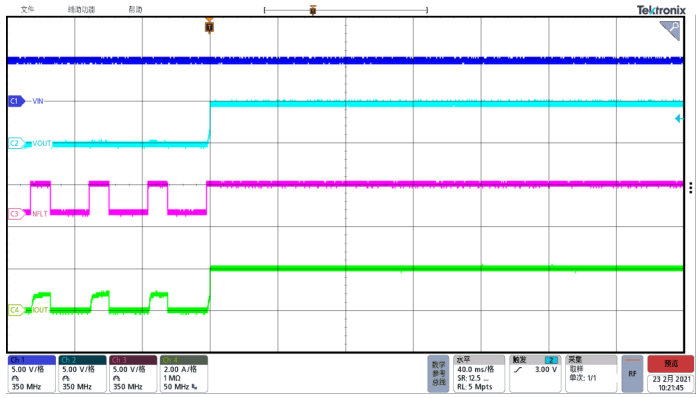
Output over current protection from 2A load



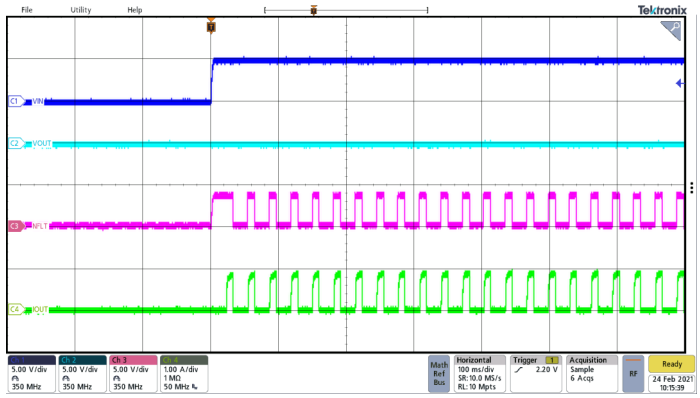
Recovery from Output over current protection



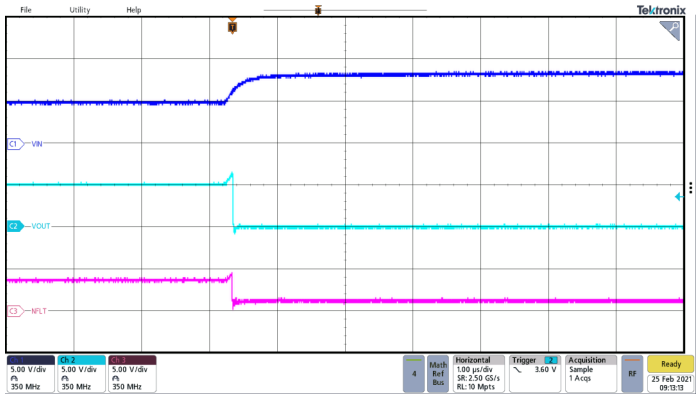
output short circuit with 2.5Ω load



output short circuit recovery with 2.5Ω load

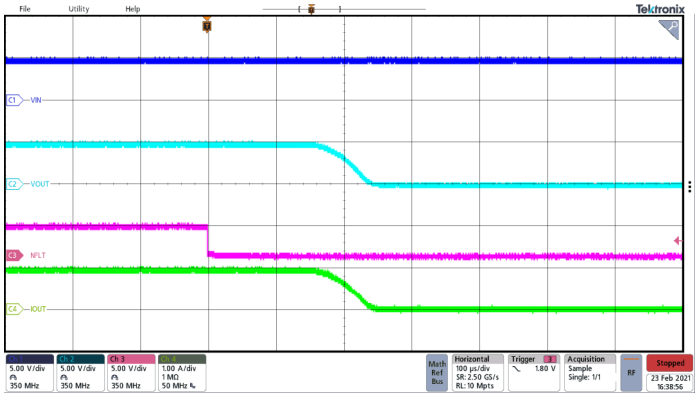


power up with output short circuit

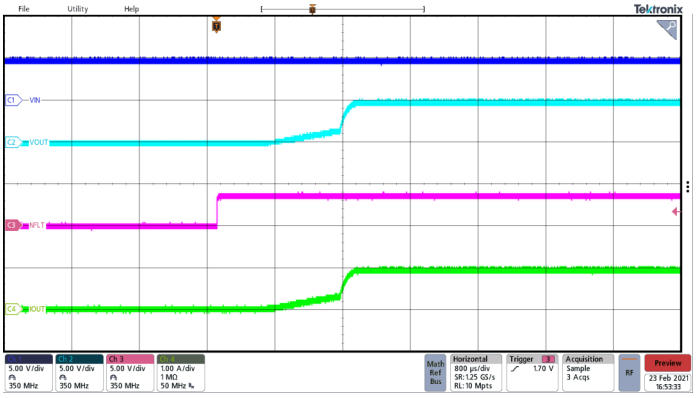


OVP Response

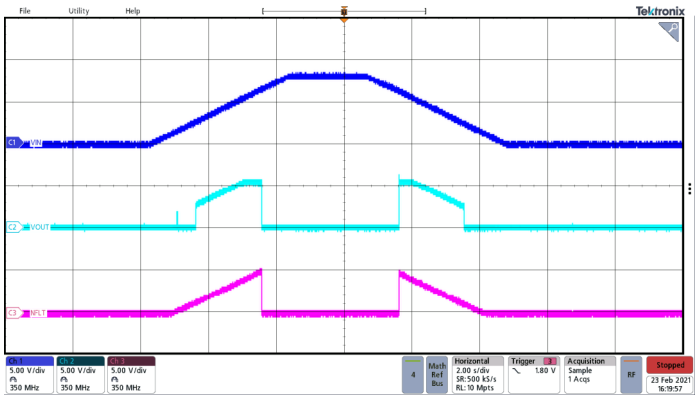
Typical Performance Characteristics (Continued)



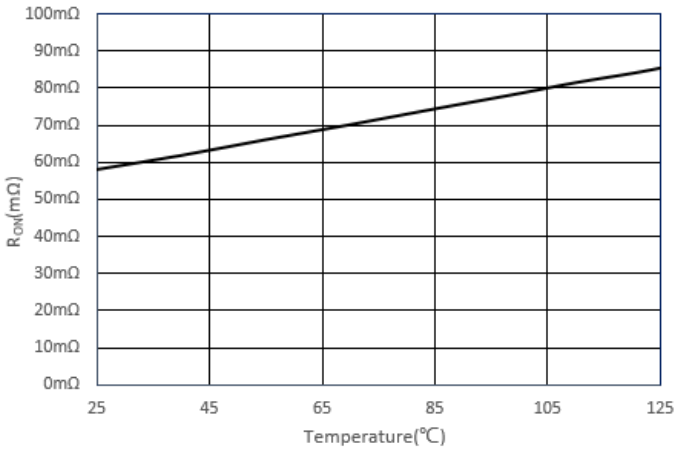
External NTC OTP response with 5Ω Load



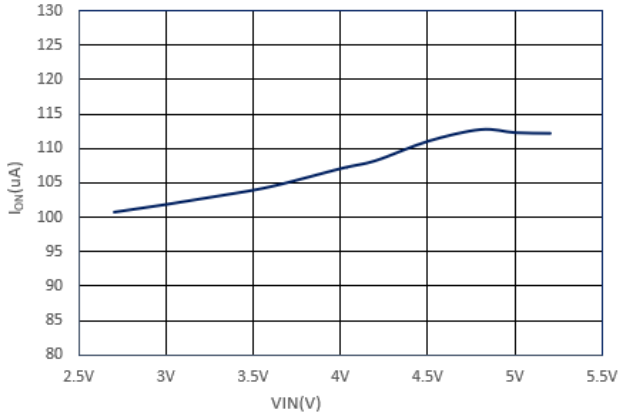
External NTC OTP recovery with 5Ω Load



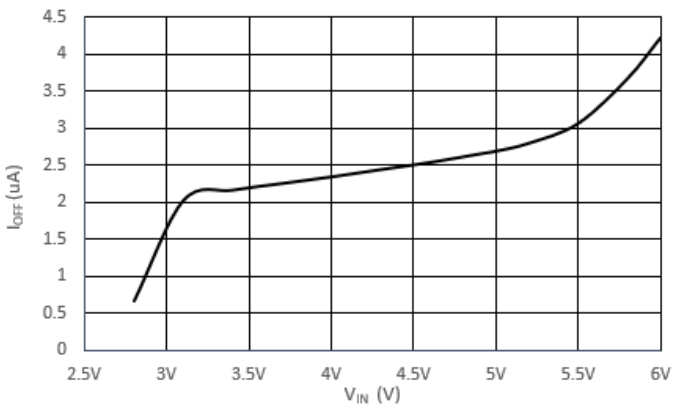
Output Clamp as Input Ramps up



R_{ON} vs. Temperature

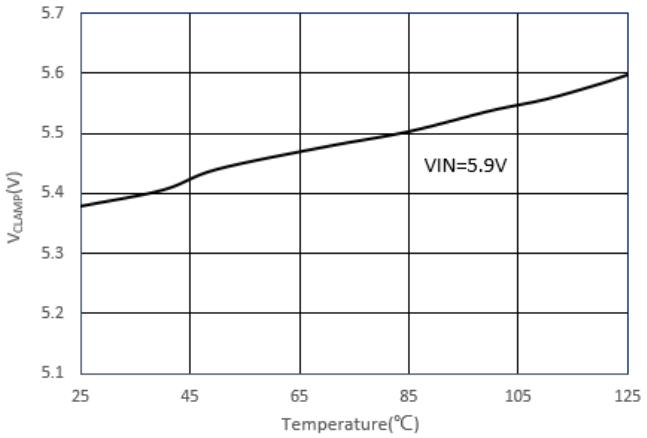


I_{ON} vs. Input Voltage

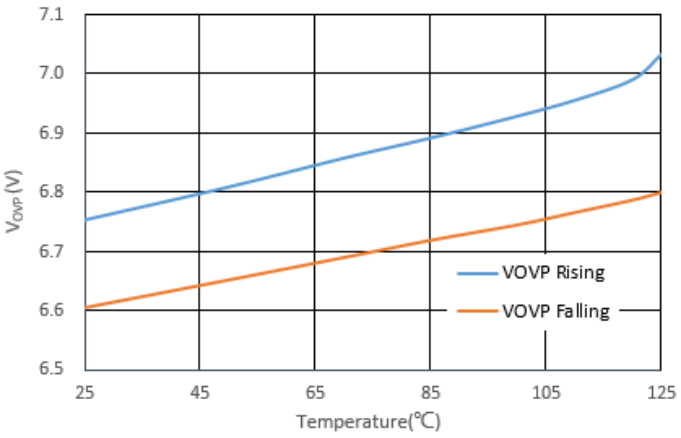


I_{OFF} vs. Input Voltage

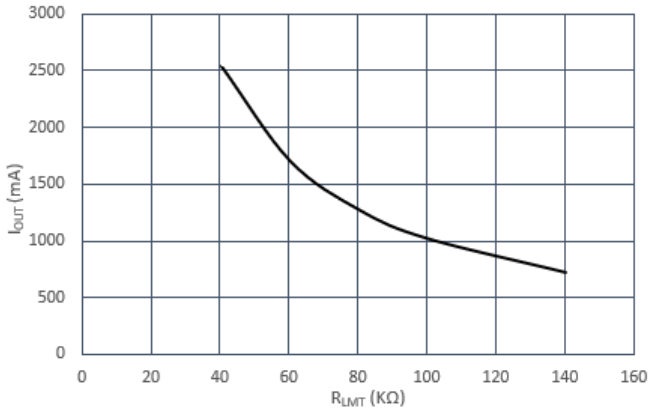
Typical Performance Characteristics (Continued)



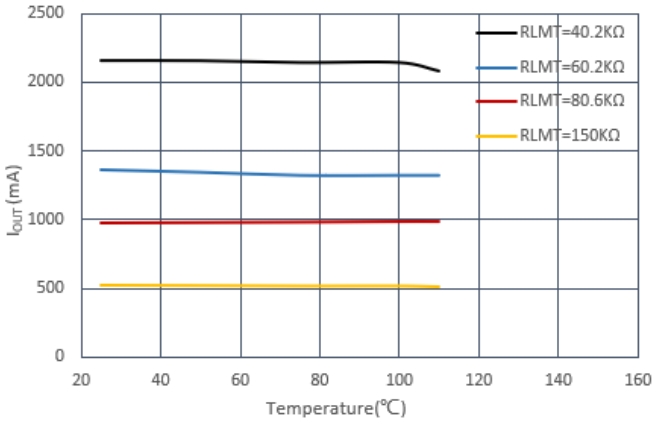
V_{CLMP} vs. Temperature



V_{OVP} vs. Temperature



I_{OCP} vs. R_{LMT}



I_{OCP} vs. Temperature

Functional Description

Device Operation

The APO2003DF is designed to provide protection to internal circuitry from external faults. The device continuously monitors the input voltage, the input current, and temperature. In case of an input overvoltage condition, the device immediately removes power by turning off the pass FET. In the case of an overcurrent condition, it limits the system current at the threshold value, and if the overcurrent persists, switches the pass FET off after a blanking period. The input overcurrent threshold is user-programmable. The device can monitor environmental temperature with a NTC thermistor as well as die temperature, and switches off when either of them exceeds pre-determined threshold. The device can be controlled by a processor, and also provides status information about fault conditions to the host.

Power-Down

The device remains in power down mode when the input voltage at the VIN pin is below the under-voltage threshold V_{UVLO}. The pass FET connected between VIN and VOUT pins is off, and the status output, nFAULT, is set to Hi-Z.

Power-On-Reset

The device resets when the input voltage at the VIN pin exceeds the V_{UVLO}. All internal counters and other circuit blocks are reset. The device then waits for duration t_{REC} for the input voltage to stabilize. After t_{REC}, if the input voltage is safe, pass FET is turned on. Because of the deglitch time at power-on, if the input voltage rises rapidly to beyond the OVP threshold, the device will not switch on at all, instead it will go into protection mode and indicate a fault on nFAULT pin. Once the device powers up, it continuously monitors the input voltage and the input current.

Input Overvoltage Protection

If the input voltage rises above over-voltage protection, the pass FET is turned off, removing power from internal circuitry. The response is very fast, with the FET turning off in less than a microsecond. The nFAULT pin is driven low. When the input voltage returns between V_{UVLO} and $V_{OVP} – V_{OVP\_HYS}$, the pass FET is turned on again after a deglitch time of t_{REC} to ensure that the input supply has stabilized. OVP threshold can be set either internally or externally. Internal OVP threshold can be selected by connecting OVLO pin to ground. To use external OVP threshold, just connect resistor divider to OVLO pin as shown in the typical application circuit, between VIN and GND. The protection voltage can be adjusted as following:

$$V_{OVP} = (R_1 + R_2) / R_2 * V_{OVLO\_TH}$$

Input Overcurrent Protection

The overcurrent threshold is programmed by a resistor R_{LMT} connected from the ILMT pin to GND. The relationship between current limit threshold and R_{LMT} can be approximated by the following equation:

$$I_{OCP}\ (A) = 93\ (A{\cdot}k\Omega) / R_{LMT}\ (k\Omega)$$

When the output is overloaded, the device will try to limit the current to I_{OCP}. If the overload condition is removed before blanking duration of t_{DGL_OCP}, the device continues to operate as normal. If the overcurrent situation persists longer than t_{DGL_OCP}, the pass FET shuts off, and nFAULT pin is driven low. Then the device will wait for a duration of t_{REC} before turning the FET back on to re-try. Once the FET is on, the current monitor is resumed to determine if overcurrent condition still exists. If yes, the FET shuts off again, and remains off for t_{REC} until next try. This hiccup cycle repeats until overload condition is removed or device is disabled.

Functional Description (Continued)

Thermal Protection

By connecting a NTC thermistor in series with a resistor (optional) from VIN to ENTS, and another resistor from ENTS to GND, the device can detect environmental temperature. The over temperature threshold (T_{OTP}) is set by the ratio of their resistance value. If the environmental temperature exceeds T_{OTP} longer than t_{DGL_OTP}, the FET is turned off with nFAULT pin driven low. The FET remains off as long as over temperature condition persists. Once the temperature drops, the FET will be turned back on after t_{REC}.

Also the device has an junction temperature protection circuit to protect device against system fault or improper use. When the junction temperature exceeds the threshold, 125°C typically, the device shuts down and stays off until the temperature cools down to a safe region (below falling threshold). Once the falling threshold, the device will automatically resume the normal operation after t_{REC}.

Enable Function

The device can be enabled or disabled through ENTS pin. When the ENTS pin is driven lower than V_{IL}, the internal FET is turned off. When the ENTS pin is higher than V_{IH}, the FET is turned on if other conditions are safe. The ENTS pin does not have any internal pull-down current and cannot be left floating. Note that the nFAULT pin functionality is also disabled when the ENTS pin is high.

Fault Indication

The nFAULT pin is an active-low open-drain output. It is in a high-impedance state when operating conditions are safe, or when the device is disabled by setting ENTS low. With ENTS high, the nFAULT pin goes low to indicate fault condition whenever any of these events occurs:

- Input overvoltage
- Input overcurrent
- Over temperature

OTG Function

In some applications, the equipment that APO2003DF resides in may be required to provide power to an accessory (e.g. a cellphone may power a headset or an external memory card) through the same connector pins that are used by the adapter for charging. In this situation, the device is required to support current flow from VOUT pin to VIN pin. If the following condition is met,

$$V_{OUT} > V_{UVLO} + 0.7V$$

the pass FET is turned on, and the reverse current flows through the channel of the pass FET. The pass FET will remain on as long as the following condition is met,

$$V_{OVP} + R_{DSON} \times I_{ACCESSORY} > V_{OUT} > V_{UVLO} - V_{UVLO\_HYST} + R_{DSON} \times I_{ACCESSORY}$$

Within this voltage range, the reverse current capability is the same as the forward capability. It should be noted that there is no overcurrent protection in this direction.

Application Information

Selection of R_1 and R_2

The ratio of R_1 and R_2 determines the over-voltage protection threshold. Once ratio is determined, a large absolute value is recommended for both R_1 and R_2, because they consume quiescent current even when device is not in use. Especially when powered by battery, this current needs to be minimized to extend the stand-by time.

Selection of R_{EN} and R_{TS}

The ENTS pin serves as both device enable and temperature sense. R_{EN} should be selected with relative to NTC thermistor so that ENTS voltage is higher than V_{IH} in normal operating region, but lower than the trip point of OTP protection. The trigger voltage can be calculated by the ratio of resistor divider as below

$$ratio = R_{EN} / (R_{NTC} + R_{TS} + R_{EN})$$

The default ratio is typical 65.7%. R_{NTC} is the value of NTC thermistor at desired temperature trip point.

For example, if 100kΩ NTC thermistor is selected, R_{EN} and R_{TS} can be configured to 150kΩ and 63.4kΩ respectively to have OTP tripped around 70°C. If OTP trip point requires better accuracy and higher quiescent current is acceptable, R_{TS} can be neglected. The table below shows typical combination of R_{TS} and R_{EN} for various temperature settings. If no temperature sense is required, NTC can be replaced by a resistor. Additionally R_{TS} and R_{EN} should be configured to ensure ENTS voltage is higher than V_{IH} in the desired operating region.

T_{OTP}	50°C	60°C	70°C	80°C	90°C
R_{TS} when R_{EN} = 150kΩ	45.3kΩ	56kΩ	63.4kΩ	68kΩ	71.5kΩ
R_{EN} when R_{TS} = 0Ω	63.4kΩ	42.2kΩ	29.4kΩ	20kΩ	14.3kΩ

R_{TS} and R_{EN} selection table for 100kΩ NTC thermistor

The OTP trip voltage is referred to Murata thermistor type, NCPWF104

NTC	50°C	60°C	70°C	80°C	90°C
Murata NCPWF104	33.195K	22.224K	15.184K	10.566K	7.481K

Selection of R_{nFAULT}

The nFAULT pin is an open-drain output that goes low during OVP, OCP, OTP, and TSD events. If the application does not require monitoring nFAULT pin, it can be left unconnected. However if required, it should be pulled high externally through R_{FAULT}, and connected to the host. The resistors should be of high value, in practice values between 10kΩ and 100kΩ should be sufficient.

Application Information

Selection of Input and Output Bypass Capacitors

The input capacitor C_{IN} is for decoupling and serves an important purpose. Whenever a step change downwards in the system load current occurs, the inductance of the input cable causes the input voltage to spike up. C_{IN} prevents the input voltage from overshooting to dangerous levels. It is recommended that a ceramic capacitor of at least 1µF be used at the input of the device. It must be located in close proximity to the VIN pin.

C_{OUT} is also important. During an over-voltage transient, this capacitance limits the output overshoot until the pass FET is turned off by the over-voltage protection circuitry. C_{OUT} must be a ceramic capacitor of at least 1µF, located close to the VOUT pin. C_{OUT} also serves as the input decoupling capacitor for the charging circuitry downstream.

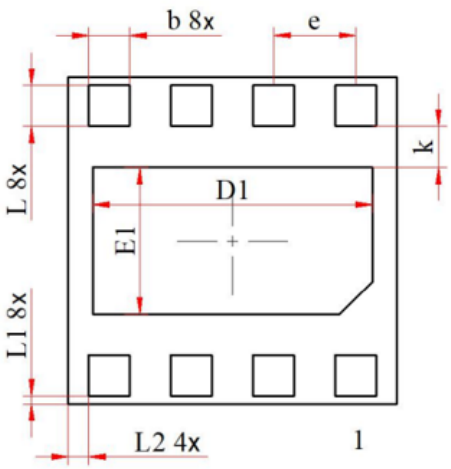
PCB Layout Guideline

This device is a protection device, and is meant to protect down-stream circuitry from hazardous voltages. Potentially, high voltages may be applied to this device. It has to be ensured that the edge-to-edge clearance of PCB traces satisfy the design rules for high voltages.

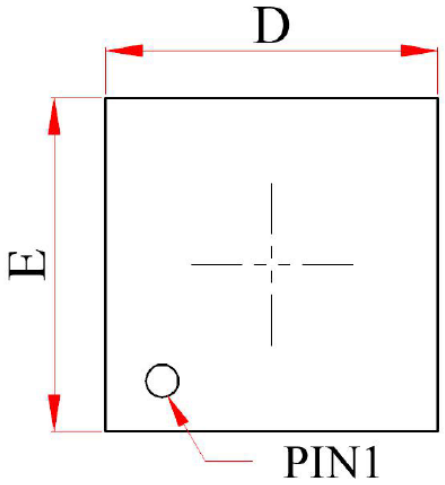
For good thermal performance, the exposed pad should be thermally coupled with the PCB ground plane. Usually this will require a copper pad directly underneath. This copper pad should be connected to the ground plane with an array of thermal vias.

C_{IN} and C_{OUT} should be put close to the device. Other components like R_{LMT}, R_1 and R_2 should sit close-by also.

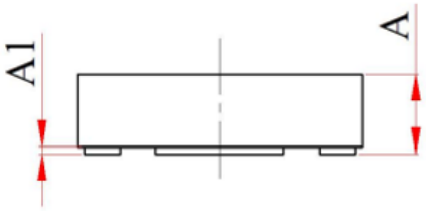
Package Outline Drawing



BOTTOM VIEW



Top View



SIDE VIEW

Symbol	Dimension In Millimeters			Dimension In Inches		
	Normal	Min	Max	Normal	Min	Max
A	--	0.500	0.600	--	0.020	0.024
A1	--	0.025	0.075	--	0.001	0.003
D	2.000	1.900	2.100	0.079	0.075	0.083
E	2.000	1.900	2.100	0.079	0.075	0.083
D1	1.700	1.600	1.800	0.067	0.063	0.071
E1	0.900	0.800	1.000	0.035	0.031	0.039
b	0.250	0.200	0.300	0.010	0.008	0.012
L	0.250	0.200	0.320	0.010	0.008	0.012
L1	0.050	0.000	0.090	0.002	0.000	0.004
L2	0.125 REF			0.005 REF		
k	0.250 REF			0.010 REF		
e	0.500 BSC			0.020 BSC		

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