Specification

資料中心參考文件用章
For Reference Only
2023.12.20
聯合聚晶股份有限公司
Integrated Solution Technology, Inc

Written by Department	Written by / Date	Approved by QRA Manager	Issued by D.C.C.
Research & Development	Sean 12/20/2023	Bonnie Lee 12/20/2023	Bonnie Lee 12/20/2023

Controlled by DCC

Copy List

Code Name	100	200	300	400	500	600	700
Dept.	HR	S/M	MFG	R&D	CH	QRA	MIS
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文件變更履歷頁

Document Change History

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description	變更依據文件號碼 ECN #	撰寫者 Writer	生效日期 Eff. Date
P001	-	New release	E03230007	Sean	2023/03/31
P002	-	Add test command	E06230017	Sean	2023/06/30
001	Page 48& 52 &54	Add Refresh 、DSLP Current Component Recommendation	E10230004	Sean	2023/10/05
002	P3	Remove I^2C interface for external temperature sensor	E10230012	Sean	2023/10/17
	P13	Modify description of TSCL/TSDA			
	P47，P48	Modify VDH1 to VDH, VDH2 to VDHR			
	P51-P54	Modify Application Circuit and Recommendation			
003	P16	Modify Read operation of 4-Line SPI	E12230003	Sean	2023/12/12
	P17	Modify Read operation of 3-Line SPI			
	P44&45	Add VDHR description of Power ON/OFF sequence			
	P37	Remove A3H command			
004	-	Modify Device Name IST7163CA1-C	E12230004	Sean	2023/12/20

續頁 CONTINUATION --- ☐ 是 YES; ☒ 否 NO

THIS CHIP HAS BEEN VERIFIED BY E INK ™ AND GOT E INK'S FULL 2BIT-E5 AUTHORIZATION.

This driver is an Active Matrix EPD all-in-one driver with timing controller for ESL. The sources have 2-bit outputs per pixel to support white/black/color. The timing controller provides control signals for the source driver and gate drivers.

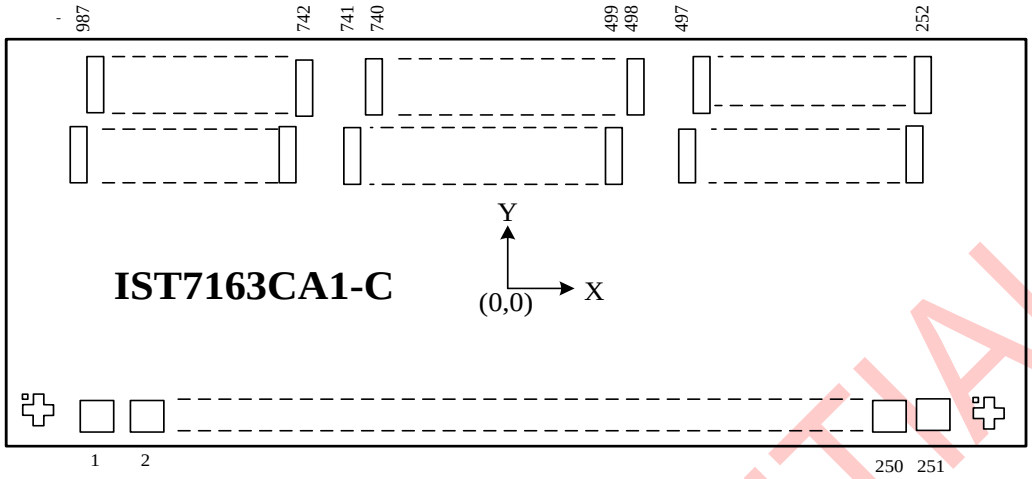
The DC-DC controller allows generate all necessary source and gate output voltage for VDH/VDL/VDHR (+/-3V~+/-15V), and VGH/VGL (+/-20v, +/-17v, +/-15v, +/-10v). The chip also includes an output buffer for the supply of the common electrode (VCOMAC or VCOMDC). The system is configurable through a 3-wire/4-wire (SPI) serial interface.

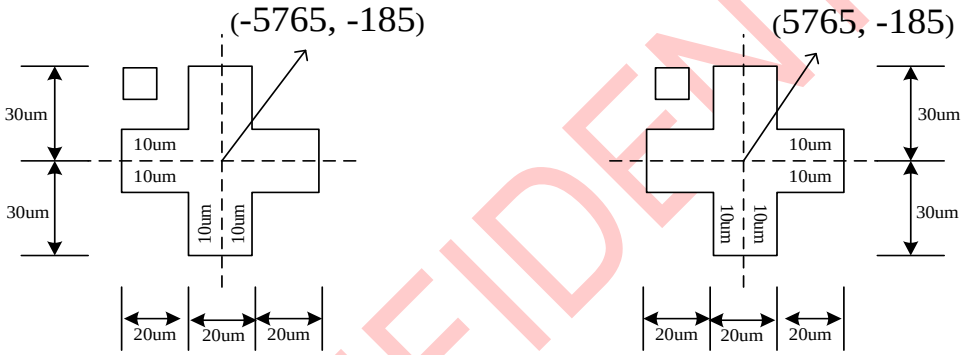
FEATURES

- System-on-chip (SOC) for ESL
- Timing controller support several all resolution
- Resolution: Support 240S x 480G
  - 240 Outputs source driver with 2-bit white/black/color per pixel
    - Output dynamic range (Voltage step: 100mV)
      - Mode 0 : 0V & VDH (+15V) & VDL (-15V) & VDHR (+3V~+15V)
      - Mode 1 : 0V & VDH (+3V~+15V) & VDL (-3V~-15V) & VDHR1 (+3V~+15V)
    - Mode 0 & 1 can be switched frame by frame (panel scanning frame)
    - Left and Right shift capability
  - 480 Output Gate drive
    - Output dynamic range: VGH and VGL: +/-20v, +/-17v, +/-15v, +/-10v
    - Up and Down shift capability
- Common electrode level
  - AC-VCOM and DC-VCOM
    - VCOMH=VDH+VCOMDC, VCOML=VDL+VCOMDC
  - Support sensing function
  - Support LUT
- Builtin frame memory maximum: (240 x480x2bits)x1 SRAM
- Builtin temperature sensor
  - On-Chip:On-Chip:-25~50°C (±2.0 °C)/8-bitstatus
- Support LPD, Low Power detection (VDD<2.5V)
- Support frame rate: 120Hz (max)
- 3-wire/4-wire (SPI) serial interface for system configuration: Clock rate up to 20MHz

- Digital supply voltage: 2.3~3.6V
- On-chip OTP for LUT and parameters (6K bytes)
- Support source cascade
- COG Package

PAD CONFIGURATION





Chip Size	11770 x 750um^2	
Bump Pitch	13um(min)	
Bump Spacing	1um(min)	
Bump Size(X*Y)	28x 70 um^2	Pad No = 1 ~ 251
	12 x 100 um^2	Pad No = 252~ 987
Bump Height	12um (Typ)	
Chip Thickness	300um (Typ)	
Hardness	90±15Hv	

PAD CENTER COORDINATES

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
1	NC<0>	-5750	-308	51	VDL	-3450	-308	101	VSS1	-1150	-308
2	VCOM	-5704	-308	52	VDL	-3404	-308	102	VSS3	-1104	-308
3	VCOM	-5658	-308	53	VDL	-3358	-308	103	VSS3	-1058	-308
4	VCOM	-5612	-308	54	VDL	-3312	-308	104	VSS3	-1012	-308
5	VCOM	-5566	-308	55	VSS1	-3266	-308	105	VSS3	-966	-308
6	VCOM	-5520	-308	56	VGH	-3220	-308	106	VSS5	-920	-308
7	VCOM	-5474	-308	57	VGH	-3174	-308	107	VSS5	-874	-308
8	VCOM	-5428	-308	58	VGH	-3128	-308	108	VSS2	-828	-308
9	VCOM	-5382	-308	59	VGH	-3082	-308	109	VSS2	-782	-308
10	VSS5	-5336	-308	60	VGH	-3036	-308	110	VSS2	-736	-308
11	DUMM	-5290	-308	61	VGH	-2990	-308	111	VSS2	-690	-308
12	DUMM	-5244	-308	62	VGH	-2944	-308	112	VSS2	-644	-308
13	DUMM	-5198	-308	63	VGH	-2898	-308	113	VSS4	-598	-308
14	DUMM	-5152	-308	64	VGH	-2852	-308	114	VSS4	-552	-308
15	DUMM	-5106	-308	65	VGH	-2806	-308	115	VSS4	-506	-308
16	DUMM	-5060	-308	66	VGH	-2760	-308	116	VSS4	-460	-308
17	DUMM	-5014	-308	67	VGH	-2714	-308	117	VSS4	-414	-308
18	DUMM	-4968	-308	68	VSS1	-2668	-308	118	VDD2	-368	-308
19	DUMM	-4922	-308	69	VDH	-2622	-308	119	VDD2	-322	-308
20	DUMM	-4876	-308	70	VDH	-2576	-308	120	VDD2	-276	-308
21	DUMM	-4830	-308	71	VDH	-2530	-308	121	VDD2	-230	-308
22	DUMM	-4784	-308	72	VDH	-2484	-308	122	VDD5	-184	-308
23	DUMM	-4738	-308	73	VDH	-2438	-308	123	VDD5	-138	-308
24	DUMM	-4692	-308	74	VDH	-2392	-308	124	VDD5	-92	-308
25	DUMM	-4646	-308	75	VDH	-2346	-308	125	VDD3	-46	-308
26	DUMM	-4600	-308	76	VDH	-2300	-308	126	VDD3	0	-308
27	DUMM	-4554	-308	77	VDH	-2254	-308	127	VDD3	46	-308
28	VGL	-4508	-308	78	VDH	-2208	-308	128	VDD1	92	-308
29	VGL	-4462	-308	79	VSS1	-2162	-308	129	VDD1	138	-308
30	VGL	-4416	-308	80	VPP	-2116	-308	130	VDD1	184	-308
31	VGL	-4370	-308	81	VPP	-2070	-308	131	VDD1	230	-308
32	VGL	-4324	-308	82	VPP	-2024	-308	132	VDD1	276	-308
33	VGL	-4278	-308	83	VPP	-1978	-308	133	VDD1	322	-308
34	VGL	-4232	-308	84	VPP	-1932	-308	134	VDD1	368	-308
35	VGL	-4186	-308	85	VPP	-1886	-308	135	DUMM	414	-308
36	VGL	-4140	-308	86	VDDLI	-1840	-308	136	DUMM	460	-308
37	VGL	-4094	-308	87	VDDLI	-1794	-308	137	DUMM	506	-308
38	VGL	-4048	-308	88	VDDLI	-1748	-308	138	DUMM	552	-308
39	VGL	-4002	-308	89	VDDLI	-1702	-308	139	DUMM	598	-308
40	VGL	-3956	-308	90	VDDLO	-1656	-308	140	DUMM	644	-308
41	VGL	-3910	-308	91	VDDLO	-1610	-308	141	DUMM	690	-308
42	VGL	-3864	-308	92	VDDLO	-1564	-308	142	DUMM	736	-308
43	VGL	-3818	-308	93	VDDLO	-1518	-308	143	TESTIN<	782	-308
44	VSS1	-3772	-308	94	VSS5	-1472	-308	144	DUMM	828	-308
45	VDL	-3726	-308	95	VSS5	-1426	-308	145	TESTIN<	874	-308
46	VDL	-3680	-308	96	VSS1	-1380	-308	146	DUMM	920	-308
47	VDL	-3634	-308	97	VSS1	-1334	-308	147	DUMM	966	-308
48	VDL	-3588	-308	98	VSS1	-1288	-308	148	DUMM	1012	-308
49	VDL	-3542	-308	99	VSS1	-1242	-308	149	M1M2	1058	-308
50	VDL	-3496	-308	100	VSS1	-1196	-308	150	DUMM	1104	-308

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
151	DUMM	1150	-308	201	CDAIO	3450	-308	251	NC<1>	5750	-308
152	MM	1196	-308	202	DUMM	3496	-308	252	NC<2>	5833	308
153	DUMM	1242	-308	203	TESTO1	3542	-308	253	NC<3>	5816	189
154	DUMM	1288	-308	204	DUMM	3588	-308	254	NC<4>	5799	308
155	VDDIO	1334	-308	205	TESTO2	3634	-308	255	G<0>	5782	189
156	VDDIO	1380	-308	206	DUMM	3680	-308	256	G<2>	5765	308
157	VDDIO	1426	-308	207	DUMM	3726	-308	257	G<4>	5748	189
158	VDDIO	1472	-308	208	DUMM	3772	-308	258	G<6>	5731	308
159	TESTIN<	1518	-308	209	DUMM	3818	-308	259	G<8>	5714	189
160	DUMM	1564	-308	210	DUMM	3864	-308	260	G<10>	5697	308
161	SDA	1610	-308	211	DUMM	3910	-308	261	G<12>	5680	189
162	DUMM	1656	-308	212	DUMM	3956	-308	262	G<14>	5663	308
163	DUMM	1702	-308	213	VDHR	4002	-308	263	G<16>	5646	189
164	SCL	1748	-308	214	VDHR	4048	-308	264	G<18>	5629	308
165	VSS1	1794	-308	215	VDHR	4094	-308	265	G<20>	5612	189
166	CSB	1840	-308	216	VDHR	4140	-308	266	G<22>	5595	308
167	VDDIO	1886	-308	217	VDHR	4186	-308	267	G<24>	5578	189
168	DUMM	1932	-308	218	VDHR	4232	-308	268	G<26>	5561	308
169	VSS1	1978	-308	219	VDHR	4278	-308	269	G<28>	5544	189
170	A0	2024	-308	220	VDHR	4324	-308	270	G<30>	5527	308
171	VDDIO	2070	-308	221	DUMM	4370	-308	271	G<32>	5510	189
172	DUMM	2116	-308	222	DUMM	4416	-308	272	G<34>	5493	308
173	VSS1	2162	-308	223	DUMM	4462	-308	273	G<36>	5476	189
174	RESB	2208	-308	224	DUMM	4508	-308	274	G<38>	5459	308
175	DUMM	2254	-308	225	VSS1	4554	-308	275	G<40>	5442	189
176	BUSY_N	2300	-308	226	FB	4600	-308	276	G<42>	5425	308
177	DUMM	2346	-308	227	FB	4646	-308	277	G<44>	5408	189
178	CL	2392	-308	228	VSS1	4692	-308	278	G<46>	5391	308
179	VDDIO	2438	-308	229	RESE	4738	-308	279	G<48>	5374	189
180	VSYNC	2484	-308	230	RESE	4784	-308	280	G<50>	5357	308
181	VSS1	2530	-308	231	VSS1	4830	-308	281	G<52>	5340	189
182	DUMM	2576	-308	232	DUMM	4876	-308	282	G<54>	5323	308
183	VDDIO	2622	-308	233	DUMM	4922	-308	283	G<56>	5306	189
184	BS	2668	-308	234	GDR	4968	-308	284	G<58>	5289	308
185	VSS1	2714	-308	235	GDR	5014	-308	285	G<60>	5272	189
186	DUMM	2760	-308	236	GDR	5060	-308	286	G<62>	5255	308
187	VDDIO	2806	-308	237	GDR	5106	-308	287	G<64>	5238	189
188	CPBI	2852	-308	238	GDR	5152	-308	288	G<66>	5221	308
189	VSS1	2898	-308	239	GDR	5198	-308	289	G<68>	5204	189
190	MS	2944	-308	240	GDR	5244	-308	290	G<70>	5187	308
191	VDDIO	2990	-308	241	GDR	5290	-308	291	G<72>	5170	189
192	DUMM	3036	-308	242	VSS5	5336	-308	292	G<74>	5153	308
193	TSDA	3082	-308	243	VCOM	5382	-308	293	G<76>	5136	189
194	TSDA	3128	-308	244	VCOM	5428	-308	294	G<78>	5119	308
195	TSCL	3174	-308	245	VCOM	5474	-308	295	G<80>	5102	189
196	TSCL	3220	-308	246	VCOM	5520	-308	296	G<82>	5085	308
197	DUMM	3266	-308	247	VCOM	5566	-308	297	G<84>	5068	189
198	DUMM	3312	-308	248	VCOM	5612	-308	298	G<86>	5051	308
199	CPBO	3358	-308	249	VCOM	5658	-308	299	G<88>	5034	189
200	DUMM	3404	-308	250	VCOM	5704	-308	300	G<90>	5017	308

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
301	G<92>	5000	189	351	G<192>	4150	189	401	G<292>	3300	189
302	G<94>	4983	308	352	G<194>	4133	308	402	G<294>	3283	308
303	G<96>	4966	189	353	G<196>	4116	189	403	G<296>	3266	189
304	G<98>	4949	308	354	G<198>	4099	308	404	G<298>	3249	308
305	G<100>	4932	189	355	G<200>	4082	189	405	G<300>	3232	189
306	G<102>	4915	308	356	G<202>	4065	308	406	G<302>	3215	308
307	G<104>	4898	189	357	G<204>	4048	189	407	G<304>	3198	189
308	G<106>	4881	308	358	G<206>	4031	308	408	G<306>	3181	308
309	G<108>	4864	189	359	G<208>	4014	189	409	G<308>	3164	189
310	G<110>	4847	308	360	G<210>	3997	308	410	G<310>	3147	308
311	G<112>	4830	189	361	G<212>	3980	189	411	G<312>	3130	189
312	G<114>	4813	308	362	G<214>	3963	308	412	G<314>	3113	308
313	G<116>	4796	189	363	G<216>	3946	189	413	G<316>	3096	189
314	G<118>	4779	308	364	G<218>	3929	308	414	G<318>	3079	308
315	G<120>	4762	189	365	G<220>	3912	189	415	G<320>	3062	189
316	G<122>	4745	308	366	G<222>	3895	308	416	G<322>	3045	308
317	G<124>	4728	189	367	G<224>	3878	189	417	G<324>	3028	189
318	G<126>	4711	308	368	G<226>	3861	308	418	G<326>	3011	308
319	G<128>	4694	189	369	G<228>	3844	189	419	G<328>	2994	189
320	G<130>	4677	308	370	G<230>	3827	308	420	G<330>	2977	308
321	G<132>	4660	189	371	G<232>	3810	189	421	G<332>	2960	189
322	G<134>	4643	308	372	G<234>	3793	308	422	G<334>	2943	308
323	G<136>	4626	189	373	G<236>	3776	189	423	G<336>	2926	189
324	G<138>	4609	308	374	G<238>	3759	308	424	G<338>	2909	308
325	G<140>	4592	189	375	G<240>	3742	189	425	G<340>	2892	189
326	G<142>	4575	308	376	G<242>	3725	308	426	G<342>	2875	308
327	G<144>	4558	189	377	G<244>	3708	189	427	G<344>	2858	189
328	G<146>	4541	308	378	G<246>	3691	308	428	G<346>	2841	308
329	G<148>	4524	189	379	G<248>	3674	189	429	G<348>	2824	189
330	G<150>	4507	308	380	G<250>	3657	308	430	G<350>	2807	308
331	G<152>	4490	189	381	G<252>	3640	189	431	G<352>	2790	189
332	G<154>	4473	308	382	G<254>	3623	308	432	G<354>	2773	308
333	G<156>	4456	189	383	G<256>	3606	189	433	G<356>	2756	189
334	G<158>	4439	308	384	G<258>	3589	308	434	G<358>	2739	308
335	G<160>	4422	189	385	G<260>	3572	189	435	G<360>	2722	189
336	G<162>	4405	308	386	G<262>	3555	308	436	G<362>	2705	308
337	G<164>	4388	189	387	G<264>	3538	189	437	G<364>	2688	189
338	G<166>	4371	308	388	G<266>	3521	308	438	G<366>	2671	308
339	G<168>	4354	189	389	G<268>	3504	189	439	G<368>	2654	189
340	G<170>	4337	308	390	G<270>	3487	308	440	G<370>	2637	308
341	G<172>	4320	189	391	G<272>	3470	189	441	G<372>	2620	189
342	G<174>	4303	308	392	G<274>	3453	308	442	G<374>	2603	308
343	G<176>	4286	189	393	G<276>	3436	189	443	G<376>	2586	189
344	G<178>	4269	308	394	G<278>	3419	308	444	G<378>	2569	308
345	G<180>	4252	189	395	G<280>	3402	189	445	G<380>	2552	189
346	G<182>	4235	308	396	G<282>	3385	308	446	G<382>	2535	308
347	G<184>	4218	189	397	G<284>	3368	189	447	G<384>	2518	189
348	G<186>	4201	308	398	G<286>	3351	308	448	G<386>	2501	308
349	G<188>	4184	189	399	G<288>	3334	189	449	G<388>	2484	189
350	G<190>	4167	308	400	G<290>	3317	308	450	G<390>	2467	308

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
451	G<392>	2450	189	501	S<1>	1540.5	189	551	S<51>	890.5	189
452	G<394>	2433	308	502	S<2>	1527.5	308	552	S<52>	877.5	308
453	G<396>	2416	189	503	S<3>	1514.5	189	553	S<53>	864.5	189
454	G<398>	2399	308	504	S<4>	1501.5	308	554	S<54>	851.5	308
455	G<400>	2382	189	505	S<5>	1488.5	189	555	S<55>	838.5	189
456	G<402>	2365	308	506	S<6>	1475.5	308	556	S<56>	825.5	308
457	G<404>	2348	189	507	S<7>	1462.5	189	557	S<57>	812.5	189
458	G<406>	2331	308	508	S<8>	1449.5	308	558	S<58>	799.5	308
459	G<408>	2314	189	509	S<9>	1436.5	189	559	S<59>	786.5	189
460	G<410>	2297	308	510	S<10>	1423.5	308	560	S<60>	773.5	308
461	G<412>	2280	189	511	S<11>	1410.5	189	561	S<61>	760.5	189
462	G<414>	2263	308	512	S<12>	1397.5	308	562	S<62>	747.5	308
463	G<416>	2246	189	513	S<13>	1384.5	189	563	S<63>	734.5	189
464	G<418>	2229	308	514	S<14>	1371.5	308	564	S<64>	721.5	308
465	G<420>	2212	189	515	S<15>	1358.5	189	565	S<65>	708.5	189
466	G<422>	2195	308	516	S<16>	1345.5	308	566	S<66>	695.5	308
467	G<424>	2178	189	517	S<17>	1332.5	189	567	S<67>	682.5	189
468	G<426>	2161	308	518	S<18>	1319.5	308	568	S<68>	669.5	308
469	G<428>	2144	189	519	S<19>	1306.5	189	569	S<69>	656.5	189
470	G<430>	2127	308	520	S<20>	1293.5	308	570	S<70>	643.5	308
471	G<432>	2110	189	521	S<21>	1280.5	189	571	S<71>	630.5	189
472	G<434>	2093	308	522	S<22>	1267.5	308	572	S<72>	617.5	308
473	G<436>	2076	189	523	S<23>	1254.5	189	573	S<73>	604.5	189
474	G<438>	2059	308	524	S<24>	1241.5	308	574	S<74>	591.5	308
475	G<440>	2042	189	525	S<25>	1228.5	189	575	S<75>	578.5	189
476	G<442>	2025	308	526	S<26>	1215.5	308	576	S<76>	565.5	308
477	G<444>	2008	189	527	S<27>	1202.5	189	577	S<77>	552.5	189
478	G<446>	1991	308	528	S<28>	1189.5	308	578	S<78>	539.5	308
479	G<448>	1974	189	529	S<29>	1176.5	189	579	S<79>	526.5	189
480	G<450>	1957	308	530	S<30>	1163.5	308	580	S<80>	513.5	308
481	G<452>	1940	189	531	S<31>	1150.5	189	581	S<81>	500.5	189
482	G<454>	1923	308	532	S<32>	1137.5	308	582	S<82>	487.5	308
483	G<456>	1906	189	533	S<33>	1124.5	189	583	S<83>	474.5	189
484	G<458>	1889	308	534	S<34>	1111.5	308	584	S<84>	461.5	308
485	G<460>	1872	189	535	S<35>	1098.5	189	585	S<85>	448.5	189
486	G<462>	1855	308	536	S<36>	1085.5	308	586	S<86>	435.5	308
487	G<464>	1838	189	537	S<37>	1072.5	189	587	S<87>	422.5	189
488	G<466>	1821	308	538	S<38>	1059.5	308	588	S<88>	409.5	308
489	G<468>	1804	189	539	S<39>	1046.5	189	589	S<89>	396.5	189
490	G<470>	1787	308	540	S<40>	1033.5	308	590	S<90>	383.5	308
491	G<472>	1770	189	541	S<41>	1020.5	189	591	S<91>	370.5	189
492	G<474>	1753	308	542	S<42>	1007.5	308	592	S<92>	357.5	308
493	G<476>	1736	189	543	S<43>	994.5	189	593	S<93>	344.5	189
494	G<478>	1719	308	544	S<44>	981.5	308	594	S<94>	331.5	308
495	NC<5>	1702	189	545	S<45>	968.5	189	595	S<95>	318.5	189
496	NC<6>	1685	308	546	S<46>	955.5	308	596	S<96>	305.5	308
497	NC<7>	1668	189	547	S<47>	942.5	189	597	S<97>	292.5	189
498	NC<8>	1579.5	308	548	S<48>	929.5	308	598	S<98>	279.5	308
499	VBD<1>	1566.5	189	549	S<49>	916.5	189	599	S<99>	266.5	189
500	S<0>	1553.5	308	550	S<50>	903.5	308	600	S<100>	253.5	308

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
601	S<101>	240.5	189	651	S<151>	-409.5	189	701	S<201>	-1059.5	189
602	S<102>	227.5	308	652	S<152>	-422.5	308	702	S<202>	-1072.5	308
603	S<103>	214.5	189	653	S<153>	-435.5	189	703	S<203>	-1085.5	189
604	S<104>	201.5	308	654	S<154>	-448.5	308	704	S<204>	-1098.5	308
605	S<105>	188.5	189	655	S<155>	-461.5	189	705	S<205>	-1111.5	189
606	S<106>	175.5	308	656	S<156>	-474.5	308	706	S<206>	-1124.5	308
607	S<107>	162.5	189	657	S<157>	-487.5	189	707	S<207>	-1137.5	189
608	S<108>	149.5	308	658	S<158>	-500.5	308	708	S<208>	-1150.5	308
609	S<109>	136.5	189	659	S<159>	-513.5	189	709	S<209>	-1163.5	189
610	S<110>	123.5	308	660	S<160>	-526.5	308	710	S<210>	-1176.5	308
611	S<111>	110.5	189	661	S<161>	-539.5	189	711	S<211>	-1189.5	189
612	S<112>	97.5	308	662	S<162>	-552.5	308	712	S<212>	-1202.5	308
613	S<113>	84.5	189	663	S<163>	-565.5	189	713	S<213>	-1215.5	189
614	S<114>	71.5	308	664	S<164>	-578.5	308	714	S<214>	-1228.5	308
615	S<115>	58.5	189	665	S<165>	-591.5	189	715	S<215>	-1241.5	189
616	S<116>	45.5	308	666	S<166>	-604.5	308	716	S<216>	-1254.5	308
617	S<117>	32.5	189	667	S<167>	-617.5	189	717	S<217>	-1267.5	189
618	S<118>	19.5	308	668	S<168>	-630.5	308	718	S<218>	-1280.5	308
619	S<119>	6.5	189	669	S<169>	-643.5	189	719	S<219>	-1293.5	189
620	S<120>	-6.5	308	670	S<170>	-656.5	308	720	S<220>	-1306.5	308
621	S<121>	-19.5	189	671	S<171>	-669.5	189	721	S<221>	-1319.5	189
622	S<122>	-32.5	308	672	S<172>	-682.5	308	722	S<222>	-1332.5	308
623	S<123>	-45.5	189	673	S<173>	-695.5	189	723	S<223>	-1345.5	189
624	S<124>	-58.5	308	674	S<174>	-708.5	308	724	S<224>	-1358.5	308
625	S<125>	-71.5	189	675	S<175>	-721.5	189	725	S<225>	-1371.5	189
626	S<126>	-84.5	308	676	S<176>	-734.5	308	726	S<226>	-1384.5	308
627	S<127>	-97.5	189	677	S<177>	-747.5	189	727	S<227>	-1397.5	189
628	S<128>	-110.5	308	678	S<178>	-760.5	308	728	S<228>	-1410.5	308
629	S<129>	-123.5	189	679	S<179>	-773.5	189	729	S<229>	-1423.5	189
630	S<130>	-136.5	308	680	S<180>	-786.5	308	730	S<230>	-1436.5	308
631	S<131>	-149.5	189	681	S<181>	-799.5	189	731	S<231>	-1449.5	189
632	S<132>	-162.5	308	682	S<182>	-812.5	308	732	S<232>	-1462.5	308
633	S<133>	-175.5	189	683	S<183>	-825.5	189	733	S<233>	-1475.5	189
634	S<134>	-188.5	308	684	S<184>	-838.5	308	734	S<234>	-1488.5	308
635	S<135>	-201.5	189	685	S<185>	-851.5	189	735	S<235>	-1501.5	189
636	S<136>	-214.5	308	686	S<186>	-864.5	308	736	S<236>	-1514.5	308
637	S<137>	-227.5	189	687	S<187>	-877.5	189	737	S<237>	-1527.5	189
638	S<138>	-240.5	308	688	S<188>	-890.5	308	738	S<238>	-1540.5	308
639	S<139>	-253.5	189	689	S<189>	-903.5	189	739	S<239>	-1553.5	189
640	S<140>	-266.5	308	690	S<190>	-916.5	308	740	VBD<2>	-1566.5	308
641	S<141>	-279.5	189	691	S<191>	-929.5	189	741	NC<9>	-1579.5	189
642	S<142>	-292.5	308	692	S<192>	-942.5	308	742	NC<10>	-1668	308
643	S<143>	-305.5	189	693	S<193>	-955.5	189	743	NC<11>	-1685	189
644	S<144>	-318.5	308	694	S<194>	-968.5	308	744	NC<12>	-1702	308
645	S<145>	-331.5	189	695	S<195>	-981.5	189	745	G<479>	-1719	189
646	S<146>	-344.5	308	696	S<196>	-994.5	308	746	G<477>	-1736	308
647	S<147>	-357.5	189	697	S<197>	-1007.5	189	747	G<475>	-1753	189
648	S<148>	-370.5	308	698	S<198>	-1020.5	308	748	G<473>	-1770	308
649	S<149>	-383.5	189	699	S<199>	-1033.5	189	749	G<471>	-1787	189
650	S<150>	-396.5	308	700	S<200>	-1046.5	308	750	G<469>	-1804	308

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
751	G<467>	-1821	189	801	G<367>	-2671	189	851	G<267>	-3521	189
752	G<465>	-1838	308	802	G<365>	-2688	308	852	G<265>	-3538	308
753	G<463>	-1855	189	803	G<363>	-2705	189	853	G<263>	-3555	189
754	G<461>	-1872	308	804	G<361>	-2722	308	854	G<261>	-3572	308
755	G<459>	-1889	189	805	G<359>	-2739	189	855	G<259>	-3589	189
756	G<457>	-1906	308	806	G<357>	-2756	308	856	G<257>	-3606	308
757	G<455>	-1923	189	807	G<355>	-2773	189	857	G<255>	-3623	189
758	G<453>	-1940	308	808	G<353>	-2790	308	858	G<253>	-3640	308
759	G<451>	-1957	189	809	G<351>	-2807	189	859	G<251>	-3657	189
760	G<449>	-1974	308	810	G<349>	-2824	308	860	G<249>	-3674	308
761	G<447>	-1991	189	811	G<347>	-2841	189	861	G<247>	-3691	189
762	G<445>	-2008	308	812	G<345>	-2858	308	862	G<245>	-3708	308
763	G<443>	-2025	189	813	G<343>	-2875	189	863	G<243>	-3725	189
764	G<441>	-2042	308	814	G<341>	-2892	308	864	G<241>	-3742	308
765	G<439>	-2059	189	815	G<339>	-2909	189	865	G<239>	-3759	189
766	G<437>	-2076	308	816	G<337>	-2926	308	866	G<237>	-3776	308
767	G<435>	-2093	189	817	G<335>	-2943	189	867	G<235>	-3793	189
768	G<433>	-2110	308	818	G<333>	-2960	308	868	G<233>	-3810	308
769	G<431>	-2127	189	819	G<331>	-2977	189	869	G<231>	-3827	189
770	G<429>	-2144	308	820	G<329>	-2994	308	870	G<229>	-3844	308
771	G<427>	-2161	189	821	G<327>	-3011	189	871	G<227>	-3861	189
772	G<425>	-2178	308	822	G<325>	-3028	308	872	G<225>	-3878	308
773	G<423>	-2195	189	823	G<323>	-3045	189	873	G<223>	-3895	189
774	G<421>	-2212	308	824	G<321>	-3062	308	874	G<221>	-3912	308
775	G<419>	-2229	189	825	G<319>	-3079	189	875	G<219>	-3929	189
776	G<417>	-2246	308	826	G<317>	-3096	308	876	G<217>	-3946	308
777	G<415>	-2263	189	827	G<315>	-3113	189	877	G<215>	-3963	189
778	G<413>	-2280	308	828	G<313>	-3130	308	878	G<213>	-3980	308
779	G<411>	-2297	189	829	G<311>	-3147	189	879	G<211>	-3997	189
780	G<409>	-2314	308	830	G<309>	-3164	308	880	G<209>	-4014	308
781	G<407>	-2331	189	831	G<307>	-3181	189	881	G<207>	-4031	189
782	G<405>	-2348	308	832	G<305>	-3198	308	882	G<205>	-4048	308
783	G<403>	-2365	189	833	G<303>	-3215	189	883	G<203>	-4065	189
784	G<401>	-2382	308	834	G<301>	-3232	308	884	G<201>	-4082	308
785	G<399>	-2399	189	835	G<299>	-3249	189	885	G<199>	-4099	189
786	G<397>	-2416	308	836	G<297>	-3266	308	886	G<197>	-4116	308
787	G<395>	-2433	189	837	G<295>	-3283	189	887	G<195>	-4133	189
788	G<393>	-2450	308	838	G<293>	-3300	308	888	G<193>	-4150	308
789	G<391>	-2467	189	839	G<291>	-3317	189	889	G<191>	-4167	189
790	G<389>	-2484	308	840	G<289>	-3334	308	890	G<189>	-4184	308
791	G<387>	-2501	189	841	G<287>	-3351	189	891	G<187>	-4201	189
792	G<385>	-2518	308	842	G<285>	-3368	308	892	G<185>	-4218	308
793	G<383>	-2535	189	843	G<283>	-3385	189	893	G<183>	-4235	189
794	G<381>	-2552	308	844	G<281>	-3402	308	894	G<181>	-4252	308
795	G<379>	-2569	189	845	G<279>	-3419	189	895	G<179>	-4269	189
796	G<377>	-2586	308	846	G<277>	-3436	308	896	G<177>	-4286	308
797	G<375>	-2603	189	847	G<275>	-3453	189	897	G<175>	-4303	189
798	G<373>	-2620	308	848	G<273>	-3470	308	898	G<173>	-4320	308
799	G<371>	-2637	189	849	G<271>	-3487	189	899	G<171>	-4337	189
800	G<369>	-2654	308	850	G<269>	-3504	308	900	G<169>	-4354	308

Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)	Pad No.	Pin Name	X(um)	Y(um)
901	G<167>	-4371	189	951	G<67>	-5221	189				
902	G<165>	-4388	308	952	G<65>	-5238	308				
903	G<163>	-4405	189	953	G<63>	-5255	189				
904	G<161>	-4422	308	954	G<61>	-5272	308				
905	G<159>	-4439	189	955	G<59>	-5289	189				
906	G<157>	-4456	308	956	G<57>	-5306	308				
907	G<155>	-4473	189	957	G<55>	-5323	189				
908	G<153>	-4490	308	958	G<53>	-5340	308				
909	G<151>	-4507	189	959	G<51>	-5357	189				
910	G<149>	-4524	308	960	G<49>	-5374	308				
911	G<147>	-4541	189	961	G<47>	-5391	189				
912	G<145>	-4558	308	962	G<45>	-5408	308				
913	G<143>	-4575	189	963	G<43>	-5425	189				
914	G<141>	-4592	308	964	G<41>	-5442	308				
915	G<139>	-4609	189	965	G<39>	-5459	189				
916	G<137>	-4626	308	966	G<37>	-5476	308				
917	G<135>	-4643	189	967	G<35>	-5493	189				
918	G<133>	-4660	308	968	G<33>	-5510	308				
919	G<131>	-4677	189	969	G<31>	-5527	189				
920	G<129>	-4694	308	970	G<29>	-5544	308				
921	G<127>	-4711	189	971	G<27>	-5561	189				
922	G<125>	-4728	308	972	G<25>	-5578	308				
923	G<123>	-4745	189	973	G<23>	-5595	189				
924	G<121>	-4762	308	974	G<21>	-5612	308				
925	G<119>	-4779	189	975	G<19>	-5629	189				
926	G<117>	-4796	308	976	G<17>	-5646	308				
927	G<115>	-4813	189	977	G<15>	-5663	189				
928	G<113>	-4830	308	978	G<13>	-5680	308				
929	G<111>	-4847	189	979	G<11>	-5697	189				
930	G<109>	-4864	308	980	G<9>	-5714	308				
931	G<107>	-4881	189	981	G<7>	-5731	189				
932	G<105>	-4898	308	982	G<5>	-5748	308				
933	G<103>	-4915	189	983	G<3>	-5765	189				
934	G<101>	-4932	308	984	G<1>	-5782	308				
935	G<99>	-4949	189	985	NC<13>	-5799	189				
936	G<97>	-4966	308	986	NC<14>	-5816	308				
937	G<95>	-4983	189	987	NC<15>	-5833	189				
938	G<93>	-5000	308								
939	G<91>	-5017	189								
940	G<89>	-5034	308								
941	G<87>	-5051	189								
942	G<85>	-5068	308								
943	G<83>	-5085	189								
944	G<81>	-5102	308								
945	G<79>	-5119	189								
946	G<77>	-5136	308								
947	G<75>	-5153	189								
948	G<73>	-5170	308								
949	G<71>	-5187	189								
950	G<69>	-5204	308								

PAD DESCRIPTION

Power Supply

Name	I/O	Description
VDDIO	Power Supply	IO power
VDD1/2/3/5	Power Supply	Analog power
VDDLI	Power Supply	Digital power
VDDLO	Power Supply	Digital power
VPP	Power Supply	OTP power
VSS1	Power Supply	Digital ground
VSS2/3/5	Power Supply	Analog ground
VSS4	Power Supply	Driver ground
VDH	I/O	Positive source driver Voltage
VDHR	I/O	Positive source driver voltage for Red
VDL	I/O	Negative source driver voltage

Micro-Controller interface

Name	I/O	Description
CL	I/O	Cascade clock, output when MS=H, input when MS=L
VSYNC	I/O	Cascade line frame sync, output when MS=H, input when MS=L
BS	I	Bus Selection. Select 3-wire / 4-wire SPI interface. L: 4-wire interface. H: 3-wire interface.
MS	I	Cascade setting pin. L: Slave chip. H: Master chip.
RESETB	I	Global reset pin. Low: reset.
A0	I	When SPI4 is select A0=L mean writing the command index to IST7163CA1-C A0=H mean writing command data or display data to IST7163CA1-C
BUSY_N	O	Driver busy flag. L: Driver is Busy. H: Host side can send command/data to driver.
CSB	I	Serial communication chip select.
SDA	I/O	Serial communication data input/output
SCL	I	Serial communication clock input.
TSCL	-	Not Connected.
TSDA	-	Not Connected.
CPBI	O	Check Panel broken input singal
CPBO	O	Check Panel broken output signal
GDR	O	N-MOS gate control, for booster circuit output.
RESE	O	Current sense input for control loop.
FB	O	(Keep Open.)
NC	-	Not Connected.

LCD Driver outputs

Name	I/O	Description
S<239:0>	O	Source driver output signals.
VBD<2:1>	O	Border output pins.
G<479:0>	O	Gate driver output signals.
VGH	I/O	Positive Gate voltage.
VGL	I/O	Negative Gate voltage.
VCOM	O	VCOM output.

I/O PIN ITO Resister Limitation

PIN Name	ITO Resister
VDDIO,VDD1/2/3/5,VSS1/2/3/4/5,VDDLI,VDDLO	<10Ω
VGH,VGL,VDH,VCOM,VDL,VDHR	<5Ω
VPP	<10Ω
BS,MS,BUSY_N,CSB,SDA,SCL,VSYNC,CL A0,CPBI,CPBO, GDR,RESE,FB	<1KΩ
RESETB	<10KΩ

FUNCTIONAL DESCRIPTION

Microprocessor Interface

CSB pin is used for chip selection. The IST7163CA1-C can interface with an MPU only when CSB is "L". When these pins are set to any other combination, A0, SCL, inputs are disabled and SDA are high impedance. In case of serial interface, the internal shift registers and the counter are reset.

MPU Interface types

IST7163CA1-C has two types of MPU interface, which are two serial interfaces, SPI3 and SPI4 serial interface is determined by BS pin as shown below.

BS	Type	Interface mode
H	SPI3	3-Line SPI Serial-mode
L	SPI4	4-Line SPI Serial-mode

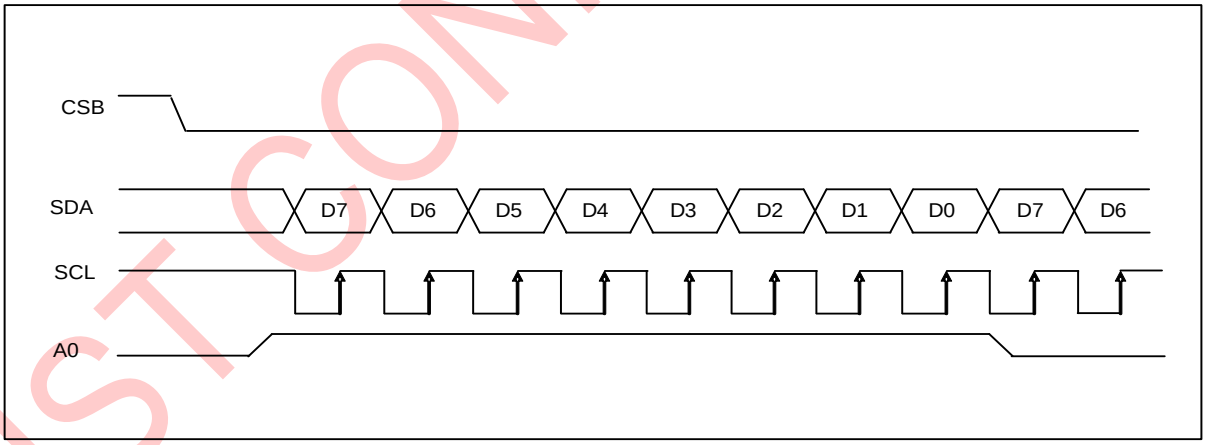
4-wire Serial Interface (BS= "L")

When BS= "L", the IST7163CA1-C configured as Serial interface(4-line), the serial data can be input/output through SDA and serial clock can be input through SCL.

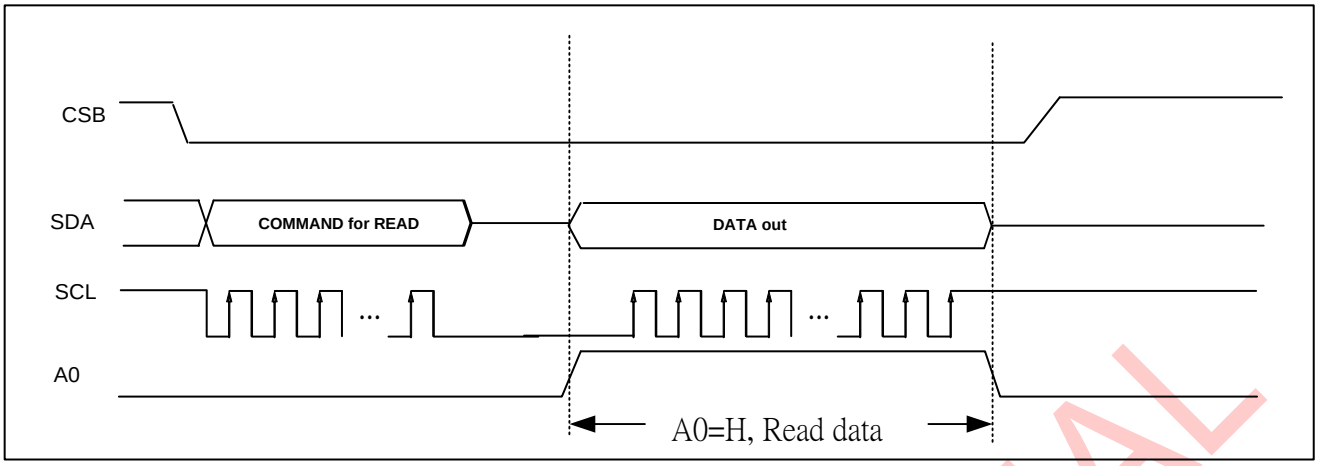
When the chip is not selected, the shift register & serial data counter will be reset and SDA&SCL will also be disabled internally.

When the chip is selected (CSB="L"), the serial data can be shifted in sequentially at the rising edge of SCL and transferred to 8-bit parallel data internally. When A0= "L", the IST7163CA1-C configured as command and A0= "H", the IST7163CA1-C configured as data.

4-Line Serial Interface Timing



Write operation of 4-Line SPI



Read operation of 4-Line SPI

3-wire Serial Interface (BS= "H")

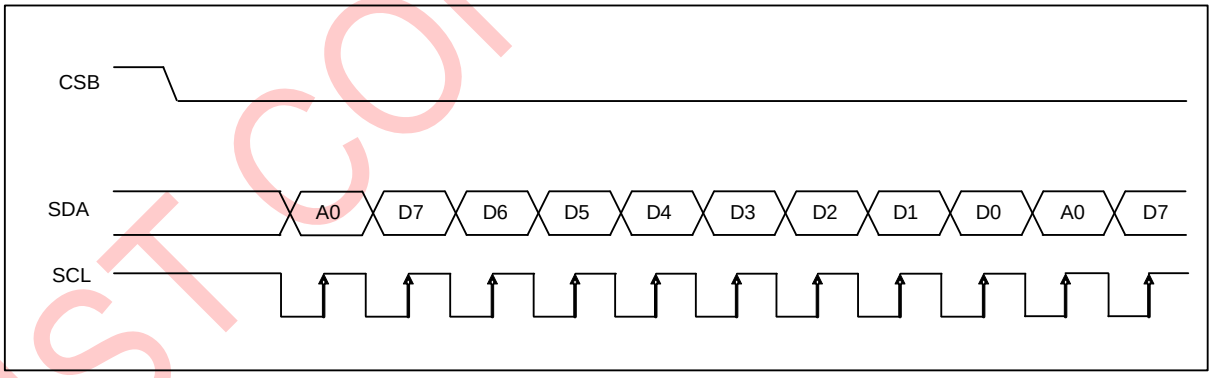
When BS= "H", the IST7163CA1-C configured as Serial interface(3-line), the serial data can be input/output through SDA and serial clock can be input through SCL.

When the chip is not selected, the shift register & serial data counter will be reset and SDA&SCL will also be disabled internally.

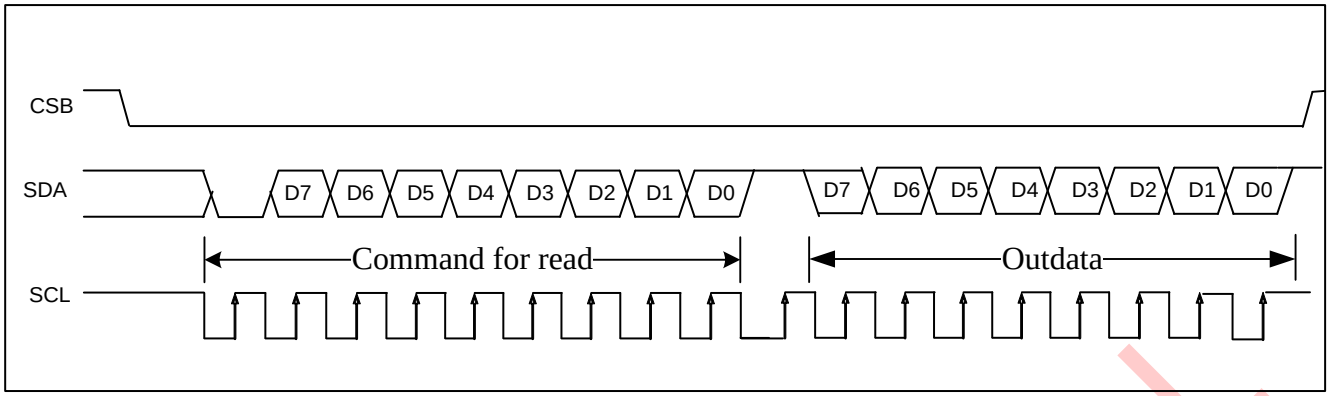
In 3-Line interface, A0 signal is not available and the 1st output of SDA will be treated as A0 flag.

When the chip is selected (CSB="L"), when1th SCL rising edge arise, SDA will be sampled as A0, 2th~9th SCL rising edge will shift the SDA to be a 8bit parallel data. and A0 will deside the 8bit data as command index or command dataor display data.

3-LineSerial Interface Timing



Write operation of 3-Line SPI



Read operation of 3-Line SPI

Busy Flag

The Busy Flag indicates whether the IST7163CA1-C is still during operation or not. When BUSY is "L", IST7163CA1-C is busy, and customer can read status from IST7163CA1-C to find out which operation trige the BUSY singal, It is not recommand writing display data or other command to IST7163CA1-C, except read the status of IST7163CA1-C.

COMMAND DESCRIPTION

R00H(PSR): Panel setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PSR	W	0	0	0	0	0	0	0	0	0	(00H)
1st Parameter	W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	1	(0FH)
2nd Parameter	W	1	LUT_EN	0	FOPT	VCMZ	1	TIEG	NORG	VC_LUTZ	(09H)

1st Parameter:

Bit7-6	Resolution setting
00b	Display resolution is 240x120 (default)
01b	Display resolution is 320x160
10b	Display resolution is 400x200
11b	Display resolution is 480x240

Bit5	Power switch operation mode
0	Power switching time in the period of frame scanning.(default).
1	Power switching time in the external period before frame scanning.

Bit3	UD function(*1)
0	Scandown; First line=Gn,Gn-1, … G2, Last line=G1
1	Scanup; First line=G1,G2, … ,Gn-1, Last line=Gn.(default)

Bit2	SHL function(*2)
0	Shift left; First data=Sn,Sn-1, … ,S2, Last data=S1.
1	Shift right; First data=S1,S2, … ,Sn-1, Last data=Sn.(default)

Bit1	SHD_N function(*3)
0	Booster OFF, register data are kept,and Source/Border/VCOM are kept 0V or floating
1	Booster ON.(default)

2nd Parameter:

Bit0	VC_LUTZ function
0	NO effect.
1	After refreshing display,the output of VCOM is set to floating automatically(default)

Bit1	NORG function
0	NO effect.(default)
1	After refreshing display,VCOM is tied to GND before power off

Bit2	TIEG function
0	NO effect.(default)
1	After power off booster,VGL will be tied to GND.

Bit4	VCMZ function
0	NO effect.(default)
1	VCOM is always floating.

Bit5	FOPT function
0	Scan 1 frame after waveform finished (Default)
1	No Scan after waveform finished and switch the source channel output to HiZ

Bit7	LUT_EN
0	LUT from OTP(default)
1	LUT from register

Priority of VCOM setting: VCMZ > NORG > FOPT > VC_LUTZ

FOPT setting is part of refreshing display.

FOPT: Power off floating.

Notes:

1. Non-select gate line keep at VGL for DSP/DRF and AMV
2. Inactive source line follow LUT for DSP/DRF
3. When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD off. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

R01H(PWR): Power Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PWR	W	0	0	0	0	0	0	0	0	1	(01H)
1st Parameter	W	1	-	-	-	-	-	VSC_EN	VS_EN	VG_EN	(07H)
2nd Parameter	W	1	-	-	-	-	-	-	VG[1]	VG[0]	(00H)
3rd Parameter	W	1	-	VDHR [6]	VDHR [5]	VDHR [4]	VDHR [3]	VDHR [2]	VDHR [1]	VDHR [0]	(00H)
4th Parameter	W	1	-	VDH [6]	VDH [5]	VDH [4]	VDH [3]	VDH [2]	VDH [1]	VDH [0]	(00H)
5th Parameter	W	1		VDL[6]	VDL [5]	VDL [4]	VDL [3]	VDL [2]	VDL [1]	VDL [0]	(00H)
6th Parameter	W	1		VDHR1 [6]	VDHR1 [5]	VDHR1 [4]	VDHR1 [3]	VDHR1 [2]	VDHR1 [1]	VDHR1 [0]	(00H)

Power mode switch mapping:

Mode 0 : 0V & +15V & -15V & VDHR (+3V~+15V)

Mode 1 : 0V & VDH (+3V~+15V) & VDL (-3V~-15V) & VDHR1 (+3V~+15V)

1st Parameter:

Bit2	Source LV power selection.
0	External source LV power from VDHR pins.
1	Internal DC/DC function for generate VDHR.

Bit1	Source power selection.
0	External source power from VDH/VDL pins.
1	Internal DC/DC function for generate VDH/VDL.

Bit0	Gate power selection.
0	External gate power from VGH/VGL pins.
1	Internal DCDC function for generate VGH/VGL.

2nd Parameter:

Bit1-0	VGHL Voltage Level.
00	VGH=20v, VGL=-20v(default)
01	VGH=17v, VGL=-17v
10	VGH=15v, VGL=-15v
11	VGH=10v, VGL=-10v

3rd & 4th Parameter: Internal VDHR/VDH power selection (Default value: 0000000b)

5th & 6th Parameter: Internal VDL/VDHR1 power selection (Default value: 0000000b)

Bit6-0	Internal VDH selection.	Internal VDL selection.	Bit6-0	Internal VDH selection.	Internal VDL selection.
0000000	3V	-3V	0110010	8.0V	-8.0V
0000001	3.1V	-3.1V	…	…	…
0000010	3.2V	-3.2V	0111100	9.0V	-9.0V
0000011	3.3V	-3.3V	…	…	…
0000100	3.4V	-3.4V	1000110	10.0V	-10.0V
0000101	3.5V	-3.5V	…	…	…
0000110	3.6V	-3.6V	1010000	11.0V	-11.0V
0000111	3.7V	-3.7V	…	…	…
0001000	3.8V	-3.8V	1011010	12.0V	-12.0V
0001001	3.9V	-3.9V	…	…	…
0001010	4.0V	-4.0V	1100100	13.0V	-13.0V
0001011	4.1V	-4.1V	…	…	…
0001100	4.2V	-4.2V	1101110	14.0V	-14.0V
0001101	4.3V	-4.3V	…	…	…
0001110	4.4V	-4.4V	1111000	15.0V	-15.0V
0001111	4.5V	-4.5V			
0010000	4.6V	-4.6V			
…	…	…			
0010100	5.0V	-5.0V			
…	…	…			
0011110	6.0V	-6.0V			
…	…	…			
0101000	7.0V	-7.0V			
…	…	…			

Notes:

1. VGH-VDH/VGH-VDHR/VGH-VDHR1 ≧ 2v
2. VGL-VDL ≧ -2v

R02H(POF): Power OFF Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
POF	W	0	0	0	0	0	0	0	1	0	(02H)
1st Parameter	W	1	0	0	0	0	0	0	0	0	(00H)

After power off command, driver will power off base on power off sequence. After power off command, BUSY_N signal will become “0”.

Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, and temperature sensor, but register will keep until VDD become off.

SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

R03H(POFS): Power on/off Sequence Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PFS	W	0	0	0	0	0	0	0	1	1	(03H)
1st Parameter	W	1	-	-	T_VDPG_OFF		-	-	T_VDS_OFF		(00H)

1st Parameter:

Bit1-0	Power off sequence of VDH and VDL
00b	20ms(default)
01b	40ms
10b	60ms
11b	80ms

Bit5-4	Power off sequence of VGH and VGL
00b	20ms(default)
01b	40ms
10b	60ms
11b	80ms

R04H(PON):Power ON Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PON	W	0	0	0	0	0	0	1	0	0	(04H)

After power on command, the driver will power ON base on Power ON sequence.

After power on command and all power sequence are ready (based on PWR command), then BUSY_N signal will become “1”.

This command only active when BUSY_N=“1”.

R06H(BTST): Booster Soft Command Reglster

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
LUT0	W	0	0	0	1	0	0	0	0	0	(06H)
1st Parameter	W	1	BT_PHA1	BT_PHA0	0	0	0	0	0	0	(00H)
2st Parameter	W	1	BT_PHB1	BT_PHB0		0	0	0	0	0	(00H)
3st Parameter	W	1	BT_PHC1	BT_PHC0		0	0	0	0	0	(00H)

D7-D6	soft start perild
00	10ms (default)
01	20ms
10	30ms
11	40ms

R07H(DSLP): Deep Sleep Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DSLP	W	0	0	0	0	0	0	1	1	1	(07H)
1st Parameter	W	1	1	0	1	0	0	1	0	1	(A5H)

After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be excited if check code = 0xA5.

R10H(DTM): Data Start Transmission Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DTM	W	0	0	0	0	1	0	0	0	0	(10H)
2-bit mode											
1st Parameter	W	1	Pixel1		Pixel2		Pixel3		Pixel4		(00H)
⋮	W	1	⋮		⋮		⋮		⋮		(00H)
Nth Parameter	W	1	Pixel(n-3)		Pixel(n-2)		Pixel(n-1)		Pixel(n)		(00H)

NOTE:"-" Don't care, can be set to VDD or GND level. "X": Dummy data, it would not be stored in frame buffer.

This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Data Refresh command (R12H). Then the chip will start to send data/VCOM for panel.

Pixel[1~n][1:0](2-bitmode):

`	Source Driver Output			
ImageData	DDX=1(Default)		DDX=0	
Pixel[1:0]	Gray level select	IP output LUT select	Gray level select	IP output LUT select
00	Gray0	ogray00	Gray3	ogray03
01	Gray1	ogray01	Gray2	ogray02
10	Gray2	ogray02	Gray1	ogray01
11	Gray3	ogray03	Gray0	ogray00

Data mapping example:

When DDX=1, Pixel[1:0]=01 -> Gray level select = Gray1, follow LUT data output from IP output port "ogray01".
When DDX=0, Pixel[1:0] = 11 -> Gray level select = Gray 0, follow LUT data output from IP output port "ogray00".

R11H(DSP): DataStop Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DSP	W	0	0	0	0	1	0	0	0	1	(11H)
1st Parameter	R	1	data_flag	-	-	-	-	-	-	-	(00H)

To stop data transmission,this command must be issued to check the data_flag.

1st Parameter:

Bit7	Data flag of receiving user data.
0	Driver didn't receive all the data.
1	Driver has already received all the one frame data.

After "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts.

This command only active when BUSY_N = "1".

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R12H(DRF): Display Refresh Command Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
DRF	W	0	0	0	0	1	0	0	1	0	(12H)
1st Parameter	W	1	-	-	-	-	-	-	-	AC/DCVCOM	(00H)

While user sent this command,driver will refresh display(data/VCOM) base on SRAM data and LUT.

AC/DCVCOM: AC,DCVCOM select.

0: ACVCOM,VCOM will follow LUT when updating image. (default)

1: DCVCOM,VCOM will always be VCOMDC when updating image

After display refresh command, BUSY_N signal will become "0"

This command only active when BUSY_N = "1".

R17H(AUTO): Auto Sequence Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Auto Sequence	W	0	0	0	0	1	0	1	1	1	(17H)
	W	1	1	0	1	0	0	1	0	1	(A5H)

The command can enable the internal sequence to execute several commands continuously.

The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host‟s control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.

AUTO(0x17)+Code(0xA5)=(PON → DRF → POF)

AUTO(0x17)+Code(0xA7)=(PON → DRF→ POF → DSLP)

R30H(PLL): PLL Control Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
PLL	W	0	0	0	1	1	0	0	0	0	(30H)
1st Parameter	W	1	-	-	-	-	Dyna	FR[2]	FR[1]	FR[0]	(02H)

The command controls the PLL clock frequency.The PLL structure must support the following frame rates:

Bit3	Dynamic frame rate (EInk use only)
0	Disable(default)
1	Enable

FR[2:0]	Framerate
000	12.5 Hz
001	25 Hz
010	50 Hz (default)
011	65 Hz
100	75 Hz
101	85 Hz
110	100 Hz
111	120 Hz

R40H(TSC): Temperature Sensor Command Register

Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TSC	W	0	0	1	0	0	0	0	0	0	(40H)
1st Parameter	R	1	TS[7]	TS[6]	TS[5]	TS[4]	TS[3]	TS[2]	TS[1]	TS[0]	(00H)

This command indicates the temperature value.

R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value.

BUSY_N become low after TSC command. WhenBUSY_N become high, Parameter can be read.

This command only active when BUSY_N="1"

Temperature boundary(internal temperature sensor): -25C~60C

D[10:3]	Temperature (°C)	D[10:3]	Temperature (°C)
1110_0111	-25	0000_0000	0
1110_1000	-24	0000_0001	1
1110_1001	-23	0000_0010	2
1110_1010	-22	0000_0011	3
1110_1011	-21	0000_0100	4
1110_1100	-20	0000_0101	5
1110_1101	-19	0000_0110	6
…	…	…	…
1111_1110	-2	0011_1011	59
1111_1111	-1	0011_1100	60

R41H(TSE): Temperature Sensor Enable Register

Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TSE	W	0	0	1	0	0	0	0	0	1	(41H)
1st Parameter	W	1	TSE	-	-	-	TO[3]	TO[2]	TO[1]	TO[0]	(00H)

This command indicates the driver IC temperature sensor enable and calibration function.

1st Parameter:

Bit3-0	Temperature level	Bit3-0	Temperature level
0000	+0℃(Default)	1000	-4℃
0001	+0.5℃	1001	-3.5℃
…	…	…	…
0111	+3.5℃	1111	-0.5℃

Bit[3:0]: Reserve one temperature offset TO[3:0] for calibration

1. TO[3]: mean "+" or "-" while 0 is "+"; 1 is "-"

2. TO[2:0]: mean temperature offset value

R44H(GPI Sensing): GPIO Input Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Check Panel Glass	W	0	0	1	0	0	0	1	0	0	(44H)
	W	1	-	-	-	-	-	-	-	GPIS	(00H)

This command will indicate status of GPI

GPIS : 0 detected low logic on GPIO

1 detected high logic on GPIO

R50H(CDI): VCOM and DATA Interval Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
CDI	W	0	0	1	0	1	0	0	0	0	(50H)
1st Parameter	W	1	VBD[2]	VBD[1]	VBD[0]	DDX[0]	CDI[3]	CDI[2]	CDI[1]	CDI[0]	(97H)

This command can set 2 kinds of parameters,1.VCOM to data output interval(CDI) 2.Boarder pin output.

VBD[2:0]: Border data selection (from LUT output by IP port border_w[1:0]).

This register will make boarder pin output being mapped to a certain grayscale.

DDX[0]	VBD[2:0]	Gray level select	IP setting for Border LUT select
0	000	Floating	N/A
	001	Gray3	border_buf=011
	010	Gray2	border_buf=010
	011	Gray1	border_buf=001
	100	Gray0	border_buf=000
1 (Default)	000	Gray0	border_buf=000
	001	Gray1	border_buf=001
	010	Gray2	border_buf=010
	011	Gray3	border_buf=011
	100	Floating(Default)	N/A

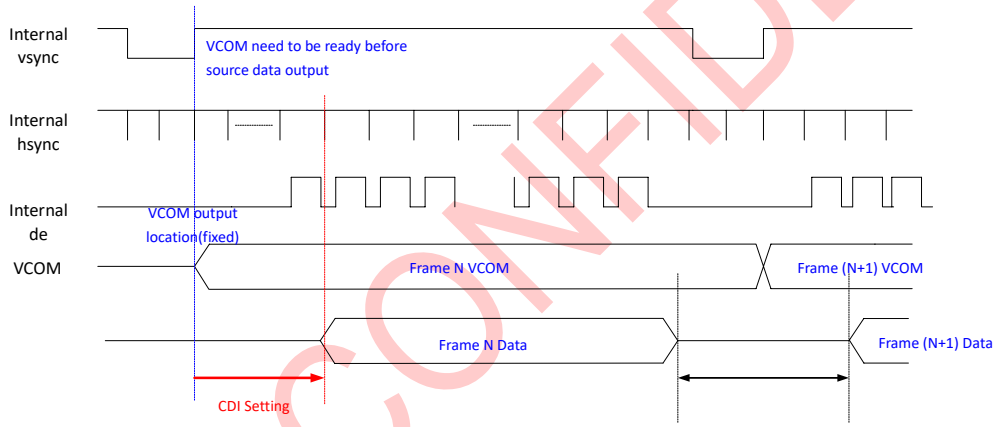
Border output voltage level: The level selection is based on mapping LUT data.

Ex: Gray 1 waveform is mapping to 15V, without VCOM offset,the real output on Boarder pin shall be 15V.

Boarder output will follow FOPT definition being defined in R00h

This command indicates the interval of Vcom and data output.When setting the vertical backporch, the total blanking will be kept as a default value (count by HSYNC)

Bit3	Bit2	Bit1	Bit0	VCOM and data interval
0	0	0	0	17 hsync
0	0	0	1	16 hsync
0	0	1	0	15 hsync
0	0	1	1	14 hsync
0	1	0	0	13 hsync
0	1	0	1	12 hsync
0	1	1	0	11 hsync
0	1	1	1	10 hsync (Default)
1	0	0	0	9 hsync.
1	0	0	1	8 hsync
1	0	1	0	7 hsync
1	0	1	1	6 hsync
1	1	0	0	5 hsync
1	1	0	1	4 hsync
1	1	1	0	3 hsync
1	1	1	1	2 hsync



R51H(LPD): Lower Power Detection Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
LPD	W	0	0	1	0	1	0	0	0	1	(51H)
1st Parameter	R	1	-	-	-	-	-	-	-	LPD	(01H)

This command indicates the input power condition. Host can read this data to understand the battery condition.

When LPD="1",system input power is normal.

When LPD="0",Low power input (VDD<2.5V,selected by LVD_SEL[1:0] in command LVSEL)

Bit0	LPD
0	Lowpowerinput.
1	Normalstatus.(Default)

This command only active when BUSY_N="1".

R60H (TCON): TCON setting Register

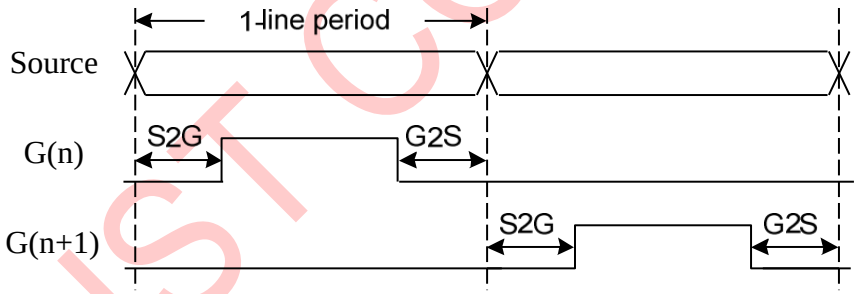
Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TSC	W	0	0	1	1	0	0	0	0	0	(60H)
1st Parameter	W	1	-	-	S2G[5]	S2G[4]	S2G[3]	S2G[2]	S2G[1]	S2G[0]	(02H)
2nd Parameter	W	1	-	-	G2S[5]	G2S[4]	G2S[3]	G2S[2]	G2S[1]	G2S[0]	(02H)

The command define as Non-overlap period of gate and source and as below:

S2G[5:0] or G2S[5:0]	Period
0	1unit
1	2unit
2	3unit**(Default)**
3	4unit
4	5unit
5	6unit
6	7unit
7	8unit
8	9unit
9	10unit
10	11unit
11	12unit
12	13unit
13	14unit
….	…
63	64unit

1 unit = 500ns

Gon_T= 1 line period – S2G –G2S, minimum Gon_T = 2 units. If(1line period – S2G –G2S) <2 units , Gon_T = 2 units



R61H(TRES): Resolution Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TRES	W	0	0	1	1	0	0	0	0	1	(61H)
1st Parameter	W	1	-	-	-	-	-	-	HRES(9)	HRES(8)	(00H)
2nd Parameter	W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	(00H)
3rd Parameter	W	1	-	-	-	-	-	-	VRES(9)	VRES(8)	(00H)
4th Parameter	W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	(00H)

Note: HRES ≦ Horizontal line of PSR, VRES ≦Vertical line of PSR.

No matter what value being set in D1 and D0 of 1st parameter(HRES[1] and HRES[0]), the register shall be kept as 0

When using register:

Horizontal display resolution = HRES

Vertical display resolution = VRES

HRES[9]=0,HRES[8]=0,and VRES[9]=0

Channel disable calculation:

GD: First G active=G0; LAST active GD = first active+VRES[7:0]-1

SD: First active channel:=S0; LAST activeSD = first active+HRES[7:2]*4-1

R65H(GSST): GATE/SOURCE START SETTING

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
GSST	W	0	0	1	1	0	0	1	0	1	(65H)
1st Parameter	W	1	-	-	-	-	-	-	-	-	(00H)
2nd Parameter	W	1	HST (7)	HST (6)	HST (5)	HST (4)	HST (3)	HST (2)	0	0	(00H)
3rd Parameter	W	1	-	-	-	-	-	-	VST (9)	VST (8)	(00H)
4th Parameter	W	1	VST (7)	VST (6)	VST (5)	VST (4)	VST (3)	VST (2)	VST (1)	VST (0)	(00H)

This command defines resolution start gate/source position.

HST[7:3]: Horizontal Display Start Position (Source)

VST[8:0]:Vertical Display Start Position (Gate)

R70H(REV): Chip Revision Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
REV	W	0	0	1	1	1	0	0	0	0	(70H)
1st Parameter	R	1	REV0[7]	REV0[6]	REV0[5]	REV0[4]	REV0[3]	REV0[2]	REV0[1]	REV0[0]	(0BH)
2nd Parameter	R	1	REV1[7]	REV1[6]	REV1[5]	REV1[4]	REV1[3]	REV1[2]	REV1[1]	REV1[0]	(04H)
3rd Parameter	R	1	REV2[7]	REV2[6]	REV2[5]	REV2[4]	REV2[3]	REV2[2]	REV2[1]	REV2[0]	(01H)

1nd Parameter:

Bit7-0	REV0
-	EInk internal number

2nd Parameter:

Bit7-0	REV1
-	EInk internal number

3rd Parameter:

Bit7-0	REV2
-	Increased each revision

R80H(AMV): Auto Measurement VCOM Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
AMV	W	0	1	0	0	0	0	0	0	0	(80H)
1st Parameter	W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	AMVX	AMVS	AMV	AMVE	(00H)

This command is to set the configuration of VCOM sensing.

1st Parameter:

Bit7-6	The sensing points of sampling time
00	2(default)
01	4
10	8
11	16

Sampling time= the last quarter of sensing time (T)

VCOM = average of N points. N=2,4,8,16

Bit5-4	The sensing time of VCOM detection
00	5s(default)
01	10s
10	15s
11	20s

Bit3	XON setting for all Gate ON of AMV
0	Gate scan normally during Auto Measure VCOM period.(default)
1	NO effect

Bit2	AMVS setting for Source output of AMV
0	Source output 0V during Auto Measure VCOM period.(default)
1	Source output VSPL during Auto MeasureVCOM period.

Bit1	Analogy signal
0	Get VCOM value by R81H(default)
1	Gate scan only. Measure VCOM externally by probing the VCOM pad.

Bit0	Auto Measure VCOM setting
0	Auto measure VCOM disble (default)
1	Auto measure VCOM enable

R81H(VV): VCOM Value Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VV	W	0	1	0	0	0	0	0	0	1	(81H)
1st Parameter	R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	(00H)

This command gets Vcom value.

1st Parameter:

Bit6-0	VCOM value
0000000	0V
0000001	-0.05V
0000010	-0.10V
⋮	⋮
1010000	-4.00V
Others	-

R82H(VDCS): VCM_DC Setting Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
VDCS	W	0	1	0	0	0	0	0	1	0	(82H)
1st Parameter	W	1	0	VDCS[6]	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	VDCS[1]	VDCS[0]	(00H)

This command set the VCOMDC value. Driver will base on this value for VCM_DC.

Bit6-0	VCOM value
0000000	0V(default)
0000001	-0.05V
0000010	-0.10V
⋮	⋮
1010000	-4.00V
Others	-

R90H(PGM): Program Mode

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Ente rProgram Mode	W	0	1	0	0	1	0	0	0	0	(90H)

After this command is issued,the chip would enter the program mode, Power mode = 1.

After the programming procedure completed,a hardware reset is necessary for leaving program mode

R91H(APG): Active Program

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Active Program OTP	W	0	1	0	0	1	0	0	0	1	(91H)

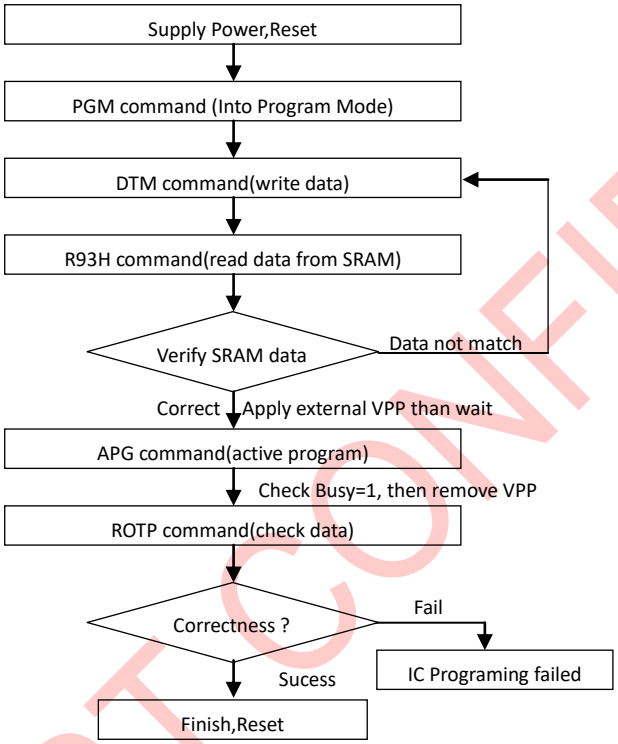
After this command is transmitted,the programming state machine would be activated.

The BUSY_N flag would fall to 0 until the programming is completed.

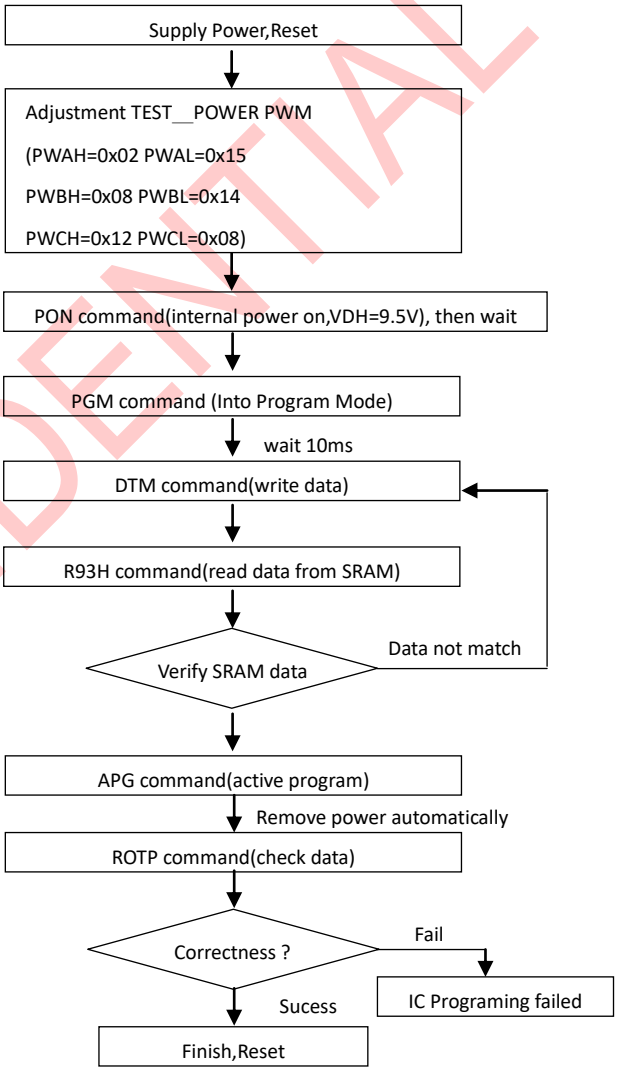
This command only active when BUSY_N="1"

R92H(ROTP): Read OTP Data

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Read OTP Data	W	0	1	0	0	1	0	0	1	0	(92H)
	R	1	Dummy								(00H)
	R	1	The data of address0 in the OTP								(00H)
	R	1									(00H)
	R	1	The data of address(n) in the OTP								(00H)



OTP Programming Flow (External VPP)



OTP Programming Flow (Internal VPP)

R93H(RSRAM):Read SRAM Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Read SRAM Data	W	0	1	0	0	1	0	0	1	0	(93H)
	R	1	Dummy								(00H)
	R	1	The data of address0 in the SRAM								(00H)
	R	1									(00H)
	R	1	The data of address(n) in the SRAM								(00H)

RA2H(PGM_CFG):OTP Program Config Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
OTP program Config	W	0	1	0	1	0	0	0	1	0	(A2H)
1st Parameter	W	1	-	-	-	VPPSEL	-	-	-	-	(00H)
2nd Parameter	W	1	PGM_SADDR[15:8]								(00H)
3rd Parameter	W	1	PGM_SADDR[7:0]								(00H)
4th Parameter	W	1	PGM_DSIZE[15:8]								(15H)
5th Parameter	W	1	PGM_DSIZE[7:0]								(DFH)

This command is to set the configuration of OTP

1st Parameter

Bit4	VPPSEL
0	External VPP **(default)**
1	Internal VPP

2nd and 3rd Parameters: Program start address PGM_SADDR[15:0]

4th and 5th Parameters: Program data size PGM_DSIZE[15:0]

RE0H(CCSET):Chip Temperature Input Select Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Temperature Input	W	0	1	1	1	0	0	0	0	0	(E0H)
1st Parameter	W	1	-	-	-	-	-	-	TSFIX	0	(00H)

This command is control input path of temperature value

1st Parameter:

Bit0	Temperature Input Selection
0	Use internal temperature sensor **(default)**
1	Use TSSET[7:0] value

RE4H(LVSEL): LVD Voltage Select Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Select LVD Voltage	W	0	1	1	1	0	0	1	0	0	(E4H)
1st Parameter	W	1	-	-	-	-	-	-	LVD_SEL[1:0]		(03H)

LVD_SEL[1:0]: Low Power Voltage selection

LVD_SEL[1:0]	LVDvalue
00	<2.2V
01	<2.3V
10	<2.4V
11	<2.5V (default)

RE6H(TSSET): Force Temperature Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
Force Temperature	W	0	1	1	1	0	0	1	1	0	(E6H)
1st Parameter	W	1	TS[7]	TS[6]	TS[5]	TS[4]	TS[3]	TS[2]	TS[1]	TS[0]	(00H)

TS[7:0]: Temperature boundary: -25C~60C

When TSFIX=1, Internal TS is disable, Temperature value will be set by TS[7:0].

TS[7:0]	Temperature (°C)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
…	…
1111_1110	-2
1111_1111	-1

TS[7:0]	Temperature (°C)
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
…	…
0011_1011	59
0011_1100	60

RFFH(TEST): TEST MODE Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	1	1	1	1	1	(FFH)
1st Parameter	W	1	data								(A5H)

Enter TEST MODE

TEST(0xFF)+Code(0xA5)=ENTER TEST MODE

TEST(0xFF)+Code(0xE3)=QUIT TEST MODE

RA8H(TEST): VDHROS_EN

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	0	1	0	1	0	0	0	(A8H)
1st Parameter	W	1	0	0	1	1	1	1	1	VDHROS EN	(3EH)

The offset enable signal of VDHR

Bit0	The offset enable signal of VDHR
0	ON(default)
1	OFF

RC3H(TEST): PWM EN Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	0	0	0	1	1	(C3H)
1st Parameter	W	1	1	1	PSTEP EN	1	1	1	PWEN	1	(FFH)

Bit1	PWEN : POWER PWM enable 0: follow REFH 1: follow default(default)
Bit5	PSTEPEN : GDR Driving enable 1:follow default(default) 0:follow RC9H

RC9H(TEST): GDROTP

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	0	1	0	0	1	(C9H)
1st Parameter	W	1			GDR_OTP_R						(00H)

Adjust the GDR driving for the three-stage voltage boosting during POWER ON and display refresh.

Bit5-4	GDR driving within BT_PHC and Display Refresh
Bit3-2	GDR driving within BT_PHB
Bit1-0	GDR driving within BT_PHA

RDAH(TEST): Driving Select

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	0	1	0	(DAH)
1st Parameter	W	1	0	0	0	0	1	VDHR SEL	VDH_SEL	VDL_SEL	(0FH)

Bit2	VDHR driving	0:weak	1:strong(default)
Bit1	VDH driving	0:weak	1:strong(default)
Bit0	VDL driving	0:weak	1:strong(default)

RDCH(TEST): CPCK SET enable

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	1	0	0	(DCH)
1st Parameter	W	1	0	0	0	0	0	0	CPCKDF EN	CPCKEN	(03H)

Bit0	CPCKEN : CPCK enable 0:OFF 1:ON(default)
Bit1	CPCKDFEN : CPCK PWH SET & CPCK PWL SET enable 1:follow default(default) 0:follow RDDH & RDEH

RDDH(TEST): CPCK PWH SET

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	1	0	1	(DDH)
1st Parameter	W	1	CPCK PWH SET								(08H)

Adjust the sampling frequency of VDH/VDL/VDHR clamping.

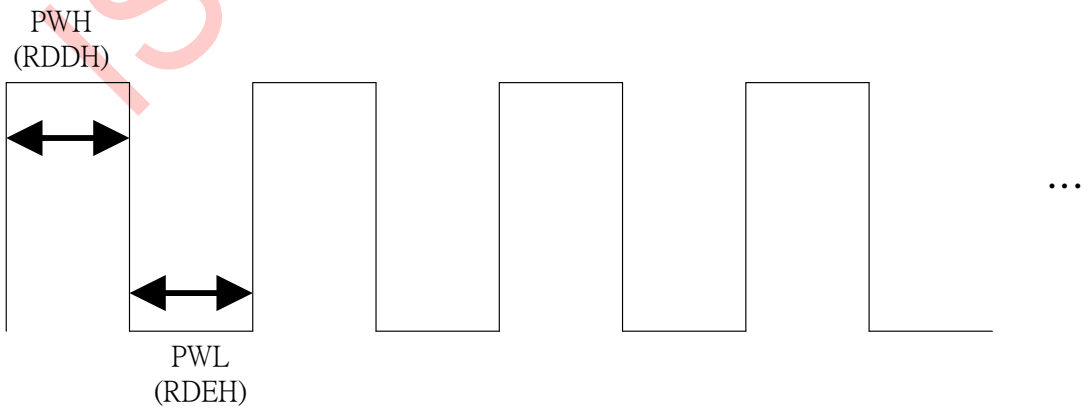
Bit7-0	
00H	0 ns
01H	125 ns
02H	250 ns
03H	375 ns
04H	500 ns
:	:
FCH	31500ns
FDH	31625ns
FEH	31750ns
FFH	31875ns

RDEH(TEST): CPCK PWL SET

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	0	1	1	1	1	0	(DEH)
1st Parameter	W	1	CPCK PWL SET								(08H)

Adjust the sampling frequency of VDH/VDL/VDHR clamping.

Bit7-0	
00H	0 ns
01H	125 ns
02H	250 ns
03H	375 ns
04H	500 ns
:	:
FCH	31500ns
FDH	31625ns
FEH	31750ns
FFH	31875ns



RE8H(TEST): VDLOS_Select

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	0	1	0	0	0	(E8H)
1st Parameter	W	1	0	0	0	0	0	0	VDLOS_SEL		(01H)

Bit1-0	Adjusting O.S. of VDL 00: strong 11:weak

RFDH(TEST): VDHOS_EN

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	1	1	1	0	1	(FDH)
1st Parameter	W	1	0	0	0	0	0	0	0	VDHOS EN	(00H)

The offset enable signal of VDH

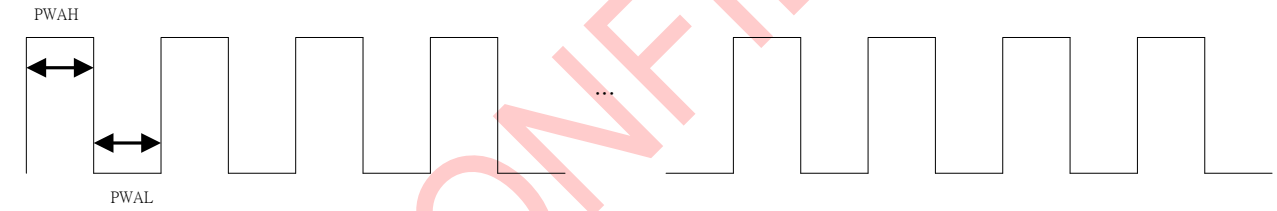
Bit0	The offset enable signal of VDH
0	OFF(default)
1	ON

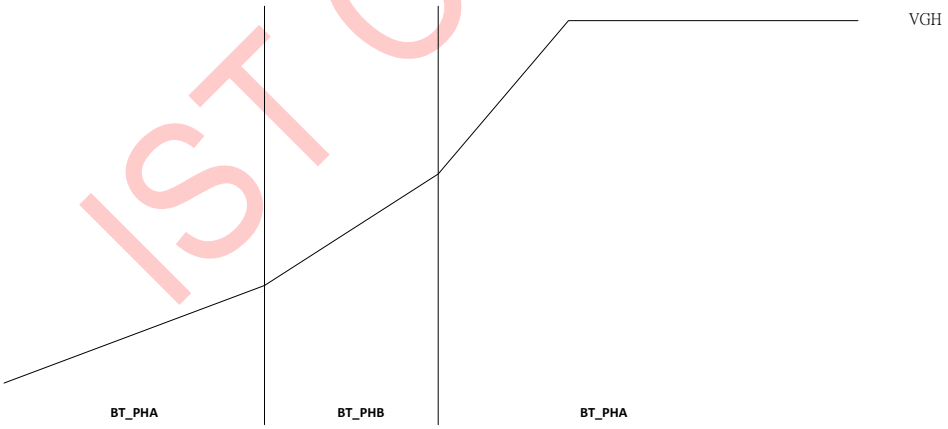
REFH(TEST_ POWER PWM):TEST__POWER PWM Register

Inst /Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	(Code)
TEST MODE	W	0	1	1	1	0	1	1	1	1	(EFH)
1st Parameter	W	1	BT_PWAH								(01H)
2st Parameter	W	1	BT_PWAL								(08H)
3st Parameter	W	1	BT_PWBH								(02H)
4st Parameter	W	1	BT_PWBL								(09H)
5st Parameter	W	1	BT_PWCH								(03H)
6st Parameter	W	1	BT_PWCL								(0AH)

1nd Parameter:

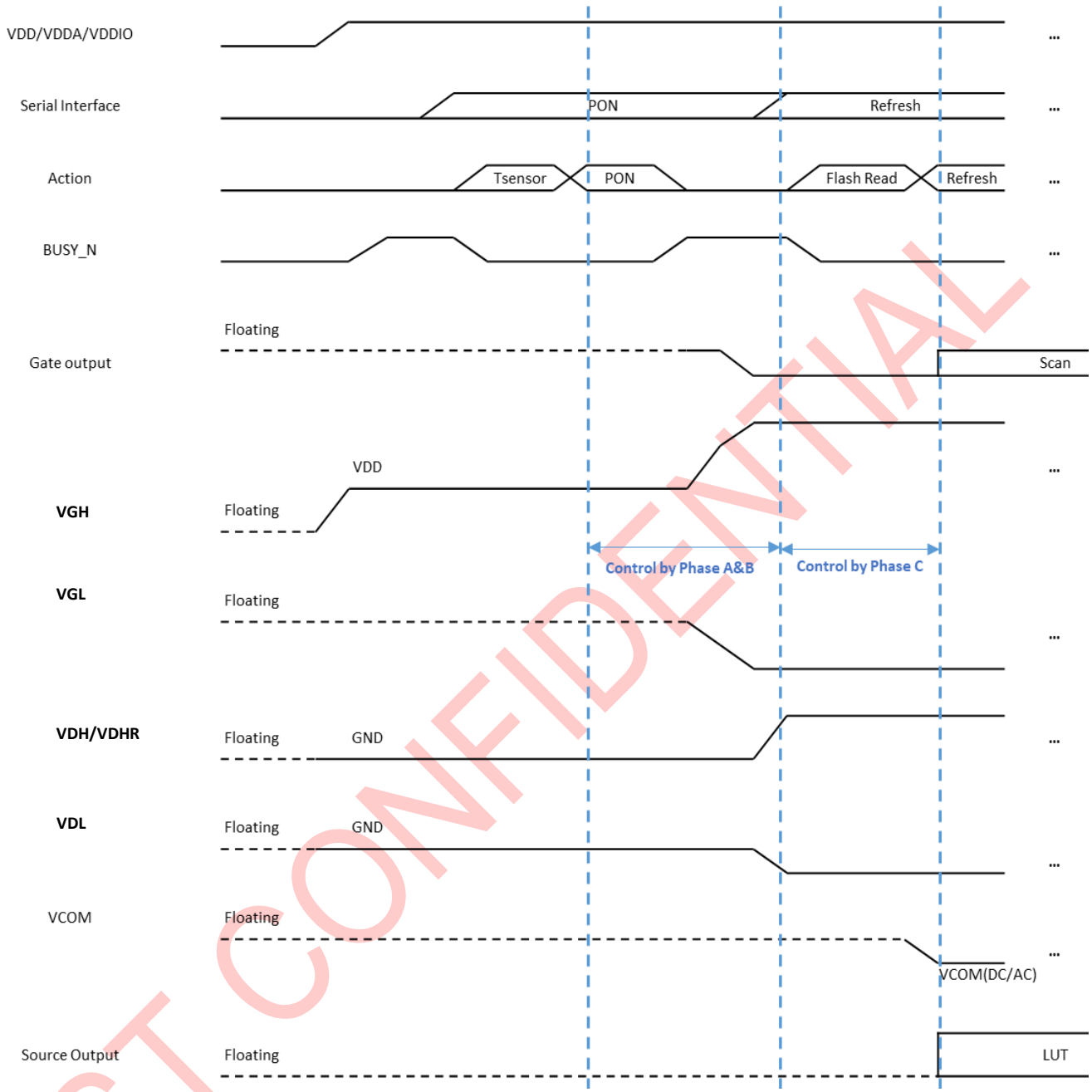
Bit7-0	PWxH/L time
00H	0 ns
01H	125 ns
02H	250 ns
03H	375 ns
04H	500 ns
:	:
FCH	31500ns
FDH	31625ns
FEH	31750ns
FFH	31875ns



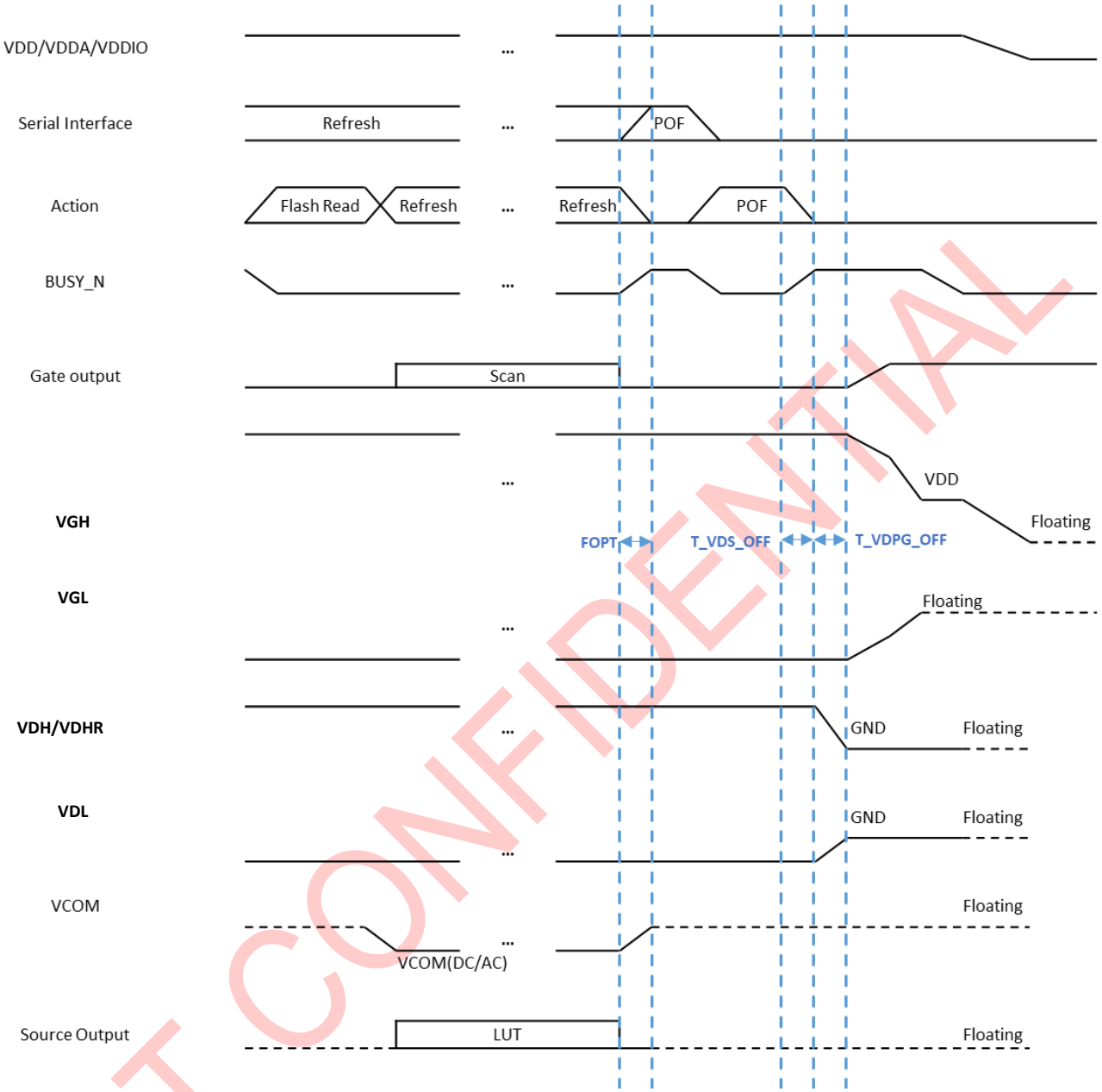


FUNCTION DESCRIPTION

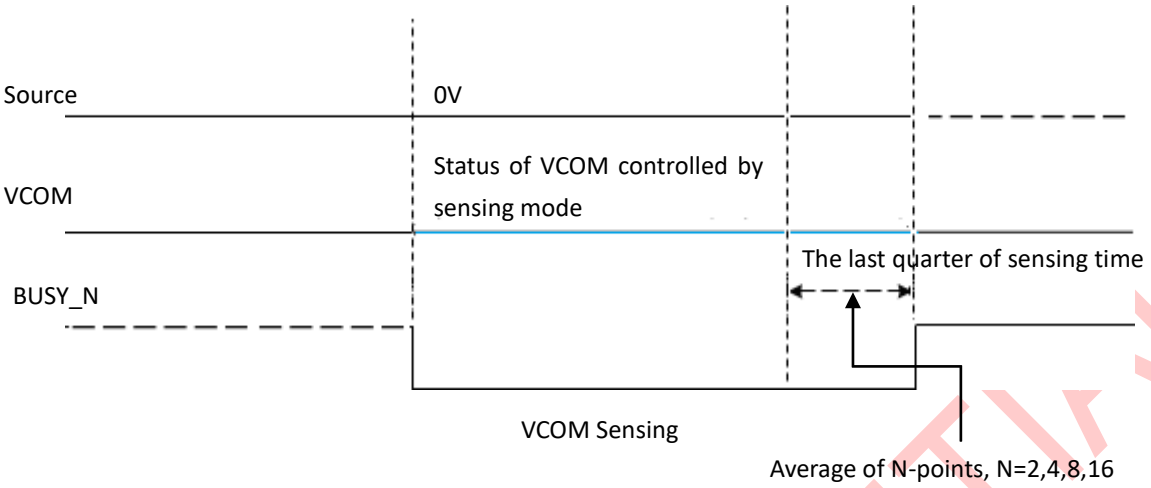
Power on sequence



Power off sequence



VCOM Sensing



ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Supply voltage range	VDDIO/VDD1/2/3/5	- 0.3 to 5	V
	VDDLI/VDDLO	- 0.3 to 2	V
	VGH	-0.3 to 20	V
	VGL	0.3 to -20	V
	VDH	-0.3 to 18	V
	VDL	0.3 to -18	V
	VDHR	-0.3 to 18	V
	VCOMDC	0.3 to -8	V
	VCOMAC (VCOMH)	-0.3 to VGH	V
	VCOMAC (VCOML)	0.3 to VGL	V
Input voltage range	VIN	-0.3 to VDDIO+0.3	V
Operating temperature range	TOPR	-30 to +85	℃
Storage temperature range	TSTR	-55 to +125	℃

NOTES:

VDDIO/VDD1/2/3/5/VDDLI/VDDLOand VGH/VGL/VDH/VDL/VDHR/VCOMDC/VCOMAC are based on VSS1/2/3/4/5 = 0V.

If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently.
It is desirable to use this LSI under electrical characteristic conditions during general operation.
Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

(Ta = -30 to 85℃)

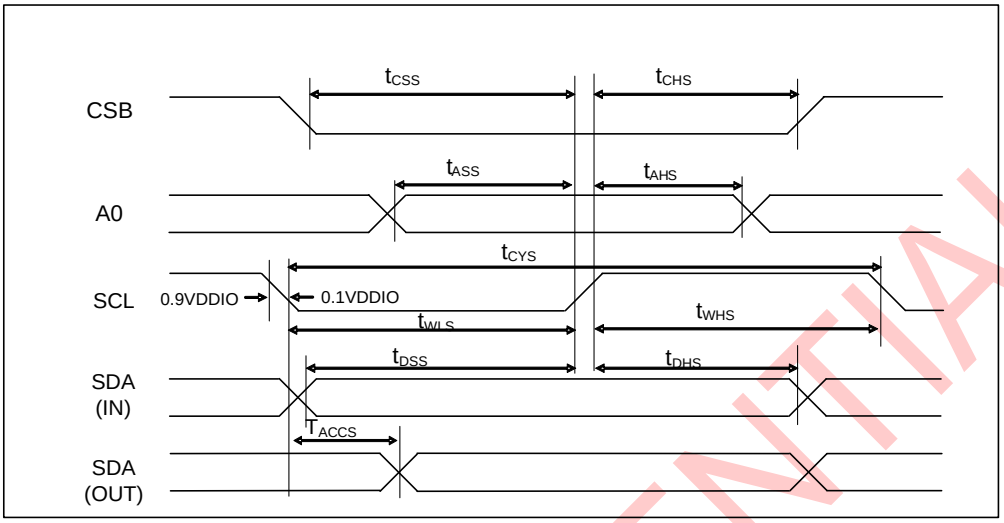
Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage		VDDIO		2.3	3.3	3.6	V
Supply Voltage		VDD1/2/3/5		2.3	3.3	3.6	V
Operation Voltage		VGH		10	-	20	V
Operation Voltage		VGL		-20	-	-10	V
Operation Voltage		VDH		3	-	15	V
Operation Voltage		VDHR		3	-	15	V
Operation Voltage		VDL		-15	-	-3	V
Operation Voltage		VCOMDC		-5	-	0	V
Operation Voltage		VCOMH		VDH+VCOMDC	-	VGH	V
Operation Voltage		VCOML		VGL	-	VDL+VCOMDC	V
Input Voltage	High	VIH		0.8*VDDIO	-	VDDIO	V
	Low	VIL		VSS1	-	0.2*VDDIO	
Output Voltage	High	VOH	IOUT = 1mA, VDDIO =2.4V	0.8*VDDIO	-	VDDIO	V
	Low	VOL	IOUT= -1mA, VDDIO =2.4V	VSS1	-	0.2*VDDIO	
Input Leakage Current		IIL	VIN= VDDIO or VSS1	-1.0	-	+1.0	μA
Driver Outputs ON Resistance		RON	Ta = 25℃, VDH=12V, VDL=-12V, VDHR=4V	-	-	10	kΩ
Oscillator Frequency (internal)		FOSC	Ta = 25℃	7.7	8.0	8.3	MHz
Refresh Current		IDD1 +IDD2 +IDD3 +IVDD5 +IDDIO+IVDDA (Refer to the specified Application Circuit of the following page)	Ta=25℃ VDDIO=VDD1/2/3/5=3V VGH=20V,VGL=-20V VDH=15V,VDL=-15V (include External circuit , no load)		1.5		mA
Deep Sleep Current		IVDD	Pattern no update, OSC off, VDD1/2/3/5=3.0V, Ta=25 ℃	-	1		uA(*1)

Note：

(*1) In Deep sleep mode, the SDA will be in Output state and to be pulledHighinternall to VDDIO. It's recommended MCU settingSDA as Hi-Z to avoid leakage.

AC CHARACTERISTICS

Serial Interface Characteristics



SPI Write(VDDIO=2.3 to 3.6V, Ta = -30 to +85℃)

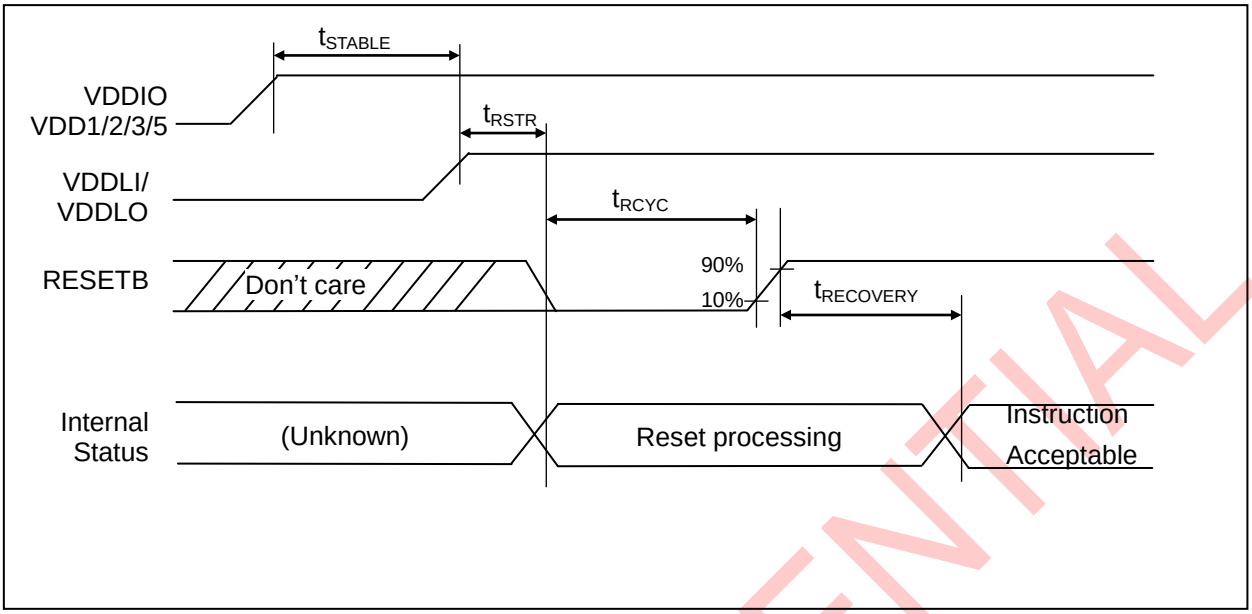
Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle	SCL	tcys	50	-	-	ns	
SCL high pulse width		twhs	25	-	-		
SCL low pulse width		twls	25	-	-		
Address setup time	A0	tass	5	-	-	ns	
Address hold time		tahs	5	-	-		
Data setup time	SDA	tdss	30	-	-	ns	
Data hold time		tdhs	30	-	-		
CSB setup time	CSB	tcss	60	-	-	ns	
CSB hold time		tchs	65	-	-		

SPI Read (VDDIO=2.3 to 3.6V, Ta = -30 to +85℃)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle	SCL	tcys	600	-	-	ns	
SCL high pulse width		twhs	150	-	-		
SCL low pulse width		twls	400	-	-		
Address setup time	A0	tass	90	-	-	ns	
Address hold time		tahs	90	-	-		
Read access time	SDA	taccS	-	-	200	ns	
CSB setup time	CSB	tcss	400	-	-	ns	
CSB hold time		tchs	150	-	-		

Note: All signal Rising time and falling Time <15ns

Reset Input Timing



(VDDIO=2.3 to 3.6V, VDD1/2/3/5 = 2.3 to 3.6V, Ta = -30 to +85℃)

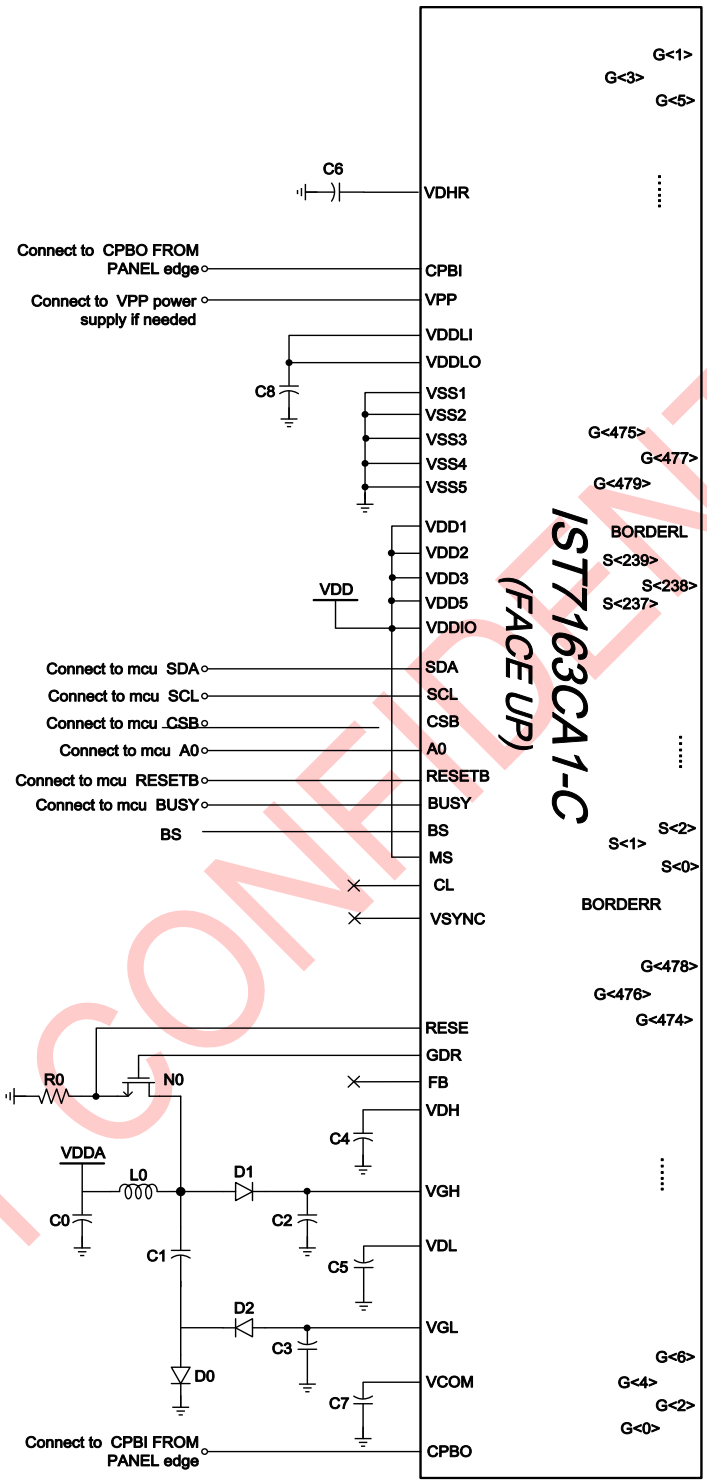
Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
VDDIO/VDD1/2/3/5 stable time	VDDIO VDD1/2/3/5	tSTABLE	10	-	-	ms	With external Cap (*1)
Reset start time	RESETB	tRSTR	0	-	-	us	
Reset cycle time	RESETB	tRCYC	1	-	-	ms	
Reset recovery time	RESETB	tRECOVERY	1	-	-	ms	(*2)

NOTE

*1. tSTABLE depending on different capacitance of Capconnect to VDDLI/VDDLO(external stabilizing capacitor), and It should be re-adjusted for different capacitance of the Cap connect to VDDLI/VDDLO.

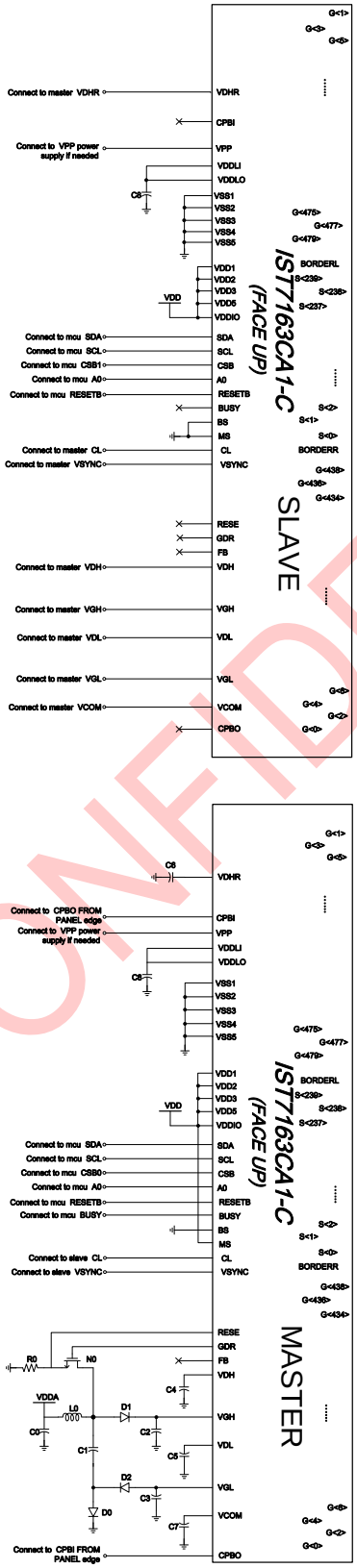
*2. After reset 1ms, it must check that the BSUY_N signal is high before the first instruction can be executed.

Application Circuit (Single chip)



Component	Item	Recommendation
Inductor	L0	10uH/47uH
Resistor	R0	0.47Ω/2.2Ω，0603/0805，1% variation
Capacitor	C0/ C1	1uF/4.7uF/25V，0603/0805，X5R/X7R
	C2/C3/C4	1uF/25V，0603/0805，X5R/X7R
	C5	1uF/25V，0805，X5R/X7R
	C6/ C7/C8	1uF/25V，0603/0805，X5R/X7R
Diode	D0/D1/D2	IF>= 2A
N-MOSFET	N0	ID>= 2A

Application Circuit (Master and Slave)



Note:

1. Slave initial code remove Power on command

2. Make sure Master and Slave use the same Lut-table

Component	Item	Recommendation
Inductor	L0	10uH/47uH
Resistor	R0	0.47Ω/2.2Ω，0603/0805，1% variation
Capacitor	C0/ C1	1uF/4.7uF/25V，0603/0805，X5R/X7R
	C2/C3/C4	1uF/25V，0603/0805，X5R/X7R
	C5	1uF/25V，0805，X5R/X7R
	C6/ C7/C8	1uF/25V，0603/0805，X5R/X7R
Diode	D0/D1/D2	IF>= 2A
N-MOSFET	N0	ID>= 2A

CAUTIONS:

1. This Specification will be subjected to modify without notice.
2. Precautions on Light:

Characteristics of semiconductor devices can be changed when exposed to light as described in the operational principles of solar batteries. Exposing this IC to light, therefore, can potentially lead to its malfunctioning.

2.1 Care must be exercised in designing the operation system and mounting the IC so that it may not be exposed light during operation.

2.2 Care must be exercised in designing the inspection process and handling the IC so that it may not be exposed to light during the process.

2.3 The IC must be shielded from light in the front, back and side faces.

3. ESD control and prevention:

3.1 Humidity Control: 30~70% relative humidity is recommended.

3.2 To reduce the risk of ESD, all equipment at the wok surface should be properly grounded and all sources of static fields removed.(Example: Station ionizers).

3.3 Grounding all personnel who come in contact with parts will eliminate a possible source of ESD. (Example: Wrist straps remove charge from the body and constitute a central part of ESD control).

4. Storage Conditions:

Before open package	After open package
Temp.=25±5℃ Humidity:50~70% Less than 1 Years	Temp.=25±5℃ Humidity:50~70% Less than 3 Months