GooDisplay

4.2 inch
E-paper Display Series
GDEY042F51

Dalian Good Display Co., Ltd.

GooDisplay®

Product Specifications

Customer	**Standard**
Description	**4.2" E-PAPER DISPLAY**
Model Name	**GDEY042F51**
Date	**2023 / 09 / 19**
Revision	**1.0**

	Design Engineering		
	Approval	**Check**	**Design**
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1. Over View

The GDEY042F51 is a display module featuring reflective electrophoretic technology, implemented on an active matrix TFT substrate. This panel has the capability to display images in black, white, yellow, and red, depending on the associated lookup table utilized. The panel's integrated circuitry includes a gate and source driver, timing controller, oscillator, DC-DC boost circuit, memory for frame buffer and lookup table storage, as well as additional circuitry to manage VCOM and BORDER settings.

2. Features

- Highlight Red and Yellow color
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I^2C signal master interface to read external temperature sensor
- Available in COG package

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	4.2	Inch	
Display Resolution	400(H)×300(V)	Pixel	Dpi:120
Active Area	84.8×63.6	mm	
Pixel Pitch	0.212×0.212	mm	
Pixel Configuration	Rectangle		
Outline Dimension	91(H)×77(V)×1.2(D)	mm	
Weight	16.09±0.05	g	

4. Mechanical Drawing of EPD module

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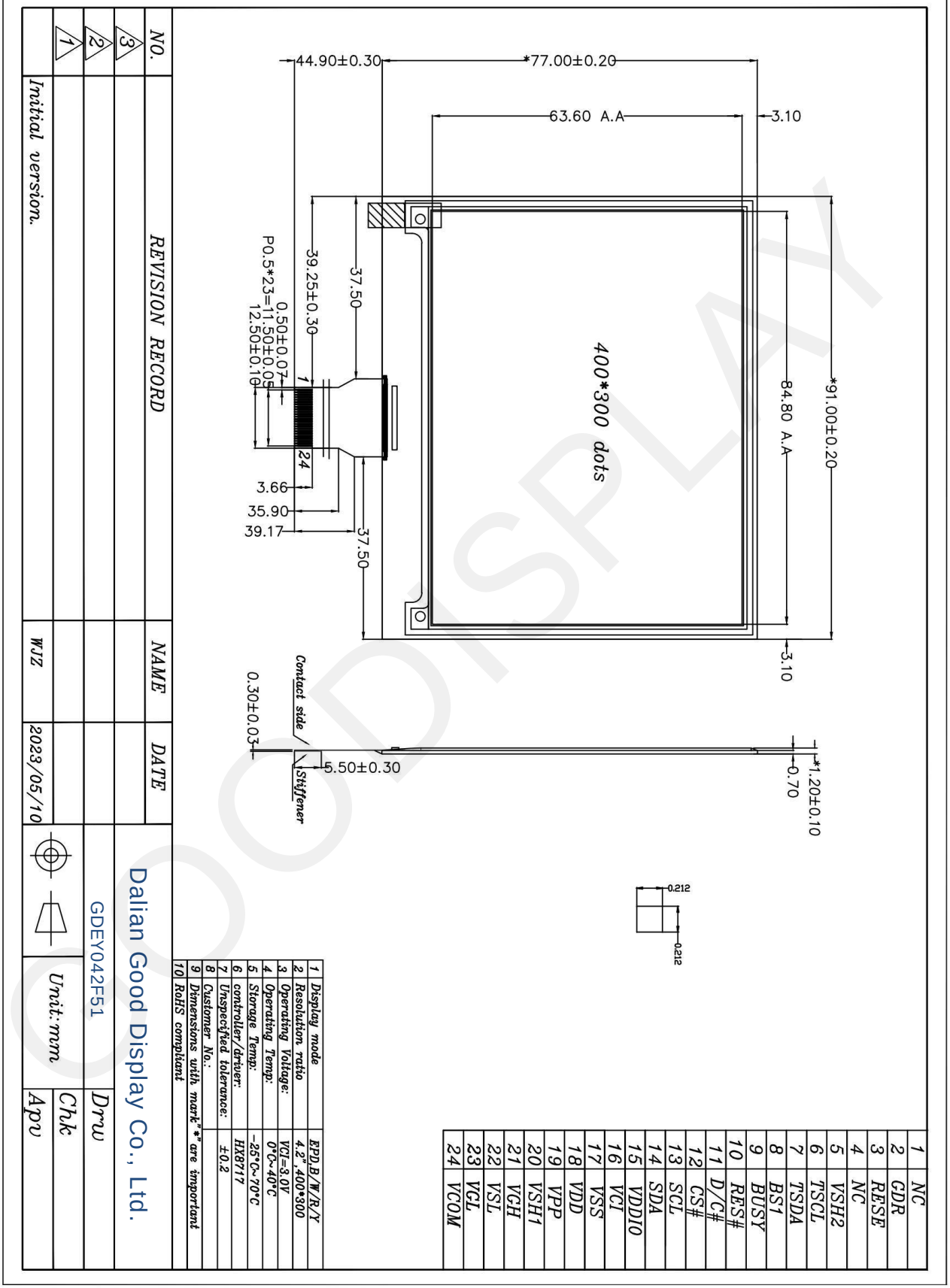

5. Input /Output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	This pin is N-MOS gate control.	
3	RESE	I	Current sense input for control loop.	
4	NC		Do not connect with other NC pins	Keep Open
5	VSH2	P	Positive source voltage	
6	TSCL	O	Leave it open if not used.	
7	TSDA	I/O	Leave it open if not used.	
8	BS1	I	Input interface setting.	
9	BUSY	O	This pin indicates the driver status.	
10	RES#	I	Global reset pin.	
11	D/C#	I	Serial communication Command/Data input.	
12	CS#	I	Serial communication chip select.	
13	SCL	I	Serial communication clock input.	
14	SDA	I/O	Serial communication data input.	
15	VDDIO	P	I/O power input.	
16	VCI	P	Digital/Analog power.	
17	VSS	P	Ground	
18	VDD	P	1.5V voltage input &output	
19	VPP	P	VPP for OTP programing. (8.25V)	
20	VSH1	P	Positive source voltage	
21	VGH	P	Positive gate voltage	
22	VSL	P	Negative Source driving voltage	
23	VGL	P	Negative gate voltage	
24	VCOM	O	VCOM driving voltage	

Note: I: Input, O: Output, P: Power, I/O: Input / Output.

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6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VDD VDDIO VDDA	-0.3 to +5.0	V
Digital input range	VI	-0.3 to VCI+0.3	V
Operating Temp range	TOPR	0 to +40	° C
Storage Temp range	TSTG	-25 to +70	° C
Optimal Storage Temp	TSTGo	23±2	° C
Optimal Storage Humidity	HSTGo	55±10	%RH

Note: (1) If ICs are stressed beyond those listed above "absolute maximum ratings", they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

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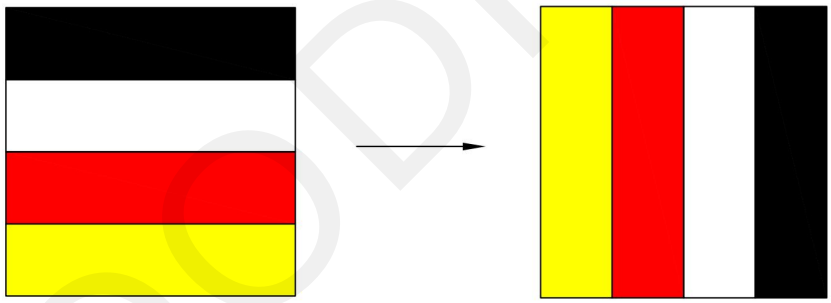
6.2 Panel DC Characteristics

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{CI}	-	VCI	2.3	3.3	3.6	V
Core logic voltage	V_{DD}		VDD	2.3	3.3	3.6	V
High level input voltage	V_{IH}	-	-	$0.8V_{CI}$	-	V_{CI}	V
Low level input voltage	V_{IL}	-	-	0	-	$0.2V_{CI}$	V
High level output voltage	V_{OH}	IOH = 400uA	-	$0.8V_{CI}$	-	V_{CI}	V
Low level output voltage	V_{OL}	IOL = -400uA	-	0	-	$0.2V_{CI}$	V
Typical power	P_{TYP}	V_{CI} =3.0V	-	-	26.4	-	mW
Deep sleep mode	P_{STPY}	V_{CI} =3.0V	-	-	0.006	-	mW
Typical operating current	Iopr_V_{CI}	V_{CI} =3.0V	-	-	8	-	mA
Image update time	-	25 ℃	-	-	28	-	sec
Stand-by current	Ist_V_{CI}		-	-	27	34	uA
Deep sleep mode current	Idslp_V_{CI}		-	-	1	5	uA

Notes: 1. The typical power is measured with following transition from horizontal 4 scale pattern to vertical 4 scale pattern.



2.The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3.The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display.

4.Electrical measurement：Multimeter

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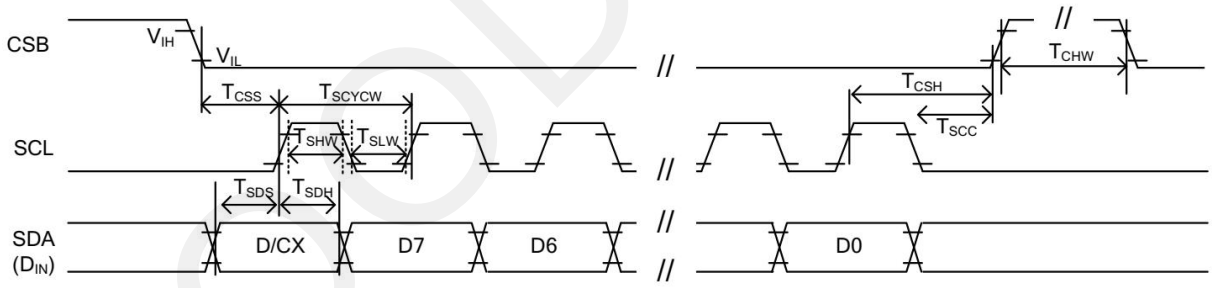
6.3 AC Characteristics

6.3.1 Display AC characteristics

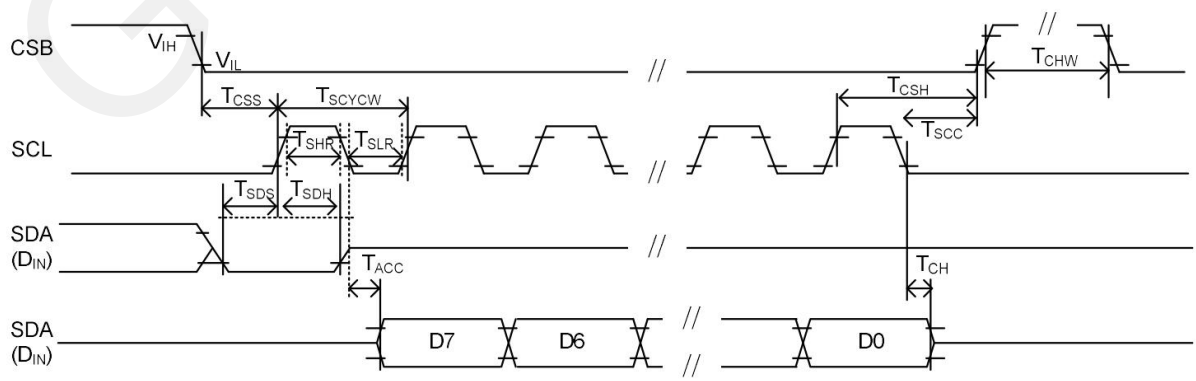
Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
OSC	F_{OSC}	IC Internal OSC	1.98	2	2.02	MHz
Frame Rate	F_{VSYNC}	Default frame rate **(400*300)**	49.5	50	50.5	Hz

6.3.2 3-wire AC characteristics

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
CSB	T_{CSS}	Chip select setup time	60	-	-	ns
	T_{CSH}	Chip select hold time	65	-	-	ns
	T_{SCC}	Chip select setup time	60	-	-	ns
	T_{CHW}	Chip select setup time	40	-	-	ns
SCL	T_{SCYCW}	Serial clock cycle **(Write)**	100	-	-	ns
	T_{SHW}	SCL "H" pulse width **(Write)**	35	-	-	ns
	T_{SLW}	SCL "L" pulse width **(Write)**	35	-	-	ns
	T_{SCYCR}	Serial clock cycle **(Read)**	150	-	-	ns
	T_{SHR}	SCL "H" pulse width **(Read)**	60	-	-	ns
	T_{SLR}	SCL "L" pulse width **(Read)**	60	-	-	ns
SDA (D_{IN})	T_{SDS}	Data setup time	30	-	-	ns
	T_{SDH}	Data hold time	30	-	-	ns
SDA (D_{OUT})	T_{ACC}	Access time	-	-	10	ns
	T_{OH}	Output disable time	15	-	-	ns



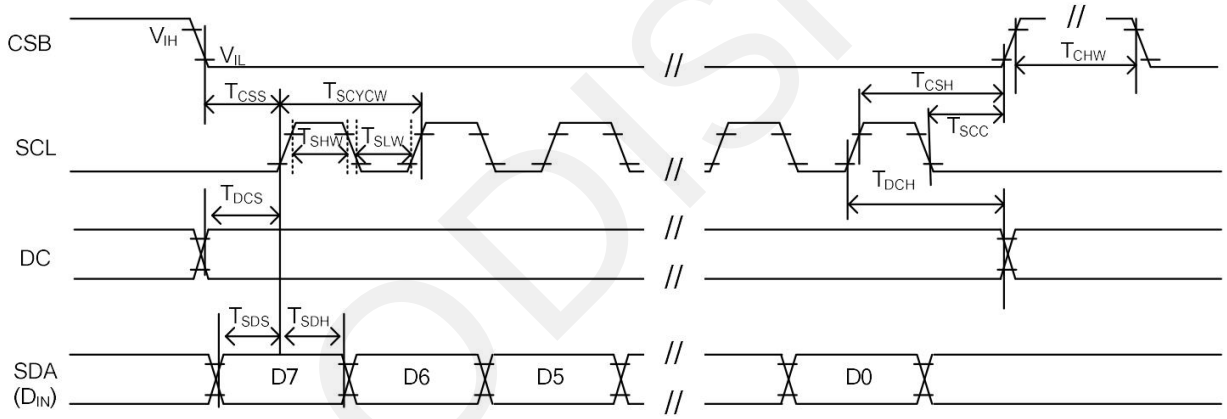
3-wire serial internal characteristics (write mode)



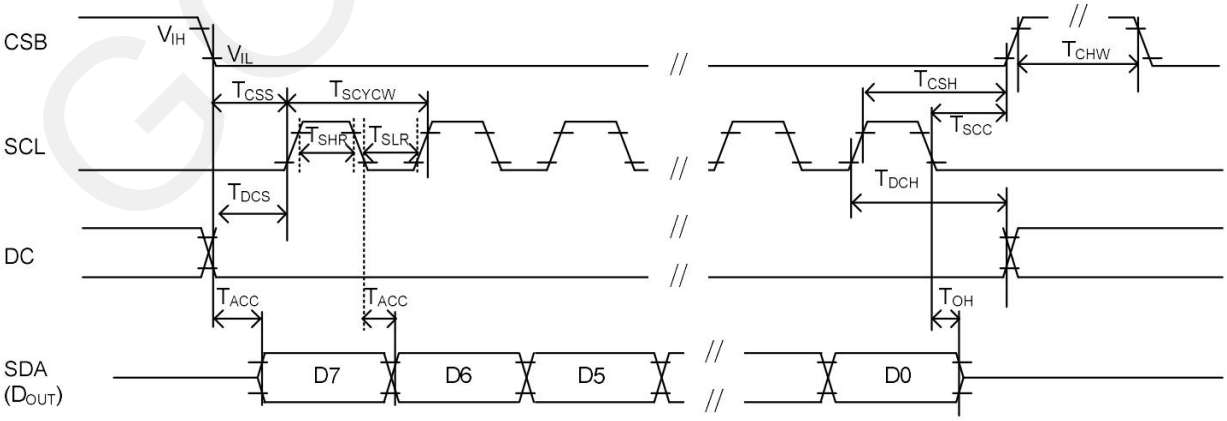
3-wire serial internal characteristics (read mode)

6.3.3 4-wire AC characteristics

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
CSB	T_{CSS}	Chip select setup time	60	-	-	ns
	T_{CSH}	Chip select hold time	65	-	-	ns
	T_{SCC}	Chip select setup time	60	-	-	ns
	T_{CHW}	Chip select setup time	40	-	-	ns
SCL	T_{SCYCW}	Serial clock cycle **(Write)**	100	-	-	ns
	T_{SHW}	SCL "H" pulse width **(Write)**	35	-	-	ns
	T_{SLW}	SCL "L" pulse width **(Write)**	35	-	-	ns
	T_{SCYCR}	Serial clock cycle **(Read)**	150	-	-	ns
	T_{SHR}	SCL "H" pulse width **(Read)**	60	-	-	ns
	T_{SLR}	SCL "L" pulse width **(Read)**	60	-	-	ns
DC	T_{DCS}	DC setup time	30	-	-	ns
	T_{DCH}	DC hold time	30	-	-	ns
SDA (D_{IN})	T_{SDS}	Data setup time	30	-	-	ns
	T_{SDH}	Data hold time	30	-	-	ns
SDA (D_{OUT})	T_{ACC}	Access time	-	-	50	ns
	T_{OH}	Output disable time	15	-	-	ns



4-wire serial internal characteristics (Write mode)



4-wire serial internal characteristics (Read mode)

7. Command Table

W/R: W: Write Cycle / **R:** Read Cycle
C/D: C: Command / **D:** Data
D[7:0]: –: Don't Care / **#:** Valid Data

Addr.(1)	Command(2)	W/R(3)	C/D	D[7:0](4)								Registers	Default
00h	Panel setting register **(PSR)**	W	C	0	0	0	0	0	0	0	0	-	00h
		W	D	#	#	#	-	#	#	#	#	RES[1:0], **PST_mode**, UD, SHL, SHD_N, RST_N	0Fh
		W	D	#	0	#	#	#	#	#	#	LUT_EN, FOPT, VCMZ, TS_AUTO, TIEG, NORG, VC_LUTZ	09h
01h	Power setting register **(PWR)**	W	C	0	0	0	0	0	0	0	1	-	01h
		W	D	-	-	-	-	-	#	#	#	VSC_EN, VS_EN, VG_EN	0Fh
		W	D	-	-	-	-	-	-	#	#	VGPN [1:0]	00h
		W	D	-	#	#	#	#	#	#	#	(Power Mode0) VSPL [6:0]	00h
		W	D	-	#	#	#	#	#	#	#	(Power Mode1) VSPH [6:0]	00h
		W	D	-	#	#	#	#	#	#	#	(Power Mode1) VSN [6:0]	00h
		W	D	-	#	#	#	#	#	#	#	(Power Mode01) VSPL [6:0]	00h
02h	Power off **(POF)**	W	C	0	0	0	0	0	0	1	0	-	02h
		W	D	-	-	-	-	-	-	-	#	EDSE	00h
03h	Power on/off sequence setting **(POFS)**	W	C	0	0	0	0	0	0	1	1	-	03h
		W	D	-	-	#	#	-	-	#	#	T_VDPG_OFF[1:0], T_VDS_OFF[1:0]	00h
		W	D	#	#	#	#	#	#	#	#	VGH_LEN[3:0], VGH_EXT[3:0]	54h
		W	D	#	#	#	#	#	#	#	#	XON_DLY[3:0], XON_LEN[3:0]	44h
04h	Power on **(PON)**	W	C	0	0	0	0	0	1	0	0	-	04h
06h	booster soft start **(BTST)**	W	C	0	0	0	0	0	1	1	0	-	06h
		W	D	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17h
		W	D	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17h
		W	D	-	-	#	#	#	#	#	#	BT_PHC[5:0]	17h
07h	Deep sleep **(DSLP)**	W	C	0	0	0	0	0	1	1	1	-	07h
		W	D	1	0	1	0	0	1	0	1	Check code	00h
10h	Display start transmission **(DTM)**	W	C	0	0	0	1	0	0	0	0	Pixel data	10h
		W	D	#	#	#	#	#	#	#	#	Pixel1, Pixel2, Pixel3, Pixel4	00h
		W	D	-	:	:	:	-	:	:	:	:	00h
		W	D	#	#	#	#	#	#	#	#	Pixel(n-3), Pixel(n-2), Pixel(n-1), Pixe(n)	00h
11h	Data stop **(DSP)**	W	C	0	0	0	1	0	0	0	1	-	11h
		R	D	#	-	-	-	-	-	-	-	Data_flag	00h
12h	Display refresh **(DRF)**	W	C	0	0	0	1	0	0	1	0	-	12h
		W	D	-	-	-	-	-	-	-	#	AC/DC VCOM	00h
17h	Auto sequence **(AUTO)**	W	C	0	0	0	1	0	1	1	1	-	17h
		W	D	1	0	1	0	0	1	0	1	Check code	00h
30h	PLL control **(PLL)**	W	C	0	0	1	1	0	0	0	0	-	30h
		W	D	-	-	-	-	#	#	#	#	Dyna, FR[2:0]	02h
40h	Temperature sensor command **(TSC)**	W	C	0	1	0	0	0	0	0	0	-	40h
		R	D	#	#	#	#	#	#	#	#	D[10:3] / TS[7:0]	00h
		R	D	#	#	#	-	-	-	-	-	D[2:0]	00h
41h	Temperature sensor enable **(TSE)**	W	C	0	1	0	0	0	0	0	1	-	41h
		W	D	#	-	-	-	#	#	#	#	TSE, TO[3:0]	00h
50h	VCOM and data interval setting **(CDI)**	W	C	0	1	0	1	0	0	0	0	-	50h
		W	D	#	#	#	#	#	#	#	#	VBD[2:0], DDX, CDI[3:0]	97h
51h	Lower power detection **(LPD)**	W	C	0	1	0	1	0	0	0	1	-	51h
		R	D	-	-	-	-	-	-	-	#	LPD	01h

Reg[1]	Command[2]	W/R[3]	C/D	D[7:0][4]								Registers	Default
61h	Resolution setting **(TRES)**	W	C	0	1	1	0	0	0	0	1	-	61h
		W	D	-	-	-	-	-	-	#	#	VRES[9:8]	00h
		W	D	#	#	#	#	#	#	#	#	VRES[7:0]	00h
		W	D	-	-	-	-	-	-	#	#	VRES[9:8]	00h
		W	D	#	#	#	#	#	#	#	#	VRES[7:0]	00h
70h	Chip revision **(REV)**	W	C	0	1	1	1	0	0	0	0	-	70h
		R	D	0	0	0	0	0	1	1	0	REV	06h
		R	D	#	#	#	#	#	#	#	#	REV1[7:0]	05h
		R	D	#	#	#	#	#	#	#	#	REV2[7:0]	01h
80h	Auto measurement VCOM **(AMV)**	W	C	1	0	0	0	0	0	0	0	-	80h
		W	D	#	#	#	#	#	#	#	#	P[1:0], AMVT[1:0], AMVX, AMVS, AMV, AMVE	00h
		W	D	#	#	#	#	#	#	#	#	AMVP2	-
81h	VCOM value **(VV)**	W	C	1	0	0	0	0	0	0	1	-	81h
		R	D	-	#	#	#	#	#	#	#	VV[6:0]	00h
82h	VCOMDC setting **(VDCS)**	W	C	1	0	0	0	0	0	1	0	-	82h
		W	D	#	#	#	#	#	#	#	#	OTP_VCM ,VDCS[6:0]	00h
83h	Partial window **(PTLW)**	W	C	1	0	0	0	0	0	1	1	-	83h
		W	D	-	-	-	-	-	-	-	#	HRST[9:8]	00h
		W	D	#	#	#	#	#	#	0	0	HRST[7:0]	00h
		W	D	-	-	-	-	-	-	-	#	HRED[9:8]	00h
		W	D	#	#	#	#	#	#	1	1	HRED[7:0]	03h
		W	D	-	-	-	-	-	-	-	#	VRST[9:8]	00h
		W	D	#	#	#	#	#	#	#	#	VRST[7:0]	00h
		W	D	-	-	-	-	-	-	-	#	VRED[9:8]	00h
		W	D	#	#	#	#	#	#	#	#	VRED[7:0]	00h
		W	D	-	-	-	-	-	-	-	#	PMODE	00h
90h	Program mode **(PGM)**	W	C	1	0	0	1	0	0	0	0	-	90h
91h	Active program **(APG)**	W	C	1	0	0	1	0	0	0	1	-	91h
92h	Read OTP data **(ROTP)**	W	C	1	0	0	1	0	0	1	0	-	92h
		R	D	-	-	-	-	-	-	-	-	Dummy	00h
		R	D	#	#	#	#	#	#	#	#	OTP data of address 0	00h
		R	D	:	:	:	:	:	:	:	:	:	00h
		R	D	#	#	#	#	#	#	#	#	OTP data of address n	00h
E3h	Power saving **(PWS)**	W	C	1	1	1	0	0	0	1	1	-	E3h
		W	D	#	#	#	#	#	#	#	#	VCOM_W[3:0], SD_W[3:0]	00h
E4h	LVD voltage select **(LVSEL)**	W	C	1	1	1	0	0	1	0	0	-	E4h
		W	D	-	-	-	-	-	-	#	#	LVD_SEL[1:0]	03h

Note: (1) All other register addresses are invalid or reserved by Himax and should not be used.
(2) Commands are processed on the 'stop' condition of the interface.
(3) Registers marked 'W/R' can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.
(4) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PSR	W	C	0	0	0	0	0	0	0	0	00h
1st parameter	W	D	RES [1:0]		PST_mode	-	UD	SHL	SHD_N	RST_N	0Fh
2nd parameter	W	D	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h

Description

1st parameter:

RES[1:0]	Bit[7:6]:Resolution setting	Note
00	Display resolution is 400x300	Default
01	Display resolution is 300x300	-
10	Display resolution is 256x256	-
11	Display resolution is 128x128	-

PST_mode	Bit[5]:Power switching operation mode	Note
0	Power switching time in the period of frame scanning	Default
1	Power switching time in the external period before frame scanning	-

UD	Bit[3]: UD select	Note
0	Scan down, first line=G[n-1] →…→ G1 → Last line=G0	-
1	Scan up, first line=G[0] → G1 → … → Last line=G[n-1]	Default

SHL	Bit[2]: SHL select	Note
0	Shift left, first data= S[n-1] → …→ S1→ Last data=S0	-
1	Shift right, first data=S0 → S1 → …→ Last data=S[n-1]	Default

SHD_N	Bit[1]: Shutdown	Note
0	Booster OFF, register data are kept, and Source/Border/VCOM are kept 0V or floating	-
1	Booster ON	Default

RST_N	Bit[0]: Reset	Note
0	Booster OFF. Register data are set to their default values, and Source/Border/VCOM: 0V	-
1	NO effect	Default

2nd parameter:

LUT_EN	Bit[7]: LUT enable	Note
0	LUT from OTP	Default
1	LUT from register	-

FOPT	Bit[5]: FOPT select	Note
0	Scan 1 frame after waveform finished	Default
1	No Scan after waveform finished, and switch the source channel output to Hi-Z	-

VCMZ	Bit[4]: VCOM Hi-Z	Note
0	NO effect	Default
1	VCOM is always floating	-

TS_AUTO	Bit[3]: Temperature Auto	Note
0	NO effect	-
1	After system reset, Temperature Sensor will be activated automatically one time	Default

TIEG	Bit[2]: Tie to GND select	Note
0	NO effect	Default
1	After power off booster, VGL will be tied to GND	-

NORG	Bit[1]:NORG function	Note
0	NO effect	Default
1	After refreshing display, VCOM is tied to GND before power off	-

VC_LUTZ	Bit[0]: VCOM Hi-Z after DRF	Note
0	NO effect	-
1	After refreshing display, the output of VCOM is set to floating automatically	Default

Priority of VCOM setting: VCMZ > NORG > FOPT > VC_LUTZ.
FOPT setting is part of refreshing display.

A. Non-select gate line keeps at VGL for DSP/DRF and AMV.
B. Inactive source line follows LUTC for DSP/DRF.
C. When SHD_N become low, Booster will turn off. Register and SRAM data will keep until VDD off. SD output and VCOM will base on previous condition. It may have two conditions: 0V or floating.
D. When RST_N become low, driver will reset. All register will reset to default value. Driver all function will disable. Source/Gate/Border/VCOM will be released to floating.

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWR	W	C	0	0	0	0	0	0	0	1	01h
1st parameter	W	D		-	-	-	-	VSC_EN	VS_EN	VG_EN	0Fh
2nd parameter	W	D	-	-	-	-	-	-	VGPN [1:0]		00h
3rd parameter	W	D	-	**(Power Mode0)** VSPL [6:0]							00h
4th parameter	W	D		**(Power Mode1)** VSPH [6:0]							00h
5th parameter	W	D	-	**(Power Mode1)** VSN [6:0]							00h
6th parameter	W	D	-	**(Power Mode1)** VSPL [6:0]							00h

Description

The command define as follows:

1st parameter:

VSC_EN	Bit[2]:Source LV power selection	Note
0	External source LV power from VSPL pins	-
1	Internal DC/DC function for generate VSPL	Default

VS_EN	Bit[1]:Source power selection	Note
0	External source power from VSPH/ VSN pins	-
1	Internal DC/DC function for generate VSPH/ VSN	Default

VG_EN	Bit[1]:Gate power selection	Note
0	External gate power from VGH/VGL pins	-
1	Internal DCDC function for generate VGH/VGL	Default

2nd parameter:

VGPN [1:0]	Bit[1:0]:VGPN voltage(1) level	Note
00	VGH=20V, VGL= -20V	Default
01	VGH=17V, VGL= -17V	-
10	VGH=15V, VGL= -15V	-
11	VGH=10V, VGL= -10V	-

Notes: (1) If VGPN voltage is set to ±17V, ±15V, ±10V, IC will auto correct source voltage as follows.
A. VGH-VSPH/VSPL≧2V.
B. VGL-VSN≧-2V.

For example:

	Symbol	Voltage setting	Real voltage
Voltage	VGH	+10V	+10V
	VGL	-10V	-10V
	VSPH	+15V	+8V
	VSN	-15V	-8V
	VSPL	+5V	+5V
	VCOMH	+15V+(-2V)	+8V+(-2V)
	VCOML	-15V+(-2V)	-8V+(-2V)
	VCOMDC	-2V	-2V

Power mode 0:

VSPH = 15V **(0x78)**
VSN = -15V **(0x78)**
3rd Parameter: Internal VSPL power selection **(Default value: 0000000)(3V~15V)**

Power mode 1:
4th & 6th Parameter: Internal VSPH/VSPL power selection **(Default value: 0000000) (3V~15V)**
5th Parameter: Internal VSN power selection **(Default value: 0000000) (-3V~-15V)**

Bit[6:0]	Internal VSPH/VSPL Power	Internal VSN Power	Bit[6:0]	Internal VSPH/VSPL Power	Internal VSN Power
0000000	3 V	-3 V	0110010	8.0 V	-8.0 V
0000001	3.1 V	-3.1 V	:	:	:
0000010	3.2 V	-3.2 V	0111100	9.0 V	-9.0 V
0000011	3.3 V	-3.3 V	:	:	:
0000100	3.4 V	-3.4 V	1000110	10.0 V	-10.0 V
0000101	3.5 V	-3.5 V	:	:	:
0000110	3.6 V	-3.6 V	1010000	11.0 V	-11.0 V
0000111	3.7 V	-3.7 V	:	:	:
0001000	3.8 V	-3.8 V	1011010	12.0 V	-12.0 V
0001001	3.9 V	-3.9 V	:	:	:
0001010	4.0 V	-4.0 V	1100100	13.0 V	-13.0 V
0001011	4.1 V	-4.1 V	:	:	:
0001100	4.2 V	-4.2 V	1101110	14.0 V	-14.0 V
0001101	4.3 V	-4.3 V	:	:	:
0001110	4.4 V	-4.4 V	1111000	15.0 V	-15.0 V
0001111	4.5 V	-4.5 V	-	-	-
0010000	4.6 V	-4.6 V	-	-	-
:	:	:	-	-	-
0010100	5.0 V	-5.0 V	-	-	-
:	:	:	-	-	-
0011110	6.0 V	-6.0 V	-	-	-
:	:	:	-	-	-
0101000	7.0 V	-7.0 V	-	-	-
:	:	:	-	-	-

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
POF	W	C	0	0	0	0	0	0	1	0	02h
1st parameter	W	D	-	-	-	-	-	-	-	EDSE	00h

Description

The command define as follows:
After the power off command, the driver will power off based on power off sequence.
After the power off command, BUSY_N signal will become '0".
This command will turn off charge pump, T-con, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned off.
SD output and VCOM will base on previous condition.
It may have two conditions:0V or floating

EDSE	Bit[0]:EPD Discharge Trigger	Note
0	Disable EPD discharge	Default
1	Enable EPD discharge	-

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
POFS	W	C	0	0	0	0	0	0	1	1	03h
1st parameter	W	D	-		T_VDPG_OFF[1:0]		-		T_VDS_OFF[1:0]		00h
2nd parameter	W	D	VGH_LEN[3:0]				VGH_EXT[3:0]				54h
3rd parameter	W	D	XON_DLY[3:0]				XON_LEN[3:0]				44h

Description

The 2nd ~3rd parameters are only for EPD discharge function. **(EDSE)**
1st parameter and 2nd ~3rd parameter would not happen at the same time.

1st parameter:

T_VDPG_OFF[1:0]	Bit[5:4]:Power off sequence of VGH and VGL	Note
00	20ms	Default
01	40ms	-
10	60ms	-
11	80ms	-

T_VDS_OFF[1:0]	Bit[1:0]:Power off sequence of VSPH/ VSPL and VSN	Note
00	20ms	Default
01	40ms	-
10	60ms	-
11	80ms	-

2nd parameter:

VGH_LEN[3:0]	Bit[7:4]:VGH power on time	VGH_EXT[3:0]	Bit[3:0]:VGH extension time
0000	0ms	0000	0ms
0001	500ms	0001	500ms
0010	1000ms	0010	1000ms
0011	1500ms	0011	1500ms
0100	2000ms	0100	2000ms **(Default)**
0101	2500ms **(Default)**	0101	2500ms
0110	3000ms	0110	3000ms
0111	3500ms	0111	3500ms
1000	4000ms	1000	4000ms
1001	4500ms	1001	4500ms
1010	5000ms	1010	5000ms
1011	5500ms	1011	5500ms
1100	6000ms	1100	6000ms
1101	6500ms	1101	6500ms

3rd parameter:

XON_DLY[3:0]	Bit[7:4]XON delay time	XON_LEN[3:0]	Bit[3:0]XON enable time
0000	0ms	-	0ms
0001	500ms	0001	500ms
0010	1000ms	0010	1000ms
0011	1500ms	0011	1500ms
0100	2000ms **(Default)**	0100	2000ms **(Default)**
0101	2500ms	0101	2500ms
0110	3000ms	0110	3000ms
0111	3500ms	0111	3500ms
1000	4000ms	1000	4000ms
1001	4500ms	1001	4500ms
1010	5000ms	1010	5000ms
1011	5500ms	1011	5500ms
1100	6000ms	1100	6000ms

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PON	W	C	0	0	0	0	0	1	0	0	04h
Description	The command define as follows: After power on command, the driver will power ON base on Power ON sequence. After power on command and all power sequence are ready **(Based on PWR command)**, then BUSY_N signal will become 1. This command only active when BUSY_N=1.										

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BTST	W	C	0	0	0	0	0	1	1	0	06h
1st parameter	W	D	BT_PHA[7:6]		BT_PHA[5:3]			BT_PHA[2:0]			17h
2nd parameter	W	D	BT_PHB[7:6]		BT_PHB[5:3]			BT_PHB[2:0]			17h
3rd parameter	W	D	-	-	BT_PHC[5:0]			BT_PHC[2:0]			17h

Description

The command define as follows:

1st parameter:

BT_PHA[7:6]	Bit[7:6]:Soft start period of phase A	Note
00	10ms	Default
01	20ms	-
10	30ms	-
11	40ms	-

BT_PHA[5:3]	Bit[5:3]:Driving strength of phase A	Note
000	Strength 1	-
001	Strength 2	-
010	Strength 3	Default
011	Strength 4	-
100	Strength 5	-
101	Strength 6	-
110	Strength 7	-
111	Strength 8	Strongest

BT_PHA[2:0]	Bit[2:0]:Min. off time setting of GDR in phase A	Note
000	0.27μs	-
001	0.34μs	-
010	0.40μs	-
011	0.54μs	-
100	0.80μs	-
101	1.54μs	-
110	3.34μs	-
111	6.58μs	Default

2nd parameter:

BT_PHB[7:6]	Bit[7:6]:Soft start period of phase B	Note
00	10ms	Default
01	20ms	-
10	30ms	-
11	40ms	-

BT_PHB[5:3]	Bit[5:3]:Driving strength of phase B	Note
000	Strength 1	-
001	Strength 2	-
010	Strength 3	Default
011	Strength 4	-
100	Strength 5	-
101	Strength 6	-
110	Strength 7	-
111	Strength 8	Strongest

BT_PHB[2:0]	Bit[2:0]:Min. off time setting of GDR in phase B	Note
000	0.27μs	-
001	0.34μs	-
010	0.40μs	-
011	0.54μs	-
100	0.80μs	-
101	1.54μs	-
110	3.34μs	-
111	6.58μs	Default

GOODISPLAY

3rd parameter:

BT_PHC[5:3]	Bit[5:3]:Driving strength of phase C	Note
000	Strength 1	-
001	Strength 2	-
010	Strength 3	Default
011	Strength 4	-
100	Strength 5	-
101	Strength 6	-
110	Strength 7	-
111	Strength 8	Strongest

BT_PHC[2:0]	Bit[2:0]:Min. off time setting of GDR in phase C	Note
000	0.27μs	-
001	0.34μs	-
010	0.40μs	-
011	0.54μs	-
100	0.80μs	-
101	1.54μs	-
110	3.34μs	-
111	6.58μs	Default

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DSLP	W	C	0	0	0	0	0	1	1	1	07h
1st parameter	W	D	0	0	0	0	0	0	0	0	00h
Description	The command define as follows: After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset. The only one parameter is a check code, the command would be executed if check code=0xA5.										

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DTM	W	C	0	0	0	1	0	0	0	0	10h
1st parameter	W	D	Pixel1		Pixel2		Pixel3		Pixel4		00h
:	W	D	:		:		:		:		00h
Mth parameter	W	D	Pixel(n-3)		Pixel(n-2)		Pixel(n-1)		Pixel(n)		00h

Description

The command define as follows:
This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a Data Refresh command. Then the chip will start to send data/VCOM for panel.

Pixel[1~n][1:0] **(2-bit mode):**

	Source output look up table			
Image Data	DDX=1 (Default)		DDX=0	
Pixel[1:0]	Gray level select	IP output LUT select	Gray level select	IP output LUT select
00	Gray 0	ogray00	Gray 3	ogray03
01	Gray 1	ogray01	Gray 2	ogray02
10	Gray 2	ogray02	Gray 1	ogray01
11	Gray 3	ogray03	Gray 0	ogray00

Data mapping example:
When DDX=1, Pixel[1:0]=01->Gray level select= Gray 1, follow LUT data output from IP output port"ogray01"
When DDX=0, Pixel[1:0]=11->Gray level select= Gray 0, follow LUT data output from IP output port"ogray00"

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DSP	W	C	0	0	0	1	0	0	0	1	11h
1st parameter	R	D	Data_flag	-	-	-	-	-	-	-	00h

Description

The command define as follows:
To stop data transmission, this command must be issued to check the Data_flag.

1st parameter:

Data_flag	Bit[7]:Data flag of receiving user data
0	Driver didn't receive all the data.
1	Driver has already received all the one frame data.

After "Data stop" **(R11h)** commands and when Data_flag=1, BUSY_N signal will become 0 and the refreshing of panel starts.

This command only active when BUSY_N=1.

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DRF	W	C	0	0	0	1	0	0	1	0	12h
1st parameter	W	D	-	-	-	-	-	-	-	AC/DC VCOM	00h
Description	The command define as follows: While user sent this command, driver will refresh display **(Data/VCOM)** base on SRAM data and LUT. **AC/DC VCOM:** AC, DC VCOM select. 0: AC VCOM, VCOM will follow LUTC when updating image. **(Default)** 1: DC VCOM, VCOM will always be VCOMDC when updating image. After display refresh command, BUSY_N signal will become 0. This command only active when BUSY_N=1.										

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
AUTO	W	C	0	0	0	1	0	1	1	1	17h
1st parameter	W	D	0	0	0	0	0	0	0	0	00h
Description	The command define as follows: The command is only for LUT from register mode **(R00h LUT_EN=1)** only. The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP. AUTO (0x17) + Code (0xA5) = (PON → DRF → POF) AUTO (0x17) + Code (0xA7) = (PON → DRF → POF → DSLP)										

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PLL	W	C	0	0	1	1	0	0	0	0	30h
1st parameter	W	D	-	-	-	-	Dyna	FR[2:0]			02h

Description

The command define as follows:
The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

Dyna	Dynamic frame rate	Note
0	Disable	Default
1	Enable	-

FR[2:0]	Bit[2:0]:Frame rate	Note
000	12.5Hz	-
001	25Hz	-
010	50Hz	Default
011	65Hz	-
100	75Hz	-
101	85Hz	-
110	100Hz	-
111	120Hz	-

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TSC	W	C	0	1	0	0	0	0	0	0	40h
1st parameter	R	D	TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0	00h
2nd parameter	R	D	-	-	-	-	-	-	-	-	00h

Description

The command define as follows:
This command indicates the temperature value.

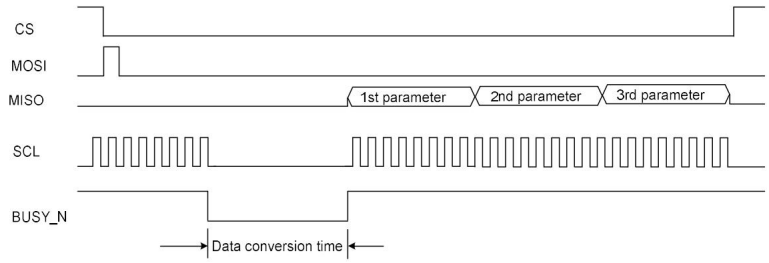
TS[7:0]: When TSE **(R41h)** is set to 0, this command reads internal temperature sensor value.

1st parameter:

TS[7:0]/D[10:3]	Temperature (°C)
1110_0111	-25
1110_1000	-24
1110_1001	-23
1110_1010	-22
1110_1011	-21
1110_1100	-20
1110_1101	-19
…	…
1111_1110	-2
1111_1111	-1

TS[7:0]/D[10:3]	Temperature (°C)
0000_0000	0
0000_0001	1
0000_0010	2
0000_0011	3
0000_0100	4
0000_0101	5
0000_0110	6
…	…
0011_1011	59
0011_1100	60

The BUSY_N behavior of other type SPI communication is the same.



This command only active when BUSY_N=1.

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TSE	W	C	0	1	0	0	0	0	0	1	41h
1st parameter	W	D	TSE	-	-	-	TO[3:0]				00h

Description

The command define as follows:
This command indicates the driver IC temperature sensor enable and calibration function.

1st parameter:

TSE	Bit[7]:TSE	Note
0	Enable internal temperature sensor	Default
1	Disable internal temperature sensor.	-

TO[3:0]: Reserve one temperature offset TO[3:0] for calibration
(Internal temperature sensor)
1. TO[3]: Mean '+' or '-', while 0 is '+'; 1 is '-'.
2. TO[2:0]: Mean temperature offset value.

Temperature offset:

TO[3:0]	Bit[3:0]:Temperature level	TO[3:0]	Bit[3:0]:Temperature level
0000	+ 0°C **(Default)**	1000	- 8°C
0001	+ 1°C	1001	- 7°C
:	:	:	:
0111	+ 7°C	1111	- 1°C

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CDI	W	C	0	1	0	1	0	0	0	0	50h
1st parameter	W	D	VBD[2:0]			DDX	CDI[3:0]				97h

Description

The command define as follows:
This command can set 2 kinds of parameters:
1. VCOM to data output interval **(CDI)** 2. Border pin output.

VBD[2:0]/DDX: Border data selection. **(From LUT)**
This register will make border pin output being mapped to a certain gray scale.

DDX	VBD[2:0]	Gray level	Note
0	000	Floating	-
	001	Gray 3	-
	010	Gray 2	-
	011	Gray 1	
	100	Gray 0	-
1	000	Gray 0	-
	001	Gray 1	-
	010	Gray 2	-
	011	Gray 3	
	100	Floating	Default

Border output voltage level: The level selection is based on mapping LUT data with VCOM shift added.
E.g.: Gray 1 waveform is mapping to 15V, VCOM value being set as -2V, the real output on border pin shall be 15V+(-2V)=13V.
Border output will follow FOPT definition being defined in R00h.

CDI[3:0] :
This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept as a default value **(Count by Hsync)**.

Bit[3]	Bit[2]	Bit[1]	Bit[0]	VCOM and data interval	Note
0	0	0	0	17Hsync	-
0	0	0	1	16Hsync	-
0	0	1	0	15Hsync	-
0	0	1	1	14Hsync	-
0	1	0	0	13Hsync	-
0	1	0	1	12Hsync	-
0	1	1	0	11Hsync	-
0	1	1	1	10Hsync	Default

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
REV	W	C	0	1	1	1	0	0	0	0	70h
1st parameter	R	D	0	0	0	0	0	1	1	0	06h
2nd parameter	R	D	REV1[7:0]								05h
3rd parameter	R	D	REV2[7:0]								01h

Description

The command define as follows:

2nd parameter:

REV1[7:0]	Bit[7:0]: E Ink internal number

3rd parameter:

REV2[7:0]	Bit[7:0]: Increased each revision:

(Default value is defined by customer.)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
AMV	W	C	1	0	0	0	0	0	0	0	80h
1st parameter	W	D	P[1:0]		AMVT[1:0]		AMVX	AMVS	AMV	AMVE	00h
2nd parameter	W	D	AMVP2								-

Description

The command define as follows:
This command indicates the IC status. Host can read this data to understand the IC status.

1st parameter:

P[1:0]	Bit[7:6]:The sensing points of sampling time	Note
00	2	Default
01	4	-
10	8	-
11	16	-

Sampling time=The last quarter of sensing time**(T)**.
VCOM=Average of N points. N=2,4,8,16.

AMVT[1:0]	Bit[5:4]:The sensing time of VCOM detection	Note
00	5s	Default
01	10s	-
10	15s	-
11	20s	-

AMVX	Bit[3]:XON setting for all Gate ON of AMV	Note
0	Gate normally scan during Auto Measure VCOM period	Default
1	All Gate ON during Auto Measure VCOM period	-

AMVS	Bit[2]:AMVS setting for Source output of AMV	Note
0	Source output 0V during auto measure VCOM period	Default
1	Source output VSPL during auto measure VCOM period	-

AMV	Bit[1]:Analogy signal	Note
0	Get VCOM value by R81H	Default
1	Gate scan only. Measure VCOM externally by probing the VCOM pad.	-

AMVE	Bit[0]:Auto measure VCOM setting	Note
0	Auto measure VCOM disable	Default
1	Auto measure VCOM enable	-

2nd parameter:

Auto Measurement VCOM would be executed only if AMVP2 =0x00.

This command only active when BUSY_N=1.

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VV	W	C	1	0	0	0	0	0	0	1	81h
1st parameter	R	D	-	VV[6:0]							00h

Description

The command define as follows:
This command gets VCOM value.

1st parameter:

VV[6:0]	Bit[6:0]:VCOM value	Note
0000000	0V	Default
0000001	-0.05V	-
0000010	-0.10V	-
:	:	-
1010000	-4.00V	-

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VDCS	W	C	1	0	0	0	0	0	1	0	82h
1st parameter	W	D	OTP_VCM	VDCS[6:0]							00h

Description

The command define as follows:
This command set the VCOMDC value. Driver will base on this value for VCOM.

1st parameter:

OTP_VCM	Bit[7]:Follow OTP VCOM value in OTP mode	Note
0	IP output value	Default
1	From the setting register	-

VDCS[6:0]	Bit[6:0]:VCOM value	Note
0000000	0V	Default
0000001	-0.05V	-
0000010	-0.10V	-
:	:	-
1010000	-4.00V	-
Others	-4.00V	-

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLW	W	C	1	0	0	0	0	0	1	1	83h
1st parameter	W	D	-	-	-	-	-	-	HRST[9:8]		00h
2nd parameter	W	D	HRST[7:2]						HRST[1:0]		00h
3rd parameter	W	D	-	-	-	-	-	-	HRED[9:8]		00h
4th parameter	W	D	HRED[7:2]						HRED[1:0]		03h
5th parameter	W	D	-	-	-	-	-	-	VRST[9:8]		00h
6th parameter	W	D	VRST[7:0]								00h
7th parameter	W	D	-	-	-	-	-	-	VRED[9:8]		00h
8th parameter	W	D	VRED[7:0]								00h
9th parameter	W	D	-	-	-	-	-	-	-	PMODE	00h

Description

The command define as follows:
The register is indicating the window before user start to transmit data.

PMODE:
0: Disable partial mode **(Default)**
1: Enable partial mode

HRST[9:0]: Horizontal start address.
HRED[9:0]: Horizontal end address.
VRST[9:0]: Vertical start address.
VRED[9:0]: Vertical end address.

No matter HRST[1:0] value being filled, it's always 00b.
No matter HRED[1:0] value being filled, it's always 11b
HRST[9]=0 and HRED[9]=0
VRST[9]=0 and VRED[9]=0

Gates scan both inside and outside of the partial window.

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PGM	W	C	1	0	0	1	0	0	0	0	90h
Description	After this command is issued, the chip would enter the program mode. After the programming procedure completed, a hardware reset is necessary for leaving program mode.										

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
APG	W	C	1	0	0	1	0	0	0	1	91h
Description	After this command is transmitted, the programming stage machine would be activated. The BUSY_N flag would fall to 0 until the programming is completed. This command only active when BUSY_N=1.										

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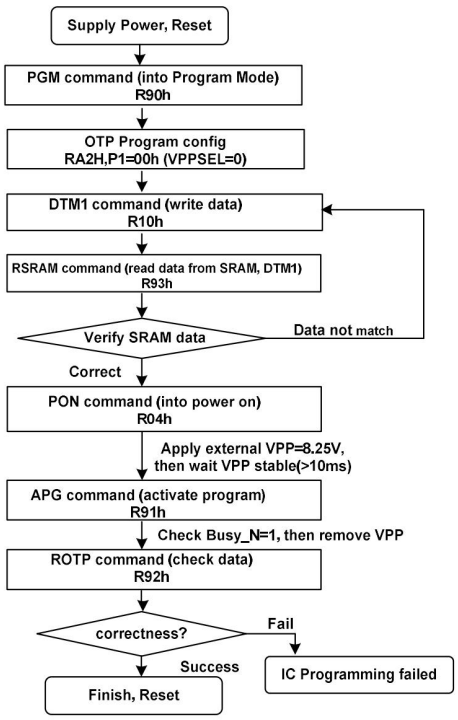
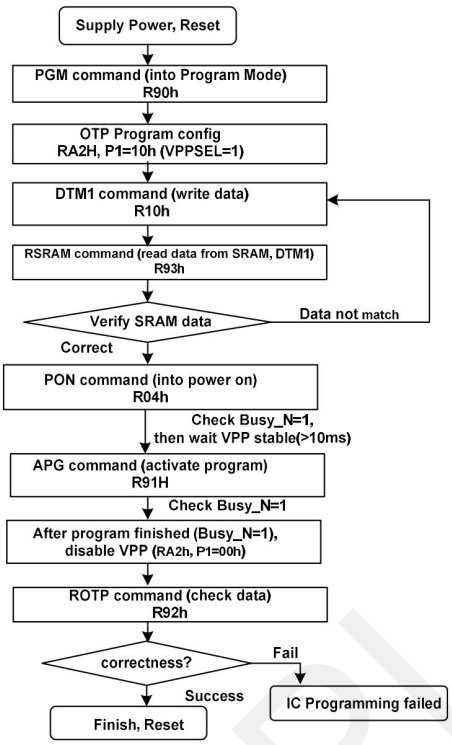
OTP programming flow (External power)



OTP programming flow (Internal power)



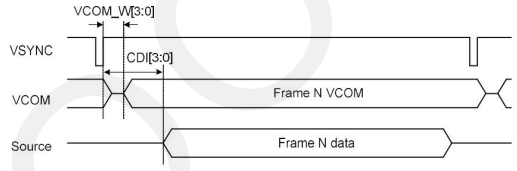
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
ROTP	W	C	1	0	0	1	0	0	1	0	92h
1st parameter	R	D	Dummy								00h
2nd parameter	R	D	The data of address 0 in the OTP								00h
3rd parameter	R	D	The data of address 1 in the OTP								00h
:	R	D	:								00h
(n+1)th parameter	R	D	The data of address (n-1) in the OTP								00h
(n+2)th parameter	R	D	The data of address (n) in the OTP								00h
Description	The command is used for reading the content of OTP for checking the data of programming.										

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWS	W	C	1	1	1	0	0	0	1	1	E3h
1st parameter	W	D	VCOM_W[3:0]				SD_W[3:0]				00h

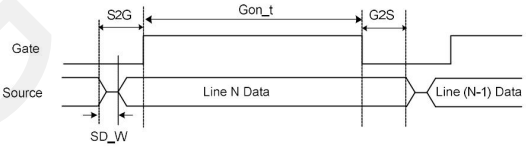
Description

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width **(Unit=Line period)**.



SD_W[3:0]: Source power saving width **(Unit=500ns), SD_W<= S2G**



Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	HEX
LVSEL	W	C	1	1	1	0	0	1	0	0	E4h
1st parameter	W	D	-	-	-	-	-	-	LVD_SEL[1:0]		03h

Description

LVD_SEL: Low power voltage selection.

LVD_SEL[1:0]	LVD value	Note
00	< 2.2V	-
01	< 2.3V	-
10	< 2.4V	-
11	< 2.5V	Default

8. Optical Specifications

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

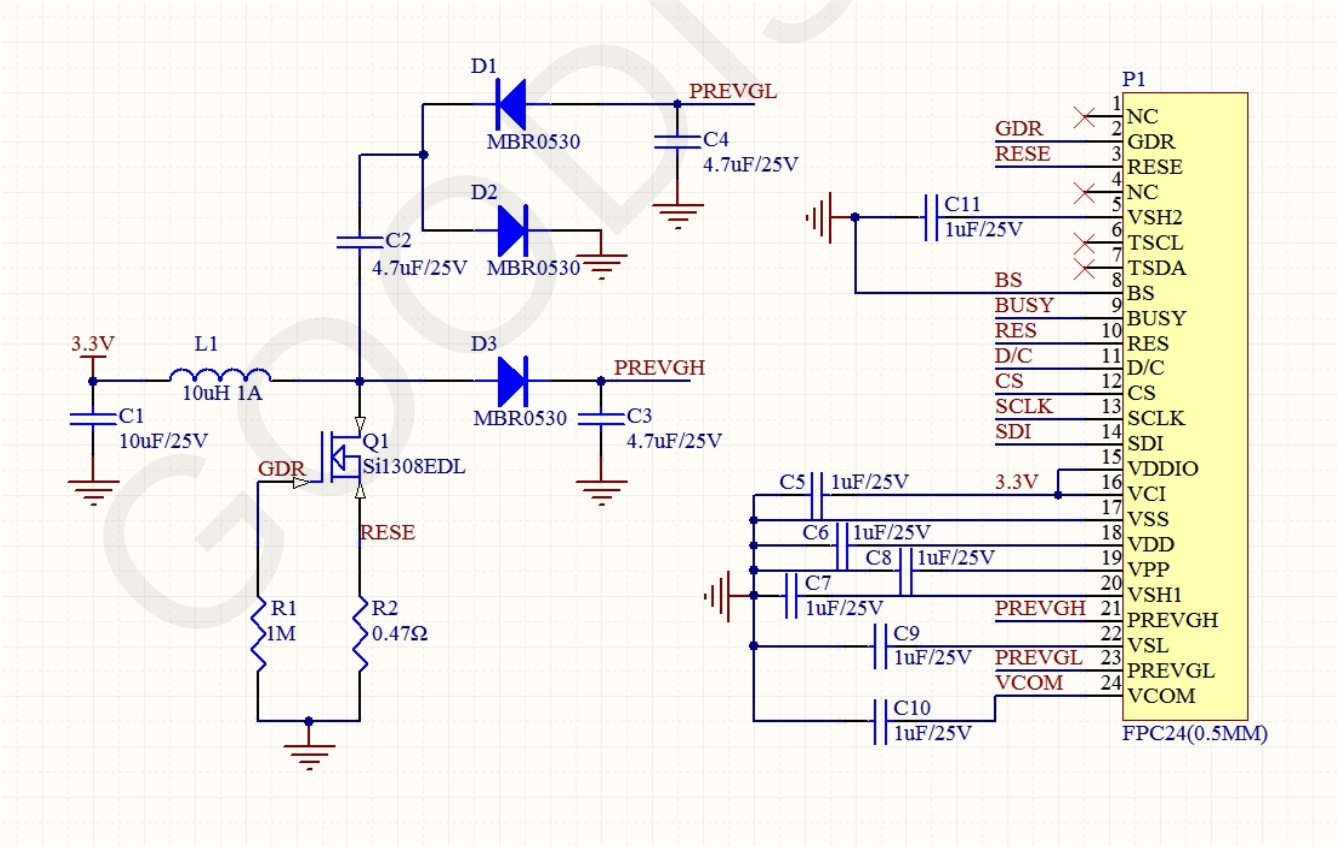
Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contrast Ratio	Indoor	8:1		-		8-2
GN	2Grey Level	-		DS+(WS-DS)*n(m-1)			8-3
T update	Image update time	at 25 °C		28	-	sec	
Life		Topr		1000000times or 5years			

Notes: 8-1. Luminance meter: Eye-One Pro Spectrophotometer.

8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

8-3. WS: White state, DS: Dark state

9. Typical Application Circuit



10. Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display, three-color (black, white and red/Yellow) E-paper Display and four-color(black, white, red and yellow) Good Display 's E-paper Display. And it is also added the functions of USB serial port, FLASH chip, font chip, current detection ect.
Development Kit consists of the development board and the pinboard.

Supported development platforms include STM32, ESP32, ESP8266, Arduino UNO, etc. More details, please click to the following links:

STM32	https://www.good-display.com/product/219.html
ESP32	https://www.good-display.com/product/338.html
ESP8266	https://www.good-display.com/product/220.html
Arduino UNO	https://www.good-display.com/product/222.html

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11. Reliability test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=60° C，RH=35%，240h Test in white pattern
3	High-Temperature Operation	T=40° C，RH=35%，240h
4	Low-Temperature Operation	T=0° C，240h
5	High-Temperature, High-Humidity Operation	T=40° C，RH=80%，240h
6	High Temperature, High Humidity Storage	T=50° C，RH=90%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25℃ 30min]→[+60℃ 30 min] : 50 cycles Test in white pattern
8	UV exposure Resistance	765W/m² for 168hrs,40 °C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell, not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display, no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display, including IC and FPC area)

Note: Put in normal temperature for 1hour after test finished, display performance is ok.

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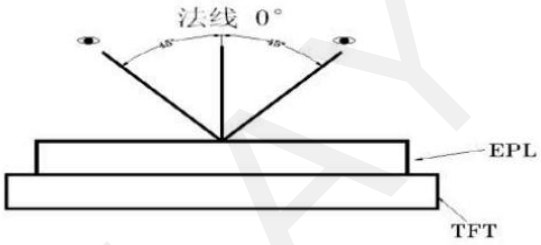
12. Inspection method and condition

12. 1 Inspection condition

Item	Condition
Illuminance	800~1500 lux
Temperature	22℃±3℃
Humidity	55±10 %RH
Distance	≥30cm
Angle	Vertical fore and aft 45
Inspection method	By eyes

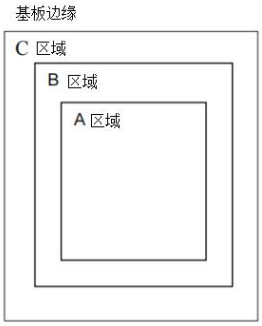


12. 2 Zone definition

A Zone： Active area

B Zone： Border zone

C Zone： From B zone edge to panel edge



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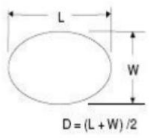
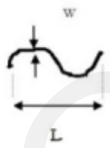
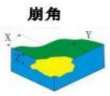
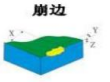
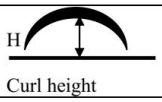
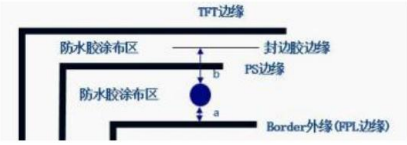
12. 3 General inspection standards for products

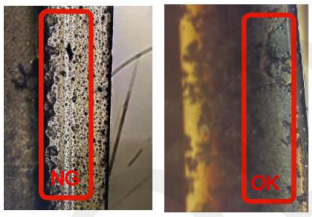
12.3.1 Appearance inspection standard

Inspection item		Figure		A zone inspection standard	B/C zone	Inspection method	MAJ/ MIN
Spot defects	Spot defects such as dot, foreign matter, air bubble, and dent etc.	Diameter D=(L+W)/2 (L-length、W-width) Measuring method shown in the figure below 	The distance between the two spots should not be less than 10mm	7.5"-13.3"Module（Not include 7.5"）： D＞1mm N=0 0.5＜D≤0.8 N≤4 D≤0.5 Ignore 0.8＜D≤1 N≤2 4.2"-7.5"Module（Not include 4.2"）： D＞0.5 N=0 0.4＜D≤0.5 N≤2 D≤0.25 Ignore 0.25＜D≤0.4 N≤4 Module below 4.2"： D＞0.5 N=0 0.4＜D≤0.5 N≤1 D≤0.25 Ignore 0.25＜D≤0.4 N≤4 0.1mm＜D≤0.25 N≤3/cm²	Foreign matter D≤1mm Pass	Check by eyes Film gauge	MIN

Inspection item		Figure		A zone inspection standard	B/C zone	Inspection method	MAJ/ MIN
Line defects	Line defects such as scratch, hair etc.	L-Length，W-Width, (W/L)＜1/4 Judged by line， (W/L)≥1/4 Judged by dot 	The distance between the two lines should not be less than 5mm	7.5"-13.3"Module（Not include 7.5"）： L＞10mm,N=0 W＞0.8mm，N=0 5mm≤L≤10mm，0.5mm≤W≤0.8mm N≤2 L≤5mm，W≤0.5mm Ignore 4.2"-7.5"Module（Not include 4.2"）： L＞8mm,N=0 W＞0.2mm，N=0 2mm≤L≤8mm，0.1mm≤W≤0.2mm N≤4 L≤2mm，W≤0.1mm Ignore Module below 4.2"： L＞5mm,N=0 W＞0.2mm，N=0 2mm≤L≤5mm，0.1mm≤W≤0.2mm N≤4 L≤2mm，W≤0.1mm Ignore	Ignore	Check by eyes Film gauge	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/ MIN
Panel chipping and crack defects	TFT panel chipping	X the length, Y the width, Z the chipping height, T the thickness of the panel  	Chipping at the edge： Module over 7.5"（Include 7.5"）： X≤ 6mm,Y≤1mm Z≤T N=3 Allowed Module below 7.5"(Not include 7.5")： X≤ 3mm,Y≤1mm Z≤T N=3 Allowed Chipping on the corner： IC sideX≤2mm Y≤2mm, Non-IC sideX≤1mm Y≤1mm . Allowed Note： Chipping should not damage the edge wiring. If it does not affect the display, allowed	Check by eyes、 Film gauge	MIN
	Crack		Crack at any zone of glass , Not allowed	Check by eyes、Film gauge	MIN
	Burr edge		No exceed the positive and negative deviation of the outline dimensions X+Y≤0.2mm Allowed	Calliper	MIN
	Curl of panel	 Curl height	Curl height H≤Total panel length 1% Allowed	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ / MIN
PS defect	Water proof film		1 .Waterproof film damage, wrinkled, open edge, not allowed 2. Exceeding the edge of module(according to the lamination drawing) Not allowed 3. Edge warped exceeds height of technical file, not allowed	Check by eyes	MIN
RTV defect	Adhesive effect		Adhesive height exceeds the display surface, not allowed	Check by eyes	MIN
			1 .Overflow, exceeds the panel side edge, affecting the size, not allowed 2 .No adhesive at panel edge≤1mm, mo exposure of wiring, allowed 3. No adhesive at edge and corner1*1mm, no exposure of wiring, allowed		
			Protection adhesive, coverage width within W≤1.5mm, no break of adhesive, allowed		
	Adhesive re-fill		Dispensing is uniform, without obvious concave and breaking, bubbling and swell, not higher than the upper surface of the PS, and the diameter of the adhesive re-filling is not more than 8mm, allowed	Check by eyes	MIN
EC defect	Adhesive bubble		1、 Effective edge sealing area of hot melt products ≥1/2 edge sealing area; 2、Bubble a+b≥1/2 effective width, N≤3, spacing≥5mm , allowed No exposure of wiring, allowed	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/ MIN
EC defect	Adhesive effect		1 .Overflow, exceeds the panel side edge, affecting the size, not allowed 2.No adhesive at panel edge≤1mm, mo exposure of wiring, allowed 3.No adhesive at edge and corner 1*1mm, no exposure of wiring, allowed 4. Adhesive height exceeds the display surface, not allowed	Visual, caliper	MIN
Silver dot adhesive defect	Silver dot adhesive		1、Single silver dot dispensing amount ≥1mm, allowed 2、One of the double silver dot dispensing amount is ≥1mm and the other has adhesive (no reference to 1mm) Allowed	Visual	MIN
			Silver dot dispensing residue on the panel ≤0.2mm, allowed	Film gauge	MIN
FPC defect	FPC wiring		FPC, TCP damage / gold finger peroxidation, adhesive residue, not allowed	Visual	MIJ
	FPC golden finger		The height of burr edge of TCP punching surface ≧ 0.4mm, not allowed	Caliper	MIN
	FPC damage/crease		Damage and breaking, not allowed Crease does not affect the electrical performance display, allowed	Check by eyes	MIN

Inspection item		Figure	Inspection standard	Inspection method	MAJ/ MIN
Protective film defect	Protective film	Scratch and crease on the surface but no affect to protection function, allowed		Check by eyes	MIN
		Adhesive at edge L≤5mm，W≤0.5mm，N=2, no entering into viewing area		Check by eyes	MIN
Stain defect	Stain	If stain can be normally wiped clean by > 99% alcohol, allowed		Visual	MIN
Pull tab defect	Pull tab	The position and direction meet the document requirements, and ensure that the protective film can be pulled off.		Check by eyes/ Manual pulling	MIN
Shading tape defect	Shading tape	Tilt≤10°, flat without warping, completely covering the IC.		Check by eyes/ Film gauge	MIN
Stiffener	Stiffener	Flat without warping, Exceeding the left and right edges of the FPC is not allowed. Left and right can be less than 0.5mm from FPC edge		Check by eyes	MIN
Label	Label/ Spraying code	The content meets the requirements of the work sheet. The attaching position meets the requirements of the technical documents.		Check by eyes	MIN

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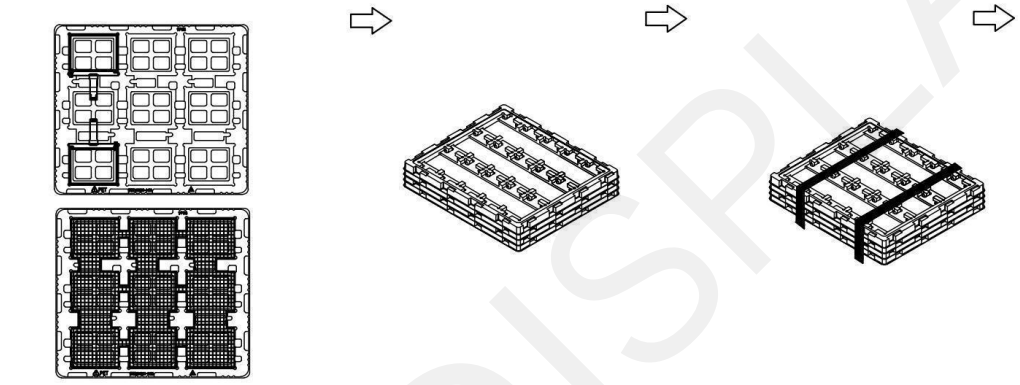
13. Packaging

PACKLING ORDER:

1) Putting 6 pcs Modules on each PET tray.And cover a dedicated EPE film.

2) Putting 9 pcs PET trays together with 1 empty tray on the top of PET tray.

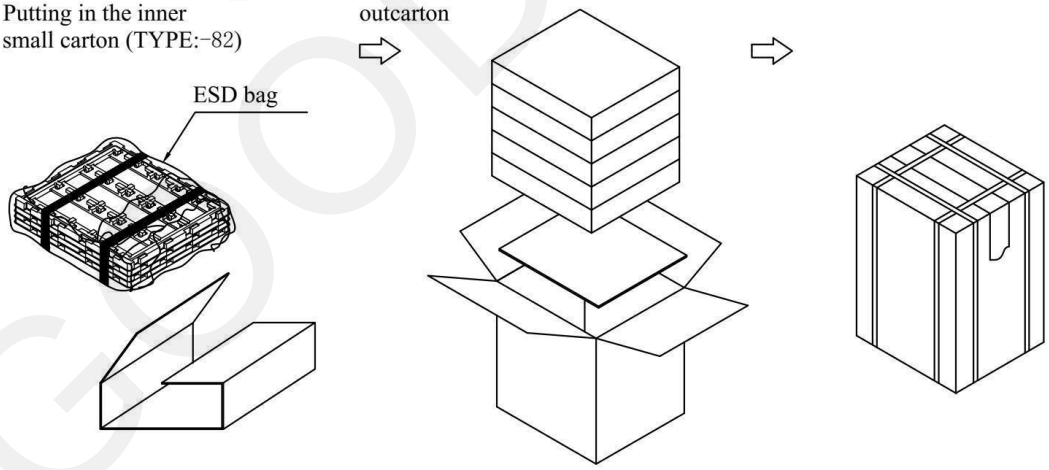
3) the tray together with rubber band



4) Insert in the ESD bag, add desiccant in the ESD bag, Putting in the inner small carton (TYPE:-82)

5) Putting 5 small cartons into one outcarton

6) Packing finished



Note:6 pcs in a tray, 9 trays in a inner carton, 5 inner cartons in a out carton, so 6x9x5=270pcs/Outcarton

Dimension (Small carton): 385*325*87mm Dimension (Out carton): 394*344*470mm

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14. Handling, Safety and Environmental Requirements

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

Product Environmental certification
RoHS

15. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.

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