



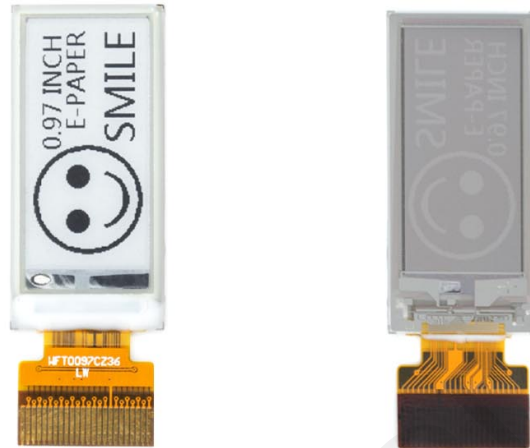
0.97 inch E-paper Display Series



GDEW0097T50

Dalian Good Display Co., Ltd.

Product Specifications



Customer	Standard
Description	0.97" E-PAPER DISPLAY
Model Name	GDEW0097T50
Date	2022/05/22
Revision	1.0

	Design Engineering		
	Approval	Check	Design
			

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1. Overview

The display is a TFT active matrix electrophoretic display, with interface and a reference system design. The 0.97" active area contains 184×88 pixels, and has 1-bit white/black full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM, and border are supplied with each panel.

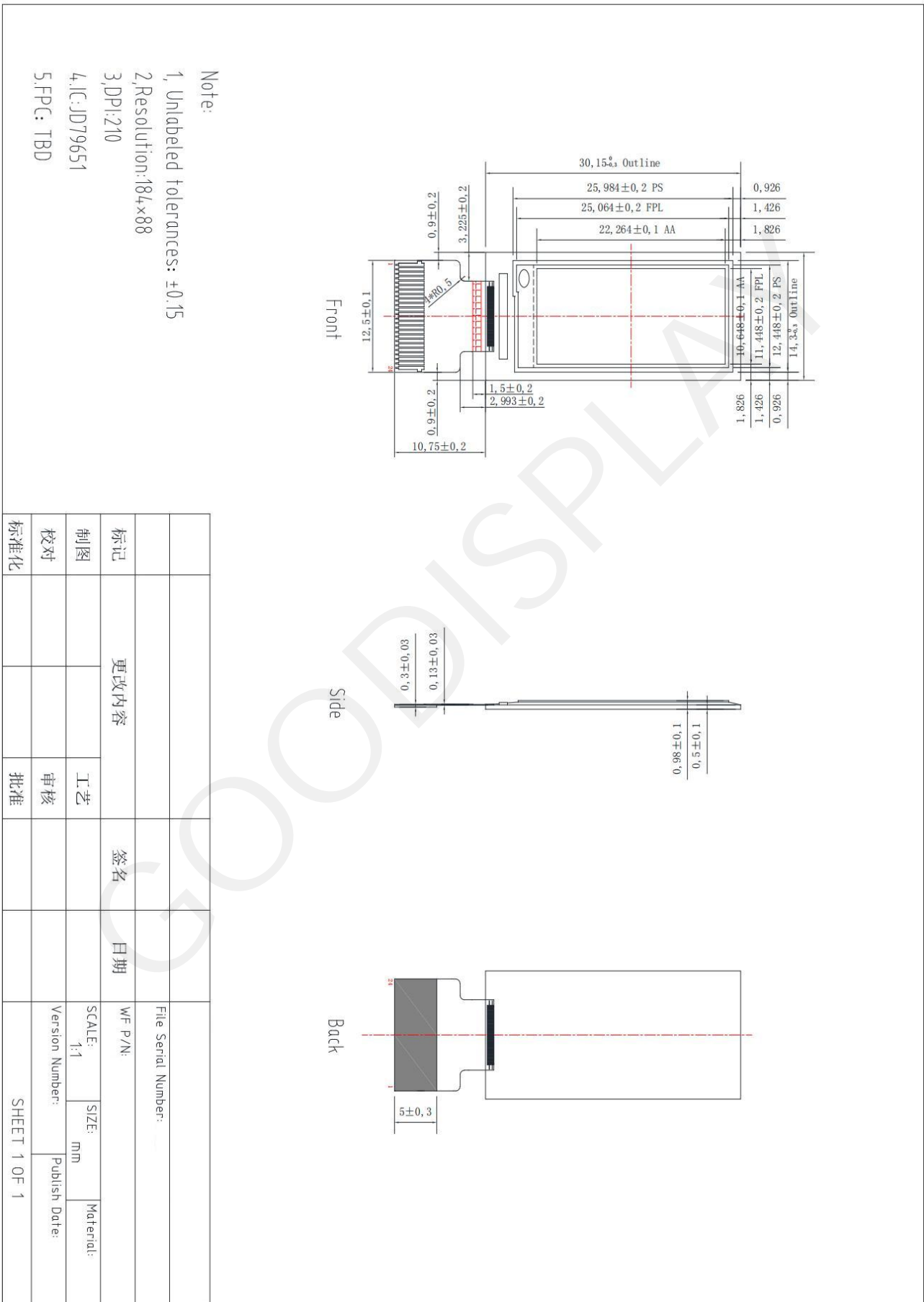
2. Features

- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On chip display RAM
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and source driving voltage
- I²C Signal Master Interface to read external temperature sensor
- Available in COG package IC thickness 180um

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	0.97	Inch	
Display Resolution	88(H)×184(V)	Pixel	Dpi: 210
Active Area	10.648(H)×22.264(V)	mm	
Pixel Pitch	0.121×0.121	mm	
Pixel Configuration	Square		
Outline Dimension	14.3(H)×30.15(V) ×0.98(D)	mm	
Weight	1±0.5	g	

4. Mechanical Drawing of EPD module



5. Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display, three-color (black, white and red/Yellow) E-paper Display and four-color (black, white, red and yellow) Good Display 's E-paper Display. And it is also added the functions of USB serial port, FLASH chip, font chip, current detection ect.

Development Kit consists of the development board and the pinboard.

Supported development platforms include STM32, ESP32, ESP8266, Arduino UNO, etc. More details, please click to the following links:

STM32 <https://www.good-display.com/product/219.html>

ESP32 <https://www.good-display.com/product/338.html>

ESP8266 <https://www.good-display.com/product/220.html>

Arduino UNO <https://www.good-display.com/product/222.html>



6. Input/Output Terminals

6.1 Pin out List

Pin #	Type	Single	Description	Remark
1		NC	No connection and do not connect with other NC pins	Keep Open
2	O	GDR	N-Channel MOSFET Gate Drive Control	
3	O	RESE	Current Sense Input for the Control Loop	
4	C	VGL	Negative Gate driving voltage	
5	C	VGH	Positive Gate driving voltage	
6	O	TSCL	I ² C Interface to digital temperature sensor Clock pin	
7	I/O	TSDA	I ² C Interface to digital temperature sensor Date pin	
8	I	BS1	Bus selection pin	Note 6-1
9	O	BUSY	Busy state output pin	Note 6-2
10	I	RES #	Reset	Note 6-3
11	I	D/C #	Data /Command control pin	Note 6-4
12	I	CS #	Chip Select input pin	Note 6-5
13	I/O	D0	serial clock pin (SPI)	
14	I/O	D1	serial data pin (SPI)	
15	I	VDDIO	Power for interface logic pins	
16	I	VCI	Power Supply pin for the chip	
17		VSS	Ground	
18	C	VDD	Core logic power pin	
19	C	VPP	Power Supply for OTP Programming	
20	C	VSH	Positive Source driving voltage	
21	C	PREVGH	Power Supply pin for VGH and VSH	
22	C	VSL	Negative Source driving voltage	
23	C	PREVGL	Power Supply pin for VCOM, VGL and VSL	
24	C	VCOM	VCOM driving voltage	

Note 6-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note 6-2: This pin (D/C#) is Data/Command control pin connecting to the MCU.

When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note 6-3: This pin (RES#) is reset signal input. The Reset is active Low.

Note 6-4: This pin (BUSY) is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin Low when the driver IC is working such as:

- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor

Note 6-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

Table: Bus interface selection

BS1	MPU Interface
L	4-lines serial peripheral interface
H	3-lines serial peripheral interface

7. Command Table

W/R: 0: Write cycle 1: Read cycle C/D: 0: Command 1: Data D7~D0: -: Don't care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default	
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00h	
		0	1	#	#	#	#	#	#	#	#	#	RES[1:0],REG,KW/R,UD,SHL,SHD_N,RST_N	8Fh
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01h	
		0	1	-	-	-	-	-	-	-	#	#	VDS_EN,VDG_EN	03h
		0	1	-	-	-	-	-	-	#	#	#	VCOM_HV,VGHL_LV[1:0]	00h
		0	1	-	-	#	#	#	#	#	#	#	VSH[5:0]	26h
		0	1	-	-	#	#	#	#	#	#	#	VSL[5:0]	26h
		0	1	-	#	#	#	#	#	#	#	#	VSHR[6:0]	06h
3	Power OFF(POF)	0	0	0	0	0	0	0	0	1	0		02h	
4	Power OFF Sequence Setting(PFS)	0	0	0	0	0	0	0	0	1	1		03h	
		0	1	-	-	#	#	-	-	-	-	-	T_VDS_OFF[1:0]	00h
5	Power ON(PON)	0	0	0	0	0	0	0	1	0	0		04h	
6	Power ON Measure(PMES)	0	0	0	0	0	0	0	1	0	1		05h	
7	Booster Soft Start(BTST)	0	0	0	0	0	0	0	1	1	0		06h	
		0	1	#	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17h
		0	1	#	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17h
		0	1	-	-	#	#	#	#	#	#	#	BT_PHC[5:0]	17h
8	Deep Sleep	0	0	0	0	0	0	0	1	1	1		07h	
		0	1	1	0	1	0	0	1	0	1	1	Check code	A5h
9	Display Start Transmission 1(DTM1, white/black Data) (x-byte command)	0	0	0	0	0	1	0	0	0	0		10h	
		0	1	#	#	#	#	#	#	#	#	#	KPXL[1:8]	00h
10	Data Stop	0	0	0	0	0	1	0	0	0	1		11h	
		1	1	#	-	-	-	-	-	-	-	-	Data_flag	00h
11	Display Refresh(DRF)	0	0	0	0	0	1	0	0	1	0		12h	
12	Display Start Transmission 2(DTM2, Red Data) (x-byte command)	0	0	0	0	0	1	0	0	1	1		13h	
		0	1	#	#	#	#	#	#	#	#	#	RPXL[1:8]	00h
13	Partial data start transmission1 (PDTM1)	0	0	0	0	0	1	0	1	0	0		14h	
		0	1	#	#	#	#	#	#	#	#	#		00h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default	
14	Partial data start transmission2 (PDTM2)	0	0	0	0	0	1	0	1	0	1		15h	
		0	1	#	#	#	#	#	#	#	#	#		00h
15	Partial Display refresh(PDRF)	0	0	0	0	0	1	0	1	1	0		16h	
		0	1	#	#	#	#	#	#	#	#	#		00h
16	OSC control(OSC)	0	0	0	0	1	1	0	0	0	0		30h	
		0	1	-	-	#	#	#	#	#	#	#	M[2:0],N[2:0],3Ah	3Ch
17	Temperature Sensor Command (TSC)	0	0	0	1	0	0	0	0	0	0		40h	
		1	1	#	#	#	#	#	#	#	#	D[10:3]/TS [7:0]	00h	
		1	1	#	#	#	-	-	-	-	-	-	D[2:0]/-	00h
18	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1		41h	
		0	1	#	-	-	-	#	#	#	#	#	TSE,TO[3:0]	00h
19	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42h	
		0	1	#	#	#	#	#	#	#	#	#	WATTR[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	#	WMSB[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	#	WLSB[7:0]	00h
20	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1		43h	
		1	1	#	#	#	#	#	#	#	#	#	RMSB[7:0]	00h
		1	1	#	#	#	#	#	#	#	#	#	RLSB[7:0]	00h
21	Vcom and data interval setting (CDI)	0	0	0	1	0	1	0	0	0	0		50h	
		0	1	#	#	#	#	#	#	#	#	#	VBD[1:0],DDX[1:0],CDI[3:0]	D7h
22	Lower Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51h	
		1	1	-	-	-	-	-	-	-	-	#	LPD	01h
23	TCON setting (TCON)	0	0	0	1	1	0	0	0	0	0		60h	
		0	1	#	#	#	#	#	#	#	#	#	S2G[3:0],G2S[3:0]	22h
24	Resolution setting (TRES)	0	0	0	1	1	0	0	0	0	1		61h	
		0	1	#	#	#	#	#	0	0	0	HRES[7:3]	00h	
		0	1	-	-	-	-	-	-	-	-	#	VRES[8:0]	00h
		0	1	#	#	#	#	#	#	#	#	#		00h
25	Source& gate Start setting	0	0	0	1	1	0	0	0	1	0		62h	
		0	1	#	#	#	#	#	-	-	-	S_start[7:3]	00h	
		0	1	-	-	-	#	-	-	-	-	#	Gscan, G_start[8]	00h
		0	1	#	#	#	#	#	#	#	#	#	G_start[7:0]	00h
26	Revision(REV)	0	0	0	1	1	1	0	0	0	0		70h	
		1	1	#	#	#	#	#	#	#	#	REV[7:0]	-	
		1	1	#	#	#	#	#	#	#	#	#	REV[15:08]	-

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
27	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71h
		1	1	-	#	#	#	#	#	#	#	PTL_FLAG,I ² C_ERR, I ² C_BUSY,DATA_FLAG,PO N,POF,BUSY	13h
28	Auto Measurement Vcom	0	0	1	0	0	0	0	0	0	0		80h
		0	1	-	-	#	#	#	#	#	#	AMVT[1:0], XON,AMVS, AMV,AMVE	10h
29	Vcom Value(VV)	0	0	1	0	0	0	0	0	0	1		81h
		1	1	-	-	#	#	#	#	#	#	VV[5:0]	00h
30	VCM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82h
		0	1	-	-	#	#	#	#	#	#	VDCS[5:0]	00h
31	Program mode(PGM)	0	0	1	0	1	0	0	0	0	0		A0h
		0	1	1	0	1	0	0	1	0	1		00h
32	Active Progmming (APG)	0	0	1	0	1	0	0	0	0	1		A1h
33	Read OTP (ROTP)	0	0	1	0	1	0	0	0	1	0		A2h

(1) Panel Setting (PSR) (Register: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting the panel	0	0	0	0	0	0	0	0	0	0
	0	1	RES1	RES0	REG	KW/R	UD	SHL	SHD_N	RST_N

RES[1:0]: Display Resolution setting (source x gate)

00b: 96x230 (Default) Active source channels: S0 ~ S95. Active gate channels: G0 ~ G229.

01b: 96x252 Active source channels: S0 ~ S95. Active gate channels: G0 ~ G251.

10b: 128x296 Active source channels: S0 ~ S127. Active gate channels: G0 ~ G295.

11b: 160x296 Active source channels: S0 ~ S159. Active gate channels: G0 ~ G295.

REG: LUT selection

0: LUT from OTP. (Default)

1: LUT from register.

KW/R: Black / White / Red

0: Pixel with Black/White/Red, KWR mode. (Default)

1: Pixel with Black/White, KW mode.

UD: Gate Scan Direction

0: Scan down. First line to last line: Gn-1 → Gn-2 → Gn-3 → ... → G0

1: Scan up. (default) First line to last line: G0 → G1 → G2 → ... → Gn-1

SHL: Source Shift direction

0: Shift left First data to last data: Sn-1 → Sn-2 → Sn-3 → ... → S0

1: Shift right. (default) First data to last data: S0 → S1 → S2 → ... → Sn-1

SHD_N: Booster Switch

0: Booster OFF

1: Booster ON (Default)

When SHD_N become LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF. And Source/Gate/Border/VCOM will be released to floating.

RST_N: Soft Reset

0: Reset. Booster OFF, Register data are set to their default values, all drivers will be reset, and all functions will be disabled. Source/Gate/Border/VCOM will be released to floating.

1: No effect (Default).

(2) Power Setting (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1
	0	1	-	-	-	-	-	-	VDS_EN	VDG_EN
	0	1	-	-	-	-	-	VCOM_HV	VGHL_LV[2:0]	
	0	1	-	-	VDH[5:0]					
	0	1	-	-	VDL[5:0]					
	0	1	-	-	VDHR[6:0]					

VDS_EN: Source power selection

0: External source power from VDH/VDL/VDHR pins.

1: Internal DC/DC function for generating VDH/VDL/VDHR.

VDG_EN: Gate power selection

0: External gate power from VGH/VGL pins

1: Internal DC/DC function for generating VGH/VGL.

VCOM_HV: VCOM Voltage Level

0: VCOMH=VDH+VCOMDC, VCOML=VHL+VCOMDC (default)

1: VCOML=VGH, VCOML=VGL

VGHL_LV[1:0]: VGH / VGL Voltage Level selection.

VGHL_LV	VGHL voltage level	VGHL_LV	VGHL voltage level
000(Default)	VGH=20V,VGL= -20V	100	VGH=16V,VGL= -16V
001	VGH=19V,VGL= -19V	101	VGH=15V,VGL= -15V
010	VGH=18V,VGL= -18V	110	VGH=14V,VGL= -14V
011	VGH=17V,VGL= -17V	111	VGH=13V,VGL= -13V

VDH[5:0]: Internal VDH power selection for B/W pixel.(Default value: 100110b)

VSH	VSH_V	VSH	VSH_V
000000	2.4V
000001	2.6V	100110	10.0V
000010	2.8V	100111	10.2V
000011	3.0V	101000	10.4V
000100	3.2V
000101	3.4V	111101	14.6V
000110	3.6V	111110	14.8V
000111	3.8V	111111	15.0V

VDL[5:0]: Internal VDL power selection for B/W pixel. (Default value: 100110b)

VDL	VDL_V	VDL	VDL_V
000000	-2.4V
000001	-2.6V	100110	-10.0V
000010	-2.8V	100111	-10.2V
000011	-3.0V	101000	-10.4V
000100	-3.2V
000101	-3.4V	111101	-14.6V
000110	-3.6V	111110	-14.8V
000111	-3.8V	111111	-15.0V

VDHR[6:0]: Internal VDHR power selection for Red pixel. (Default value: 000011b)

VSHR	VSHR_V	VSHR	VSHR_V
0000000	2.4V
0000001	2.5V	1010000	10.4V
0000010	2.6V	1010001	10.5V
0000011	2.7V	1010010	10.6V
0000100	2.8V	1010011	10.7V
0000101	2.9V	1010100	10.8V
0000110	3.0V	1010101	10.9V
0000111	3.1V	1010110	11.0V

(3) Power OFF (PWR) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	0	0	0	0	0	0	0	0	1	0

After the Power Off command, the driver will be power off. Refer to the power management section for the Sequence. This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep sleep mode. Source/Gate/Border/VCOM will be released to floating.

(4) Power off sequence setting (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1
	0	1	-	-	VSH_OFF[1:0]		VSL_OFF[1:0]		VSHR_OFF[1:0]	

Vshr_off[1:0]: 00: 5 ms (Default) 01: 10 ms 10: 20 ms 11: 40 ms

Vsl_off[1:0]: 00: 5 ms (Default) 01: 10 ms 10: 20 ms 11: 40 ms

Vsh_off[1:0]: 00: 5 ms (Default) 01: 10 ms 10: 20 ms 11: 40 ms

(5) Power ON (PON) (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the Power	0	0	0	0	0	0	0	1	0	0

After the Power ON command, the driver will be powered ON. Refer to the power management section for the sequence. This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltage are ready, the BUSY signal will return to high.

(6) Power ON Measure (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	1	0	1

If user want to read temperature sensor or detect low power in power off mode, user has to send this command. After power on measure command, driver will switch on relevant command with Low Power detection (R51H) and temperature measurement. (R40H).

(7) Booster Soft Start (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	0	0	1	1	0
	0	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0
	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0

BTPHA[7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA[5:3]: Driving strength of phase A

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4

100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHA[2:0]: Minimum OFF time setting of GDR in phase B

	000b: 0.27uS	001b: 0.34uS	010b: 0.40uS	011b: 0.54uS
	100b: 0.80uS	101b: 1.54uS	110b: 3.34uS	111b: 6.58uS
BTPHB[7:6]:	Soft start period of phase B.			
	00b: 10mS	01b: 20mS	10b: 30mS	11b: 40mS
BTPHB[5:3]:	Driving strength of phase B			
	000b: strength 1	001b: strength 2	010b: strength 3	011b: strength 4
	100b: strength 5	101b: strength 6	110b: strength 7	111b: strength 8 (strongest)
BTPHB[2:0]:	Minimum OFF time setting of GDR in phase B			
	000b: 0.27uS	001b: 0.34uS	010b: 0.40uS	011b: 0.54uS
	100b: 0.80uS	101b: 1.54uS	110b: 3.34uS	111b: 6.58uS
BTPHC[5:3]:	Driving strength of phase C			
	000b: strength 1	001b: strength 2	010b: strength 3	011b: strength 4
	100b: strength 5	101b: strength 6	110b: strength 7	111b: strength 8 (strongest)
BTPHC[2:0]:	Minimum OFF time setting of GDR in phase C			
	000b: 0.27uS	001b: 0.34uS	010b: 0.40uS	011b: 0.54uS
	100b: 0.80uS	101b: 1.54uS	110b: 3.34uS	111b: 6.58uS

(8) Deep Sleep (DSLPL) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep Sleep	0	0	0	0	0	0	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

After this command is transmitted, the chip will enter deep-sleep mode to save power. The deep sleep mode will return to standby mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

(9) Data Start Transmission 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	0	0
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

This command starts transmitting data and write them into SRAM. To complete data transmission, command DSP (Data transmission Stop) must be issued. Then the chip will start to send data/VCOM for panel.

In B/W mode, this command writes “OLD” data to SRAM.

In B/W/Red mode, this command writes “B/W” data to SRAM.

In Program mode, this command writes “OTP” data to SRAM for programming.

(10) Data Stop (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Stopping data transmission	0	0	0	0	0	1	0	0	0	1
	1	1	Data_flag	-	-	-	-	-	-	-

Check the completeness of data. If data is complete, start to refresh display.

Data_flag: Data flag of receiving user data.

0: Driver didn't receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After "Data Start" (R10h) or "Data Stop" (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY signal will become "0" and the refreshing of panel starts.

(11) Display Refresh (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Refreshing the display	0	0	0	0	0	1	0	0	1	0

After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT. After Display Refresh command, BUSY_N signal will become "0".

This command only active when BUSY_N = "1".

(12) Display Refresh (DRF) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	1	1
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

This command starts transmitting data and write them into SRAM. To complete data transmission, command DSP (Data transmission Stop) must be issued. Then the chip will start to send data/VCOM for panel.

In B/W mode, this command writes "NEW" data to SRAM.

In B/W/Red mode, this command writes "RED" data to SRAM.

(13) Partial Data Start transmission 1 Register (PDTM1) R14H

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	1	0	0
	0	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0
	0	1								Y[8]
	0	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]
	0	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0
	0	1								L[8]
	0	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]
	0	1	Kpixel1	Kpixel2	Kpixel3	Kpixel4	Kpixel5	Kpixel6	Kpixel7	Kpixel8
	0	1								
	0	1	Kpixel(n-7)	Kpixel(n-6)	Kpixel(n-5)	Kpixel(n-4)	Kpixel(n-3)	Kpixel(n-2)	Kpixel(n-1)	Kpixeln

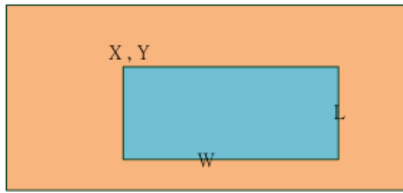
The command define as follows:

The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel.

In B/W mode, this command writes "OLD" data to SRAM.

In B/W/Red mode, this command writes "B/W" data to SRAM.

Partial update location and area



Note: X and W should be the multiple of 8.

(14) Partial Data Start transmission 2 register (R15h)

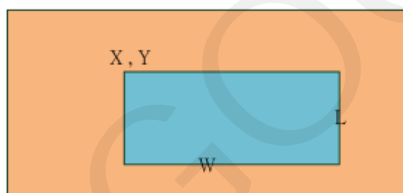
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial Data Start transmission 2	0	0	0	0	0	1	0	1	0	1
	0	1	-	-	-	-	-	-	-	X[8]
	0	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0
			-	-	-	-	-	-	-	Y[8]
	0	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]
	0	1	-	-	-	-	-	-	-	W[8]
	0	1	W[7]	W[6]	W[5]	W[4]	W[3]	0	0	0
			-	-	-	-	-	-	-	L[8]
	0	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]
	0	1	Kpixel1	Kpixel2	Kpixel3	Kpixel4	Kpixel5	Kpixel6	Kpixel7	Kpixel8
	0	1
	0	1	Kpixel(n-7)	Kpixel(n-6)	Kpixel(n-5)	Kpixel(n-4)	Kpixel(n-3)	Kpixel(n-2)	Kpixel(n-1)	Kpixel(n)

The command define as follows: The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 11H. Then chip will start to send data/VCOM for panel.

In B/W mode, this command writes “NEW” data to SRAM.

In B/W/Red mode, this command writes “RED” data to SRAM.

Partial update location and area



Note: X and W should be the multiple of 8.

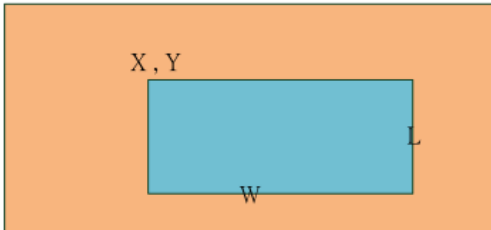
(1) Partial Display Refresh Command (R16h)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial Display Refresh	0	0	0	0	0	1	0	1	1	0
	0	1	DFV_EN							X[8]
	0	1	X[7]	X[6]	X[5]	X[4]	X[3]	0	0	0
										Y[8]
	0	1	Y[7]	Y[6]	Y[5]	Y[4]	Y[3]	Y[2]	Y[1]	Y[0]

	0	1								W[8]
	0	1	W[7]	W[6]	W[5]	W[4]	W[3]	W[2]	W[1]	W[0]
										L[8]
	0	1	L[7]	L[6]	L[5]	L[4]	L[3]	L[2]	L[1]	L[0]

While user sent this command, driver will refresh display (data/VCOM) base on SRAM data and LUT.

Only the area (X,Y, W, L) would update, the others pixel output would follow VCOM LUT After display refresh command, BUSY_N signal will become “0”.



Note: X and W should be the multiple of 8.

DFV_EN: data follow VCOM function on display area.

DFV_EN=1: Only effective in B/W mode, if pixel from “New data” SRAM equal to “Old data” SRAM on display area, this pixel output would follow VCOM LUT.

DFV_EN=0: Data doesn't follow VCOM LUT.

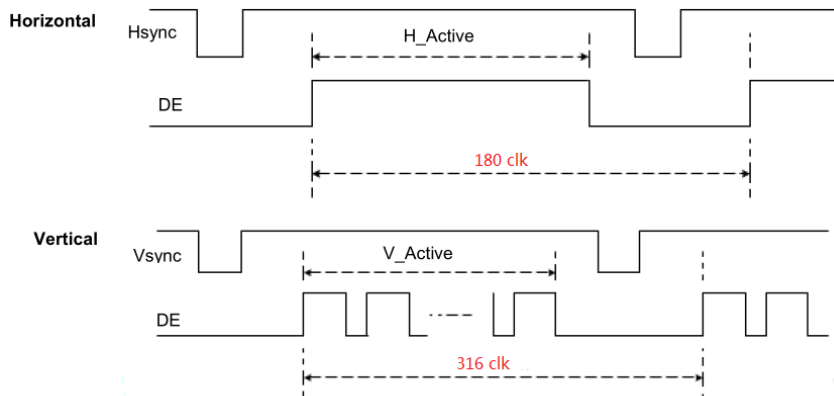
This command only active when BUSY_N = “1”.

(15) OSC Control (PLL) (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Controlling PLL	0	0	0	0	1	1	0	0	0	0
	0	1	-	-	M[2:0]			N[2:0]		

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

M	N	Frame Rate	M	N	Frame Rate	M	N	Frame Rate	M	N	Frame Rate
1	1	29 Hz	3	1	86 Hz	5	1	150 Hz	7	1	200 Hz
	2	14 Hz		2	43 Hz		2	72 Hz		2	100 Hz
	3	10 Hz		3	29 Hz		3	48 Hz		3	67 Hz
	4	7 Hz		4	21 Hz		4	36 Hz		4	50 Hz (Default)
	5	6 Hz		5	17 Hz		5	29 Hz		5	40 Hz
	6	5 Hz		6	14 Hz		6	24 Hz		6	33Hz
	7	4 Hz		7	12Hz		7	20 Hz		7	29 Hz
2	1	57 Hz	4	1	114 Hz	6	1	171 Hz			
	2	29 Hz		2	57 Hz		2	86 Hz			
	3	19 Hz		3	38 Hz		3	57 Hz			
	4	14 Hz		4	29Hz		4	43 Hz			
	5	11 Hz		5	23 Hz		5	34 Hz			
	6	10 Hz		6	19 Hz		6	29 Hz			
	7	8 Hz		7	16 Hz		7	24 Hz			



(16) Temperature Sensor Calibration (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	0	0	0	0	0	0
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6/TS3	D5/TS2	D4/TS1	D3/TS0
	1	1	D2	D1	D0	-	-	-	-	-

This command reads the temperature sensed by the temperature sensor.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temperature (°C)	TS[7:0]/D[10:3]	Temperature (°C)	TS[7:0]/D[10:3]	Temperature (°C)
1110_0111	-25	0000_0000	0	0001_1001	25
1110_1000	-24	0000_0001	1	0001_1010	26
1110_1001	-23	0000_0010	2	0001_1011	27
1110_1010	-22	0000_0011	3	0001_1100	28
1110_1011	-21	0000_0100	4	0001_1101	29
1110_1100	-20	0000_0101	5	0001_1110	30
1110_1101	-19	0000_0110	6	0001_1111	31
1110_1110	-18	0000_0111	7	0010_0000	32
1110_1111	-17	0000_1000	8	0010_0001	33
1111_0000	-16	0000_1001	9	0010_0010	34
1111_0001	-15	0000_1010	10	0010_0011	35
1111_0010	-14	0000_1011	11	0010_0100	36
1111_0011	-13	0000_1100	12	0010_0101	37
1111_0100	-12	0000_1101	13	0010_0110	38
1111_0101	-11	0000_1110	14	0010_0111	39
1111_0110	-10	0000_1111	15	0010_1000	40
1111_0111	-9	0001_0000	16	0010_1001	41
1111_1000	-8	0001_0001	17	0010_1010	42
1111_1001	-7	0001_0010	18	0010_1011	43
1111_1010	-6	0001_0011	19	0010_1100	44

1111_1011	-5	0001_0100	20	0010_1101	45
1111_1100	-4	0001_0101	21	0010_1110	46
1111_1101	-3	0001_0110	22	0010_1111	47
1111_1110	-2	0001_0111	23	0011_0000	48
1111_1111	-1	0001_1000	24	0011_0001	49

TS[1:0]	T (°C)
00	+0
01	+0.25
10	+0.5
11	+0.75

(17) Temperature Sensor Enable (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enable Temperature Sensor/Offset	0	0	0	1	0	0	0	0	0	1
	0	1	TSE	-	-	-	TO[3:0]			

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (Default)

1: Disable; using external sensor.

TO[3:0]: Temperature offset.

TO[3]: sign bit 0b: + 1b: -

TO[2:0]	Calculation	TO[2:0]	Calculation
0000 b	0
0001	1	0110	6
0010	2	0111	7

(18) Temperature Sensor Write (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Write External Temperature Sensor	0	0	0	1	0	0	0	0	1	0
	0	1	WATTR[7:0]							
	0	1	WMSB[7:0]							
	0	0	WLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.

WATTR: D[7:6]: I²C Write Byte Number

00b : 1 byte (head byte only)

01b : 2 bytes (head byte + pointer)

10b : 3 bytes (head byte + pointer + 1st parameter)

11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

D[5:3]: User-defined address bits (A2, A1, A0)

D[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor.

WLSB[7:0]: LSByte of write-data to external temperature sensor.

(19) Temperature Sensor Read (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read External Temperature Sensor	0	0	0	1	0	0	0	0	1	1
	1	1	RMSB[7:0]							
	1	1	RLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor

RLSB[7:0]: LSByte read data from external temperature sensor

(20) VCOM And Data Interval Setting (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval Between Vcom and Data	0	0	0	1	0	1	0	0	0	0
	0	1	VBD[1:0]		DDX[1:0]		CDI[3:0]			

This command indicates the interval of Vcom and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

VBD[1:0]: Border data selection

B/W/Red mode (BWR=0)

DDX[0]	VBD[1:0]	LUT	DDX[0]	VBD[1:0]	LUT
0	00	Floating	1(Default)	00	LUTB
	01	LUTR		01	LUTW
	10	LUTW		10	LUTR
	11	LUTB		11	Floating

B/W mode (BWR=1)

DDX[0]	VBD[1:0]	LUT	DDX[0]	VBD[1:0]	LUT
0	00	Floating	1(Default)	00	Floating
	01	LUTBW (1→0)		01	LUTWB (1→0)
	10	LUTWB (0→1)		10	LUTBW (0→1)
	11	Floating		11	Floating

DDX[1:0]: Data polarity.

DDX[1] for RED data, DDX[0] for BW data in the B/W/Red mode.

DDX[0] for B/W mode.

B/W/Red mode (BWR=0)

DDX[1:0]	Data{Red, B/W}	LUT	DDX[1:0]	Data{Red, B/W}	LUT
00	00	LUTW	10	00	LUTR
	01	LUTB		01	LUTR
	10	LUTR		10	LUTW
	11	LUTR		11	LUTB

01(Default)	00	LUTB	11	00	LUTR
	01	LUTW		01	LUTR
	10	LUTR		10	LUTB
	11	LUTR		11	LUTW

B/W mode (BWR=1)

DDX[0]	Data{New, Old}	LUT	DDX[0]	Data{New, Old}	LUT
0	00	LUTWW (0→0)	1(Default)	00	LUTBB (0→0)
	01	LUTBW (1→0)		01	LUTWB (0→1)
	10	LUTWB (0→1)		10	LUTBW (1→0)
	11	LUTBB (1→1)		11	LUTWW (1→1)

CDI[3:0]: Vcom and data interval

CDI[3:0]	Vcom and Data Interval	CDI[3:0]	Vcom and Data Interval
0000 b	17 hsync	0110	11
0001	16	0111	10 (Default)
0010	15
0011	14	1101	4
0100	13	1110	3
0101	12	1111	2

(21) Low Power Detection (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Detect Low Power	0	0	0	1	0	1	0	0	0	1
	1	1	-	-	-	-	-	-	-	LPD

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Interval Low Power Detection Flag

0: Low power input (VDD < 2.5V) 1: Normal status (default)

(22) TCON Setting (TCON) (R60H)

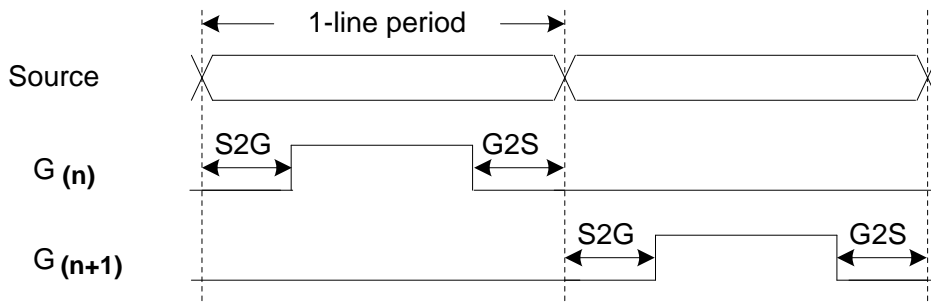
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Gate/Source Non-overlap Period	0	0	0	1	1	0	0	0	0	0
	0	1	S2G[3:0]				G2S[3:0]			

This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period	S2G[3:0] or G2S[3:0]	Period
0000b	4
0001	8	1011	48
0010	12(Default)	1100	52
0011	16	1101	56
0100	20	1110	60
0101	24	1111	64

Period = 660 nS.



(23) Resolution Setting (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	0	1	1	0	0	0	0	1	
	0	1	HRES[7:3]					0	0	0	
	0	1	-	-	-	-	-	-	-	VRES[8]	
	0	0	VRES[7:0]								

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[7:3]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Active channel calculation:

- GD : First active gate = G0 (Fixed); LAST active gate = VRES[8:0] - 1
- SD : First active source = S0 (Fixed); LAST active source = HRES[7:3]*8 - 1

(24) Source & gate start setting(R62H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Source & gate start setting	0	0	0	1	1	0	0	0	0	1
	0	1	S_start[7]	S_start[6]	S_start[5]	S_start[4]	S_start[3]	-	-	-
	0	1	-	-	-	gscan	-	-	-	G_start[8]
	0	1	G_start[7]	G_start[6]	G_start[5]	G_start[4]	G_start[3]	G_start[2]	G_start[1]	G_start[0]

1. S_Start [8:0]: which source output line is the first date line
2. G_Start[8:0]: which gate line is the first scan line
3. gscan: Gate scan select
- 0: Normal scan
- 1: Cascade type 2 scan

(25) REVISION register(REV) R70H

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
REVISION register	0	0	0	1	1	1	0	0	0	0
	0	1	REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]
	0	1	REV[15]	REV[14]	REV[13]	REV[12]	REV[11]	REV[10]	REV[9]	REV[8]

The command defines as: The LUT_REV is read from OTP address = 0x001.& 0x002

(26) Status register (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read Flags	0	0	0	1	1	1	0	0	0	1
	1	1	-	-	I ² C_ERR	I ² C_BUSY	data_flag	PON	POF	BUSY

This command reads the IC status.

I²C_ERR: I²C master error status.

I²C_BUSY_N: I²C master BUSY_N status (low active)

Data_flag: Driver has already received all the one frame data.

PON: 0: Not in PON mode. 1: In PON mode.

POF: 0: Not in POF mode. 1: In POF mode.

BUSY_N: Driver BUSY_N status (low active)

(27) Auto Measure Vcom (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	0
	0	1	-	-	AMVT[1:0]	XON	AMVS	AMV	AMVE	

This command reads the IC status.

AMVT[1:0]: Auto Measure Vcom Time

00b: 3s

01b: 5s (Default)

10b: 8s

11b: 10s

XON: All Gate ON of AMV

0: Gate normally scan during Auto Measure VCOM period. (default)

1: All Gate ON during Auto Measure VCOM period.

AMVS: Source output of AMV

0: Source output 0V during Auto Measure VCOM period. (default)

1: Source output VDHR during Auto Measure VCOM period.

AMV: Analog signal

0: Get Vcom value with the VV command (R81h) (default)

1: Get Vcom value in analog signal. (External analog to digital converter)

AMVE: Auto Measure Vcom Enable (Disable)

0: Auto measure VCOM disable (default)

1: Auto measure VCOM enable

(28) Vcom Value (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	1
	1	1	-	-	VV[5:0]					

This command gets the Vcom value.

VV[5:0]: Vcom Value Output

VV[5:0]	Vcom value
00 0000b	-0.10 V
00 0001b	-0.15 V

00 0010b	-0.20 V
:	:
11 1010b	-3.00 V

(29) VCM_DC Setting (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set VCM_DC	0	0	1	0	0	0	0	0	1	0
	0	1	-	-	VDCS[5:0]					

This command sets VCOM_DC value

VDCS[5:0]: VCOM_DC Setting

VDCS[5:0]	Vcom value
00 0000b	-0.10 V (default)
00 0001b	-0.15 V
00 0010b	-0.20 V
:	:
11 1010b	-3.00 V

(30) Program Mode (PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enter Program Mode	0	0	1	0	1	0	0	0	0	0
	0	1	1	0	1	0	0	1	0	1

After this command is issued, the chip would enter the program mode.

The mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be executed if check code = 0xA5.

(31) Active Program (APG) (RA1H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Active Program OTP	0	0	1	0	1	0	0	0	0	1

After this command is transmitted, the programming state machine would be activated.

(32) Read OTP Data (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read OTP data for check	0	0	1	0	1	0	0	0	1	0
	1	1	Dummy							
	1	1	The data of address 0x000 in the OTP							
	1	1	The data of address 0x001 in the OTP							
	1	1	..							
	1	1	The data of address (n-1) in the OTP							
	1	1	The data of address (n) in the OTP							

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0xFFF.

8. Electrical Characteristics

8.1 Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V _{CI}	-0.3 to +6.0	V
Logic Input Voltage	V _{IN}	-0.3 to V _{CI} +2.4	V
Operating Temp. range	T _{OPR}	0 to +50	°C
Storage Temp. range	T _{STG}	-25 to +70	°C

8.2 Panel DC Characteristics

The following specifications apply for: V_{SS} = 0V, V_{CI} = 3.3V, T_A = 25

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Single ground	V _{SS}	-	-	0	-	V
Logic Supply Voltage	V _{CI}	-	2.3	3.3	3.6	V
High level input voltage	V _{IH}	Digital input pins	0.7V _{CI}	-	V _{CI}	V
Low level input voltage	V _{IL}	Digital input pins	0	-	0.3V _{CI}	V
High level output voltage	V _{OH}	Digital input pins , I _{OH} = 400uA	V _{CI} -0.4	-	-	V
Low level output voltage	V _{OL}	Digital input pins , I _{OL} = -400uA	0	-	0.4	V
Image update current	I _{UPDATE}	-	-	8	10	mA
Standby panel current	I _{standby}	-	-	-	5	uA
Power panel (update)	P _{UPDATE}	-	-	120	250	mW
Standby power panel	P _{STBY}	-	-	-	0.0165	mW
Operating temperature	-	-	0	-	50	°C
Storage temperature	-	-	-25	-	70	°C
Full update Time	-	-	-	4	5	Sec
Partial update Time	-	-	-	0.3	-	Sec
Deep sleep mode current	I _{VCI}	DC/DC off No clock No input load Ram data not retain	-	2	5	uA
Sleep mode current	I _{VCI}	DC/DC off No clock No input load Ram data retain	-	35	50	uA

- The Typical power consumption is measured with following pattern transition : from horizontal 2 gray scale pattern to vertical 2 gray scale pattern.(Note 8-1)
- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display -V_{com} is recommended to be set in the range of assigned value ±0.1V.

Note 8-1

The Typical power consumption



8.3 Panel AC Characteristics

8.3.1 Oscillator frequency

The following specifications apply for : VSS = 0V, VCI = 3.3V, TA= 25

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal Oscillator frequency	Fosc	VCI=2.3 to 3.6V	-	1.625	-	MHz

8.3.2 MCU Interface

8.3.2.1 MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS1 pins. When it is " Low" , 4-wire SPI is selected. When it is " High" , 3-wire SPI (9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
	D1	D0	CS#	D/C#	RES#
Bus interface	SDIN	SCLK	CS#	D/C#	RES#
SPI4	SDIN	SCLK	CS#	D/C#	RES#
SPI3	SDIN	SCLK	CS#	L	RES#

Table 8.1:MCU interface assignment under different bus interface mode

Note 8.2: L is connected to VSS

Note 8.3: H is connected to VCI

8.3.2.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN.

Function	CS#	D/C#	SCLK
Write Command	L	L	↑
Write data	L	H	↑

Table 8.2: Control pins of 4-wire Serial Peripheral interface

Note 8.4: ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the GraphicDisplay Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

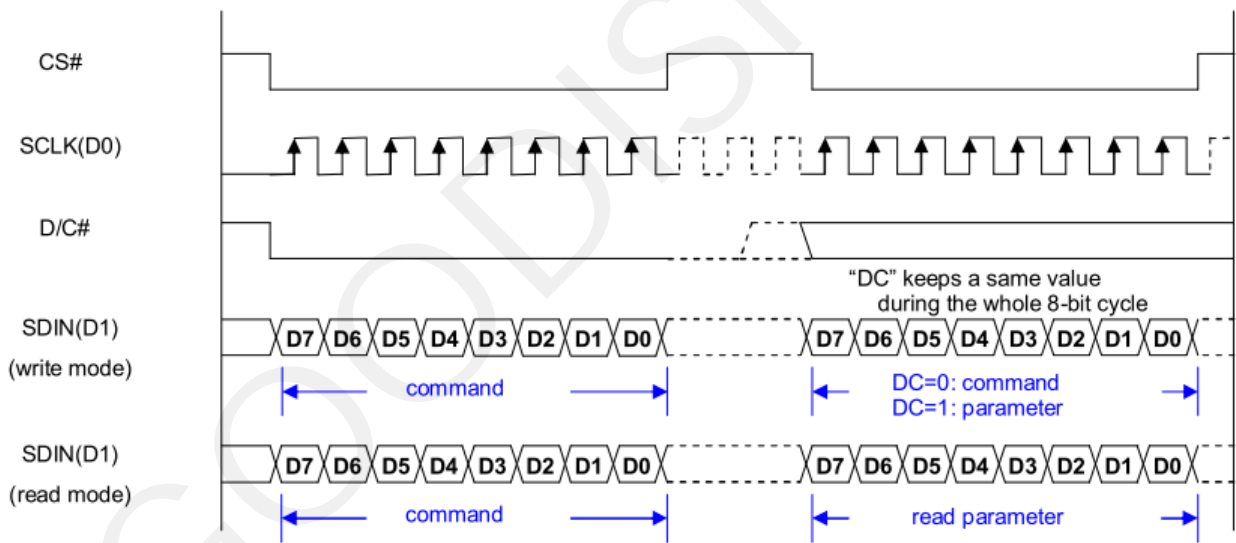


Figure 8.1: Write procedure in 4-wire Serial PeripheralInterface mode

8.3.2.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data ADIN and CS#. In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN, The pin D/C# can be connected to an external ground. The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write Command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

Table 8.3: Control pins of 3-wire Serial Peripheral Interface

Note 8.5: stands for rising edge of signal

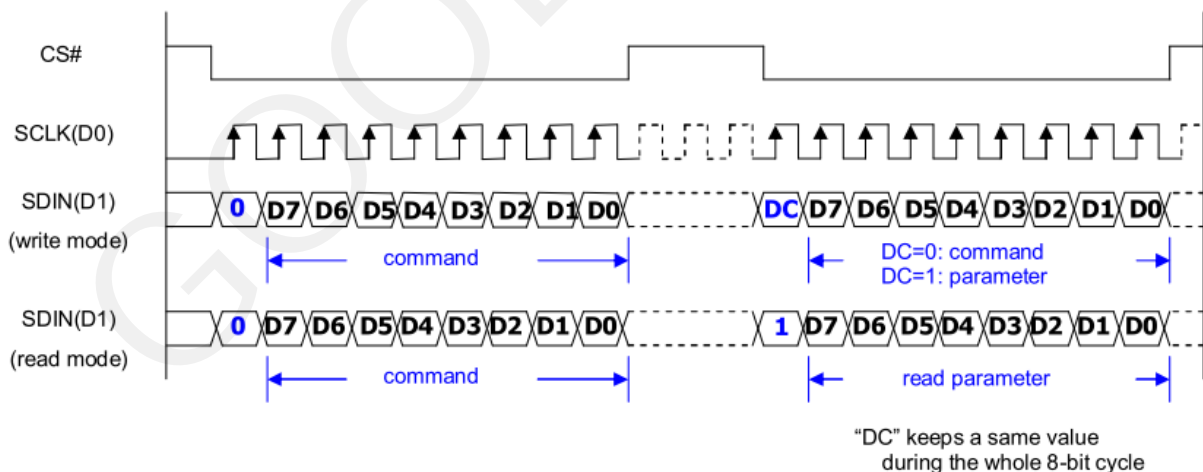
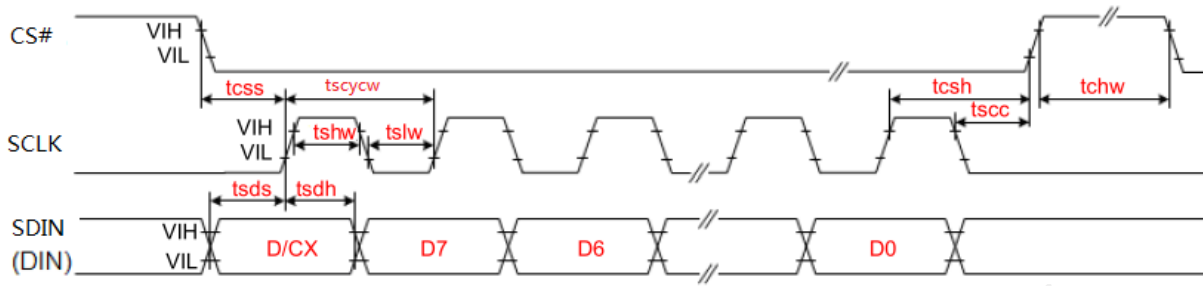
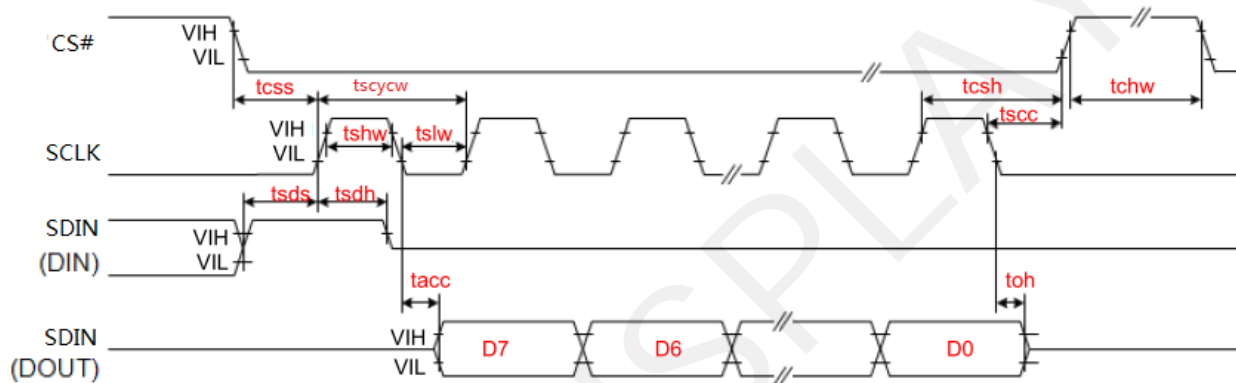


Figure 8.2: Write procedure in 3-wire Serial Peripheral Interface mode

8.3.3 Timing Characteristics of Series Interface



3-wire Serial Interface – Write



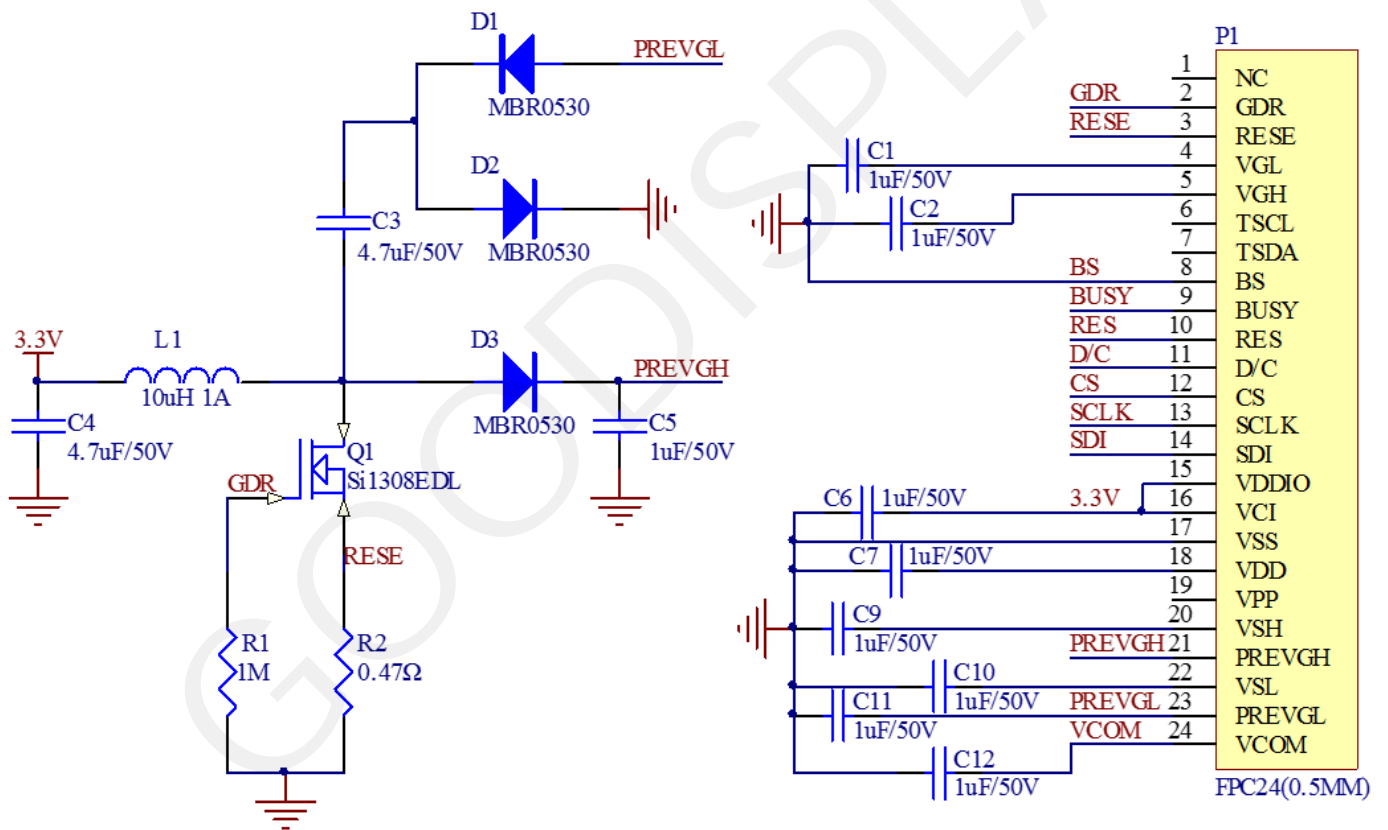
3-wire Serial Interface – Read

Symbol	Signal	Parameter	Min	Typ	Max	Unit
tcss	CS#	Chip Select Setup Time	60	-	-	ns
tsh		Chip Select Hold Time	65	-	-	ns
tsc		Chip Select Setup Time	20	-	-	ns
tchw		Chip Select Setup Time	40	-	-	ns
tscycw		Serial clock cycle (write)	100	-	-	ns
tshw	SCLK	SCL "H" pulse width (write)	35	-	-	ns
tslw		SCL "L" pulse width (write)	35	-	-	ns
tscycr		Serial clock cycle (Read)	150	-	-	ns
tshr		SCL "H" pulse width (Read)	60	-	-	ns
tslr		SCL "L" pulse width (Read)	60	-	-	ns
tsds	SDIN (DIN)	Data setup time	30	-	-	ns
tsdh		Data hold time	30	-	-	ns
tacc	SDIN (DOUT)	Access time	-	-	10	ns
toh		Output disable time	15	-	-	ns

8.4 Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25°C	26.4	40	mW	-
Power consumption in standby mode	-	25°C	-	0.0165	mW	-

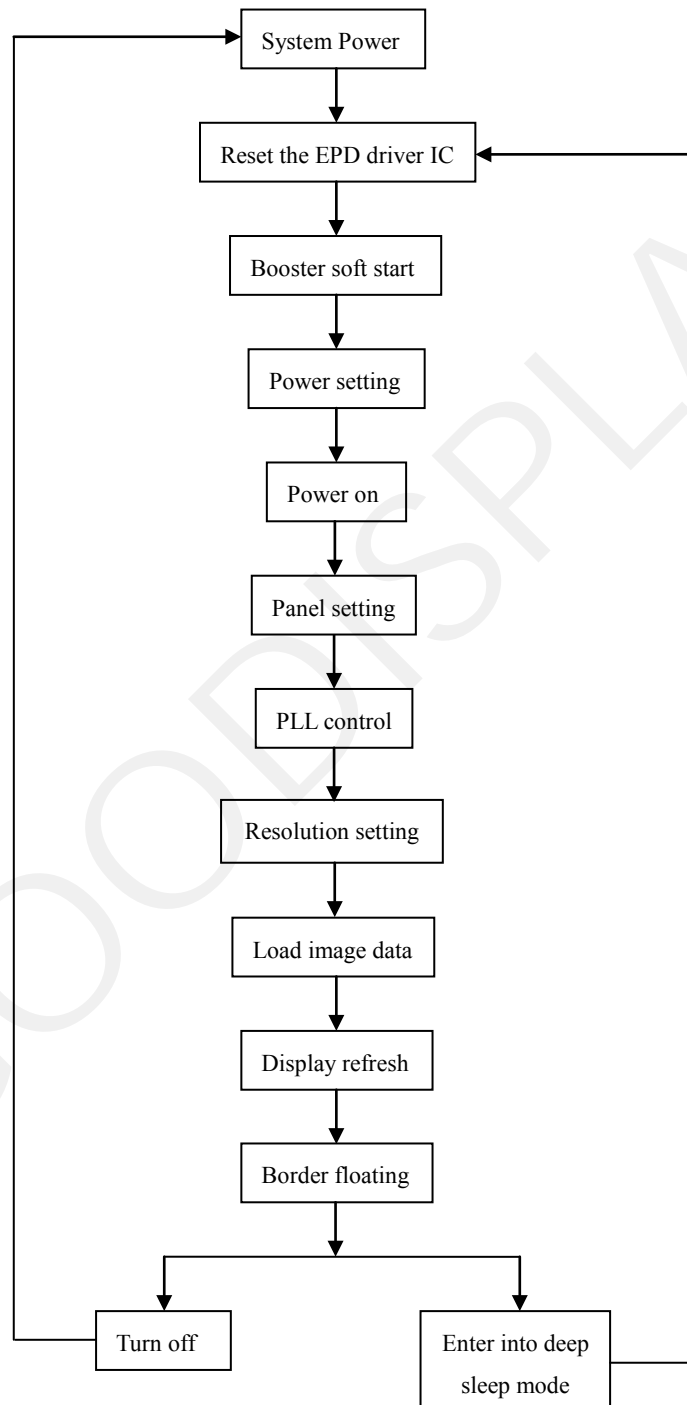
8.5 Reference Circuit



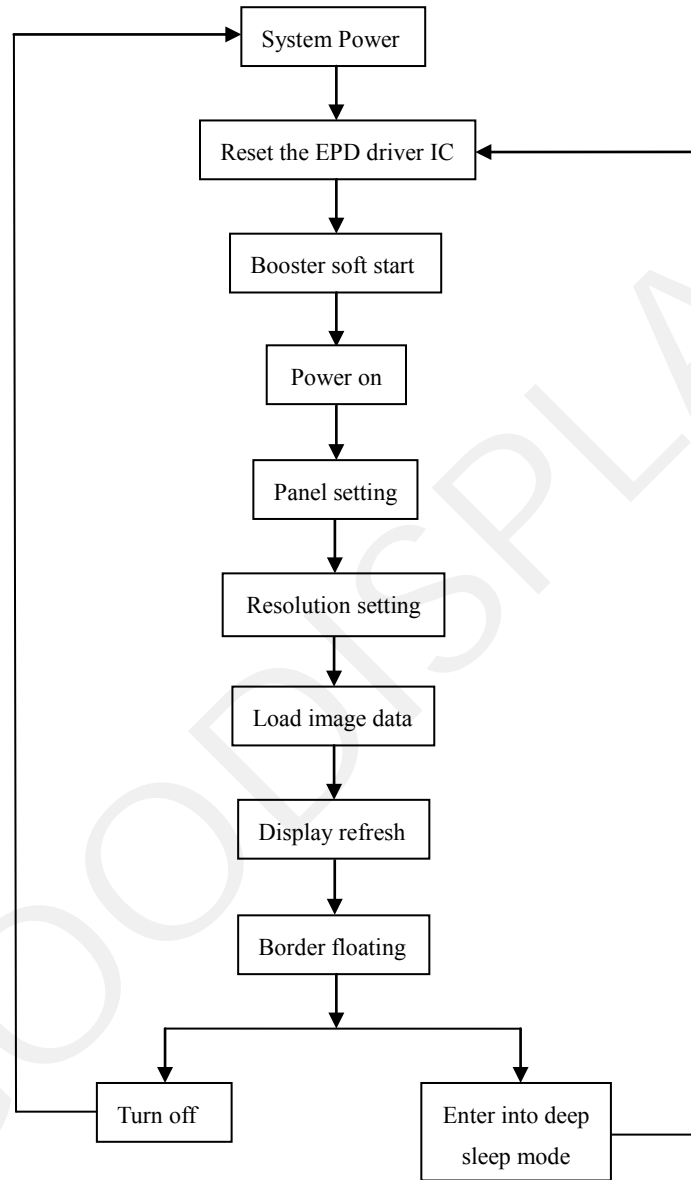
9. Typical Operating Sequence

9.1 Normal Operation Flow

1. BW mode & LUT form Register

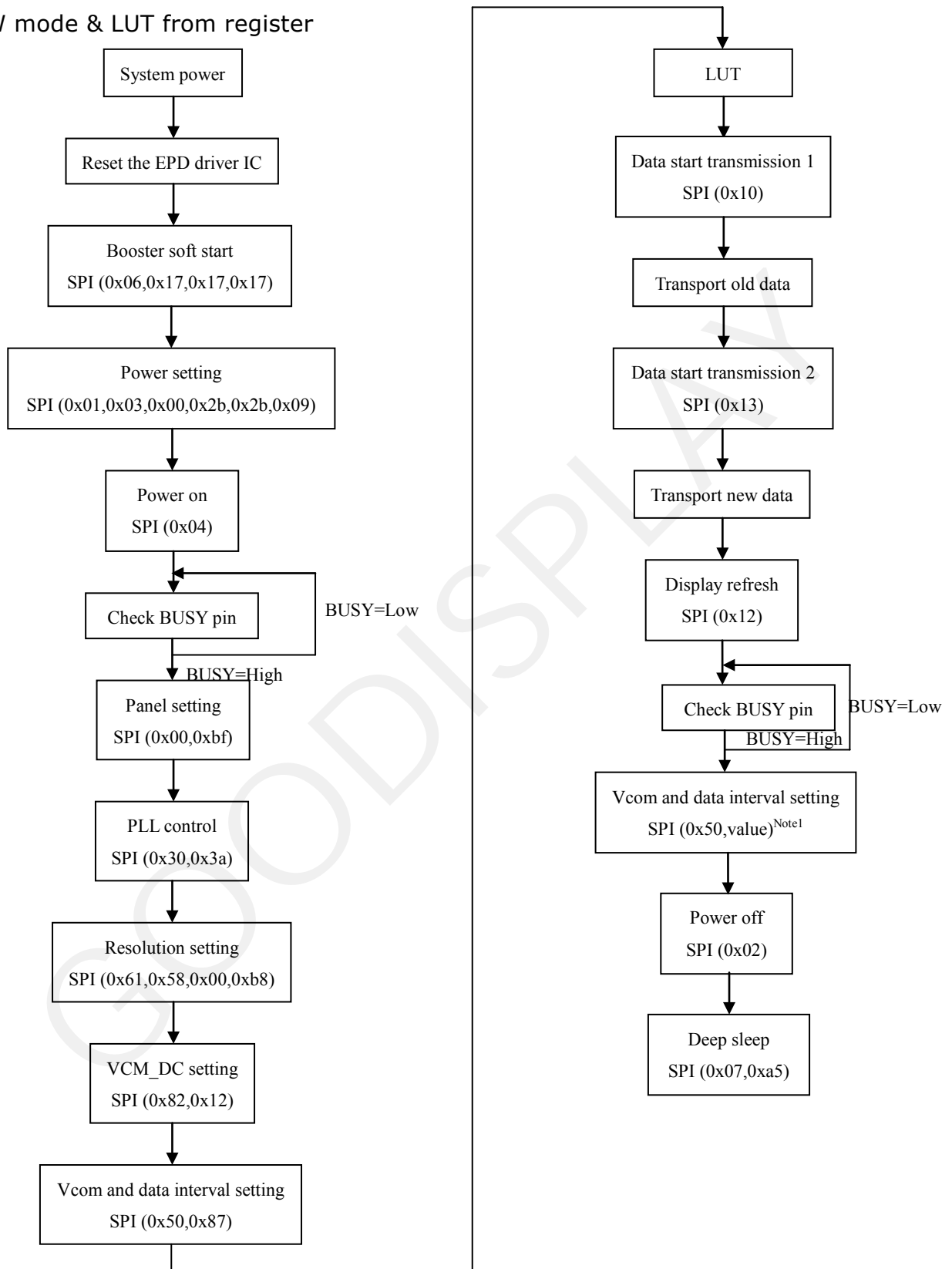


2. BW mode & LUT form OTP



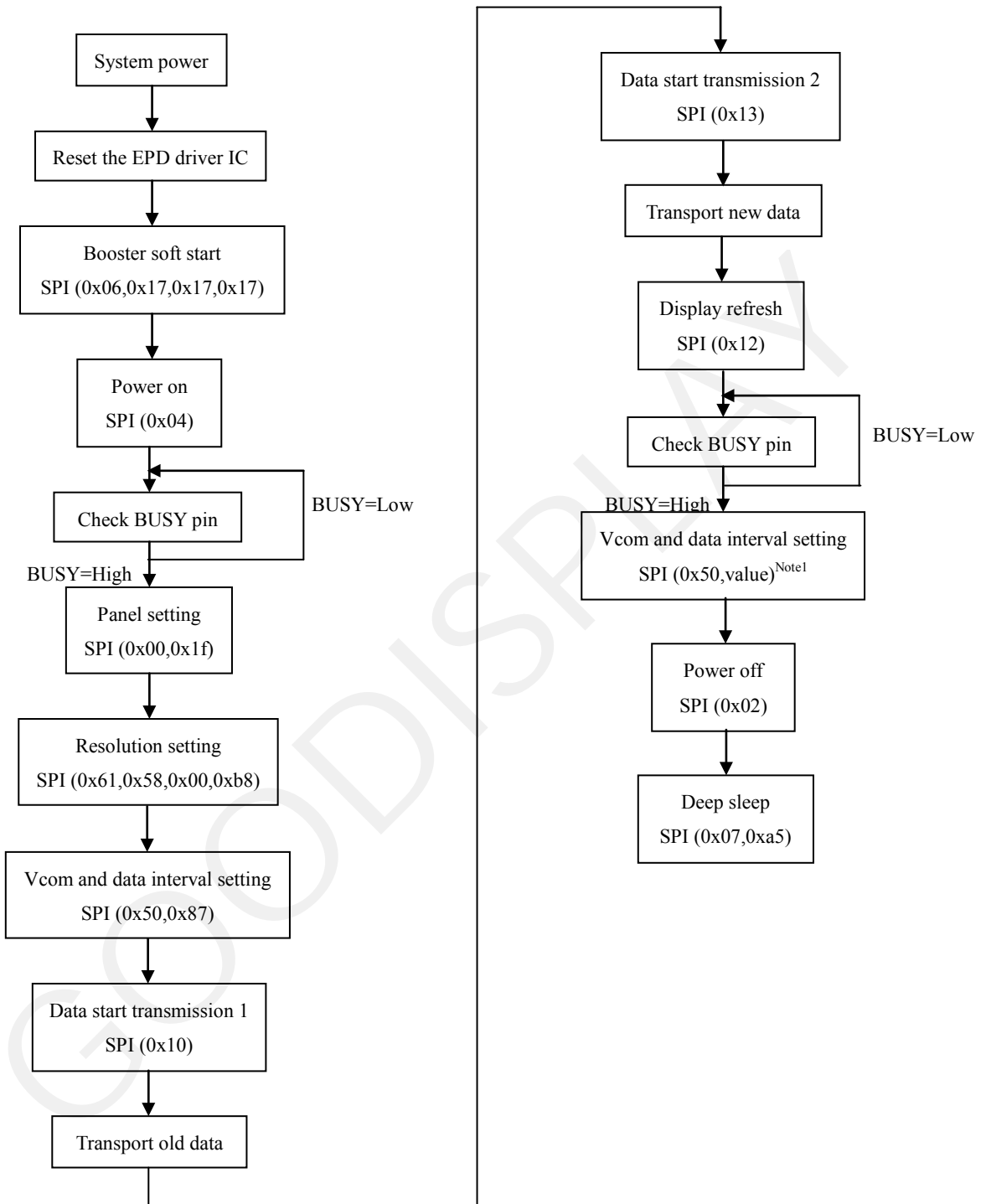
9.2 Reference Program Code

1. BW mode & LUT from register



Note1: Set border to floating.

2. BW mode & LUT from OTP



Note1: Set border to floating.

10. Optical characteristics

10.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 10-1
Gn	4 Grey Level	-	-	$DS+(WS-DS) \times n(m-1)$	-	L*	-
CR	Contrast Ratio	indoor	9		-	-	-
Panel's life		0°C~50°C		1000000 times or 5 years			Note 10-2

WS: White state, DS: Dark state

Gray state from Dark to White : DS、WS

m: 2

Note 10-1: Luminance meter: Eye – One Pro Spectrophotometer

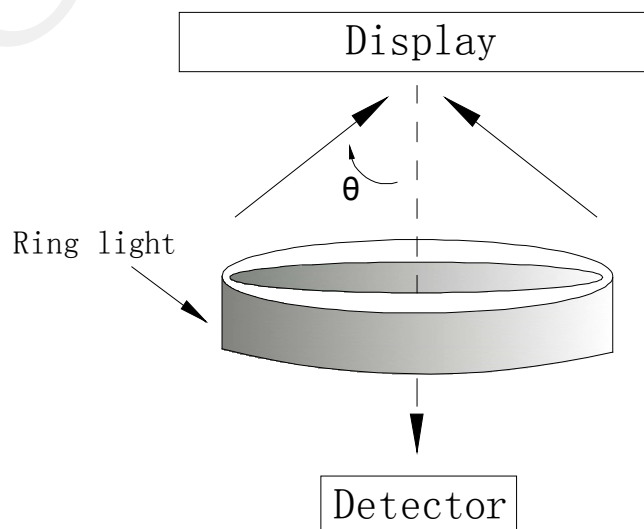
Note 10-2: Panel life will not guaranteed when work in temperature below 0 degree or above 50 degree. Each update interval time should be minimum at 180 seconds.

10.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd)(): R1: white reflectance

Rd: dark reflectance

$$CR = R1/Rd$$

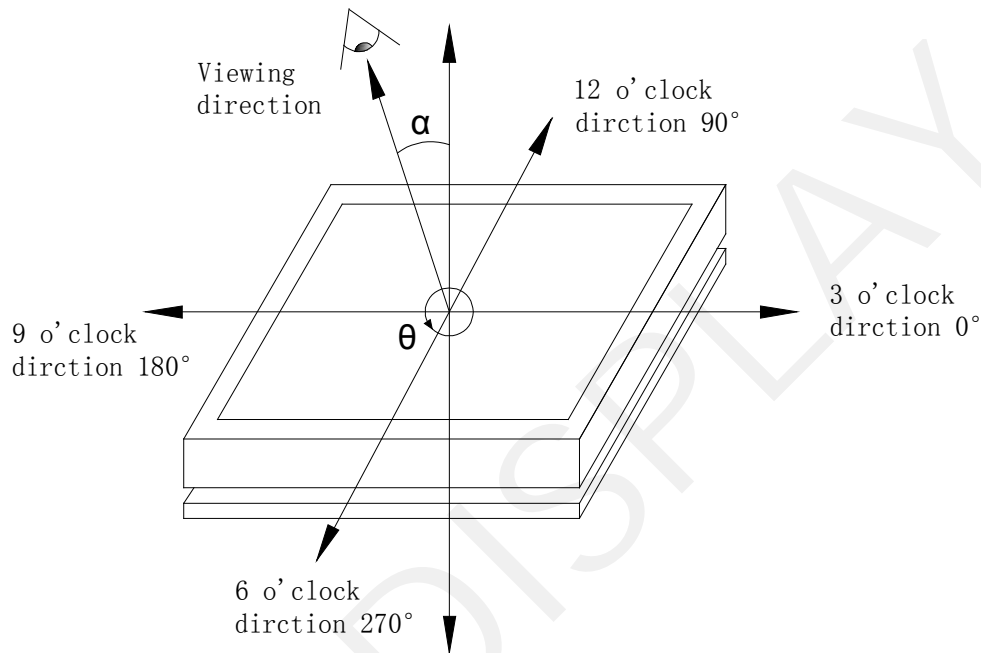


10.3 Reflection ratio

The reflection ratio is expressed as:

$$R = \text{Reflectance Factor white board} \times (L_{\text{center}} / L_{\text{white board}})$$

L_{center} is the luminance measured at center in a white area ($R=G=B=1$). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



11. Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T=50°C, RH=35% for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Bp.	When experiment finished, the EPD must meet electrical and optical performance standards.
2	Low-Temperature Operation	T = 0°C for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Ab.	When experiment finished, the EPD must meet electrical and optical performance standards.
3	High-Temperature Storage	T=+70°C, RH=35% for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Bp.	When experiment finished, the EPD must meet electrical and optical performance standards.
4	Low-Temperature Storage	T = -25°C for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-2Ab	When experiment finished, the EPD must meet electrical and optical performance standards.
5	High Temperature, High-Humidity Operation	T=+40°C, RH=80% For 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-3CA.	When experiment finished, the EPD must meet electrical and optical performance standards.
6	High Temperature, High-Humidity Storage	T=+60°C, RH=80% for 192 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-3CA.	When experiment finished, the EPD must meet electrical performance standards.
7	Temperature Cycle	[-25°C 30mins]→ [+70°C, RH=35% 30mins],	1. Samples are put in the Temp & Humid. Environmental Chamber. Temperature cycle starts with -25°C, storage period 30 minutes. After 30 minutes, it needs 30min to	When experiment finished, the EPD must meet electrical

		100 cycles Test in white pattern	<p>let temperature rise to 70°C. After 30min, temperature will be adjusted to 70°C, RH=35%, and storage period is 30 minutes. After 30 minutes, it needs 30min to let temperature rise to -25°C. One temperature cycle (2hrs) is complete.</p> <p>2. Temperature cycle repeats 100 times.</p> <p>3. When 100 cycles finished, the samples will be taken out from experiment chamber and set aside a few minutes. As EPDs return to room temperature, tests will observe the appearance, and test electrical and optical performance based on standard # IEC 60 068-2-14NB.</p>	and optical performance standards.
8	UV exposure Resistance	765 W/m ² for 168 hrs,40°C	Standard # IEC 60 068-2-5 Sa	
9	Electrostatic discharge	Machine model: +/-250V, 0 Ω ,200pF	Standard # IEC61000-4-2	
10	Package Vibration	1.04G, Frequency : 10~500Hz Direction : X,Y,Z Duration:1hours in each direction	Full packed for shipment	
11	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3 edges, 6 face One drop for each.	Full packed for shipment	

Actual EMC level to be measured on customer application.

Note: (1) The protective film must be removed before temperature test.

(2) In order to make sure the display module can provide the best display quality, the update should be made after putting the display module in stable temperature environment for 4 hours at 25 .

12. Point and line standard

Part-A: Active area


Part-B: Border area

Equipment: Electrical test fixture, Point gauge

Outline dimension:

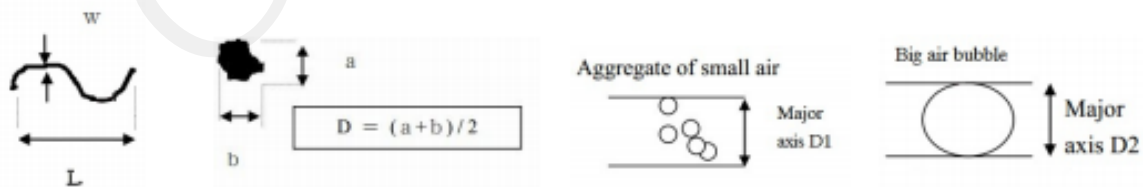
14.3(H)×30.15(V)×0.98(D)

Unit: mm

Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	23 ± 2°C	55 ± 5%RH	1200~1500Lux	300 mm	35 Sec	
Name	Causes	Spot size			Part-A	Part-B
Spot	B/W spot in glass or protection sheet, foreign mat. Pin hole	$D \leq 0.15\text{mm}$			Ignore	Ignore
		$0.15\text{mm} < D \leq 0.25\text{mm}$			2	
		$0.25\text{mm} < D$			0	
Scratch or line defect	Scratch on glass or Scratch on FPL or Particle is Protection sheet.	Length	Width		Part-A	Ignore
		$L \leq 1.0\text{mm}$	$W \leq 0.1\text{mm}$		Ignore	
		$1.0\text{mm} < L \leq 2.5\text{mm}$	$0.1\text{mm} < W \leq 0.2\text{mm}$		2	
		$2.5\text{mm} < L$	$0.2\text{mm} < W$		0	
Air bubble	Air bubble	$D1, D2 \leq 0.15\text{mm}$			Ignore	Ignore
		$0.15\text{mm} < D1, D2 \leq 0.2\text{mm}$			2	
		$0.2\text{mm} < D1, D2$			0	
Side Fragment						
	$X \leq 3\text{mm}, Y \leq 0.5\text{mm}$ & display is ok, Ignore					

Remarks: Spot define: That only can be seen under WS or DS defects.

- Any defect which is visible under gray pattern or transition process but invisible under black and white is disregarded.
- Here is definition of the "Spot" and "Scratch or line defect".
Spot: $W > 1/4L$ Scratch or line defect: $W \leq 1/4L$
- Definition for L/W and D (major axis)
- FPC bonding area pad doesn't allowed visual inspection.



Note: AQL = 0.4

13. Handling, Safety and Environmental Requirements

WARNING

<p>The display glass may break when it is dropped or bumped on a hard surface. Handle with care.</p> <p>Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.</p>
--

CAUTION

<p>The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.</p>

<p>Disassembling the display module can cause permanent damage and invalidate the warranty agreements.</p>
--

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status

Product specification	The data sheet contains final product specifications.
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Limiting values

<p>Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134).</p>

<p>Stress above one or more of the limiting values may cause permanent damage to the device.</p>
--

<p>These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.</p>
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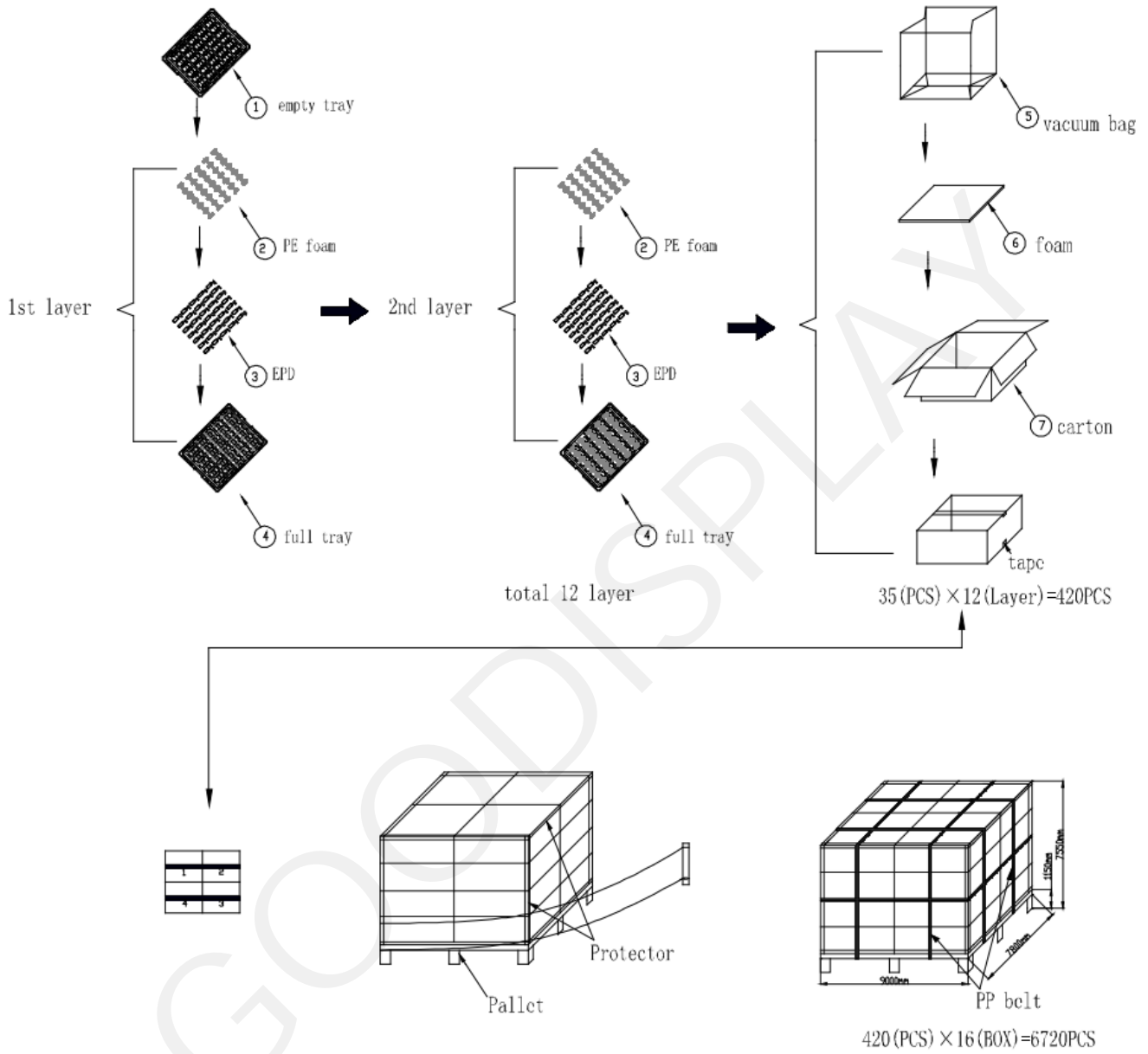
Application information

<p>Where application information is given, it is advisory and does not form part of the specification.</p>
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Product Environmental certification
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RoHS

14. Packing



15. Precautions

- (1) Do not apply pressure to the EPD panel in order to prevent damaging it.
- (2) Do not connect or disconnect the interface connector while the EPD panel is in operation.
- (3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.
- (4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.
- (5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue
- (6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.