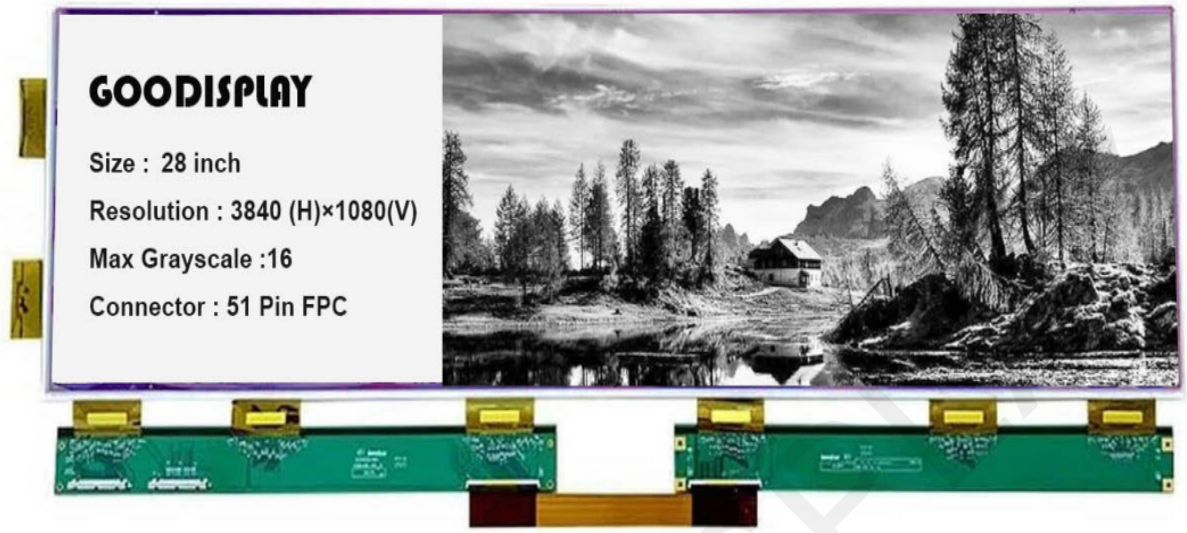
# 28.0 inch E-paper Display Series

# GDEP280T01

Dalian Good Display Co., Ltd.

# Product Specifications




| | |
|---|---|
| **Customer** | **Standard** |
| **Description** | **28.0" E-PAPER DISPLAY** |
| **Model Name** | **GDEP280T01** |
| **Date** | **2023/01/06** |
| **Revision** | **1.0** |

| | Design Engineering | | |
|---|---|---|---|
| | **Approval** | **Check** | **Design** |
| | 刘玉印宝 | 修燕凤印 | 吴良之印 |

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# CONTENTS

## 1. Overview

GDEP280T01 is a reflective electrophoretic technology display module based on active matrix TFT substrate. It has 28” active area with 3840 x 1080 pixels and 32:9 aspect ratio. The display is capable to display images at 16 Gray levels (1 to 4 bits) depending on the display controller and the associated waveform file it used.

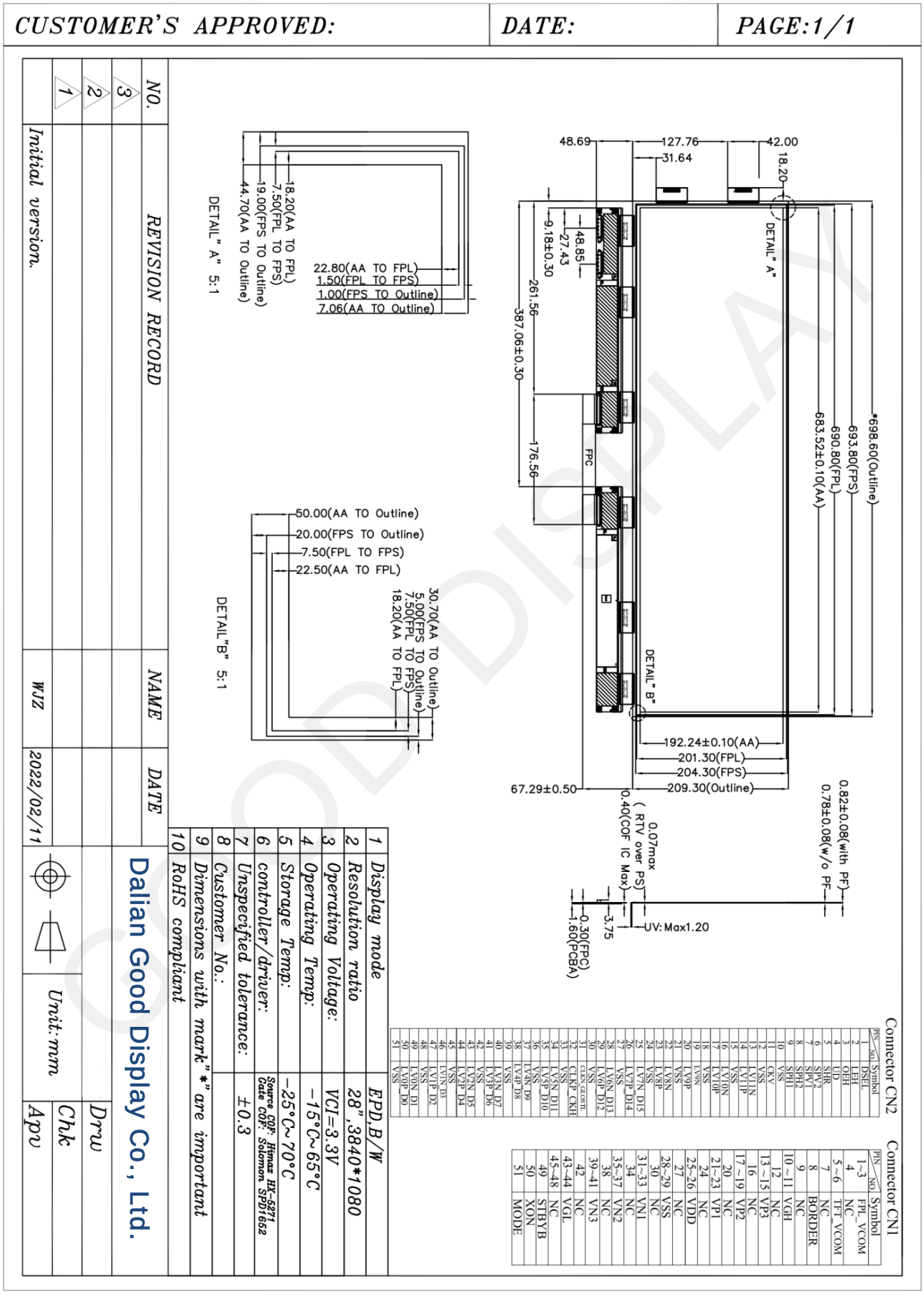
## 2.Features

- High contrast electrophoretic imaging film
- 3840 x 1080 display
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Landscape portrait modes
- Ultra wide viewing angle

## 3. Mechanical Specifications

| Parameter | Specifications | Unit | Remark |
|---|---|---|---|
| Screen Size | 28” | Inch | |
| Display Resolution | 3840 (H)×1080(V) | Pixel | 32:9 |
| Active Area | 683.52(H)×190.24(V) | mm | 143dpi |
| Pixel Pitch | 0.178 | mm | |
| Pixel Configuration | Square | | |
| Outline Dimension | 698.6(H)*209.3(V)*0.953(D) | mm | |
| Module Weight | TBD | g | |
| Number of Gray | 16 Gray Level | | |
| Display operating mode | Reflective mode | | |
| Glass Substrate | 0.5mm | mm | |
| Surface Treatment | Anti-glare | | |
| Driver IC | Source COF: Himax HX-5271<br>Gate COF: Solomon SPD1652 | | |

# 4. Mechanical Drawing of EPD module




| PIN_NO | Symbol |
|---|---|
| 1 | DSEL |
| 2 | LEH |
| 3 | OEH |
| 4 | UD |
| 5 | SHR |
| 6 | SPV2 |
| 7 | SPV1 |
| 8 | SPH2 |
| 9 | SPH1 |
| 10 | VSS |
| 11 | CKV |
| 12 | VSS |
| 13 | LV11N |
| 14 | LV11P |
| 15 | VSS |
| 16 | LV10N |
| 17 | LV10P |
| 18 | VSS |
| 19 | LV9N |
| 20 | LV9P |
| 21 | VSS |
| 22 | LV8N |
| 23 | LV8P |
| 24 | VSS |
| 25 | LV7N_D15 |
| 26 | LV7P_D14 |
| 27 | VSS |
| 28 | LV6N_D13 |
| 29 | LV6P_D12 |
| 30 | VSS |
| 31 | CLKN_GLOSTL |
| 32 | CLKP_CKH |
| 33 | VSS |
| 34 | LV5N_D11 |
| 35 | LV5P_D10 |
| 36 | VSS |
| 37 | LV4N_D9 |
| 38 | LV4P_D8 |
| 39 | VSS |
| 40 | LV3N_D7 |
| 41 | LV3P_D6 |
| 42 | VSS |
| 43 | LV2N_D5 |
| 44 | LV2P_D4 |
| 45 | VSS |
| 46 | LV1N_D3 |
| 47 | LV1P_D2 |
| 48 | VSS |
| 49 | LV0N_D1 |
| 50 | LV0P_D0 |
| 51 | VSS |

| PIN_NO | Symbol |
|---|---|
| 1~3 | FPL_VCOM |
| 4 | NC |
| 5~6 | TFT_VCOM |
| 7 | NC |
| 8 | BORDER |
| 9 | NC |
| 10~11 | VGH |
| 12 | NC |
| 13~15 | VP3 |
| 16 | NC |
| 17~19 | VP2 |
| 20 | NC |
| 21~23 | VP1 |
| 24 | NC |
| 25~26 | VDD |
| 27 | NC |
| 28~29 | VSS |
| 30 | NC |
| 31~33 | VN1 |
| 34 | NC |
| 35~37 | VN2 |
| 38 | NC |
| 39~41 | VN3 |
| 42 | NC |
| 43~44 | VGL |
| 45~48 | NC |
| 49 | STBYB |
| 50 | XON |
| 51 | MODE |

# 5. Input /Output Terminals

## 5.1 Connector type

| Item | Pin numbers | Pitch (mm) | Connector | Note |
|---|---|---|---|---|
| CN1 | 51 | 0.5 | P-TWO 187059-51221-1 | LVDS Type |
| CN2 | 51 | 0.5 | P-TWO 187059-51221-1 | LVDS Type |

## 5.2 Pin Assignment

## Connector CN1

| Pin # | Signal | Description | Remark |
|---|---|---|---|
| 1 | FPL_VCOM | Common Voltage. | |
| 2 | FPL_VCOM | Common Voltage. | |
| 3 | FPL_VCOM | Common Voltage. | |
| 4 | NC | NO Connection | |
| 5 | TFT_VCOM | Common Voltage. | |
| 6 | TFT_VCOM | Common Voltage. | |
| 7 | NC | NO Connection | |
| 8 | BORDER | Border connection | |
| 9 | NC | NO Connection | |
| 10 | VGH | Positive power supply gate driver. | |
| 11 | VGH | Positive power supply gate driver. | |
| 12 | NC | NO Connection | |
| 13 | VP3 | Positive power supply source driver. | |
| 14 | VP3 | Positive power supply source driver. | |
| 15 | VP3 | Positive power supply source driver. | |
| 16 | NC | NO Connection | |
| 17 | VP2 | Positive power supply source driver. | |
| 18 | VP2 | Positive power supply source driver. | |
| 19 | VP2 | Positive power supply source driver. | |
| 20 | NC | NO Connection | |
| 21 | VP1 | Positive power supply source driver. | |
| 22 | VP1 | Positive power supply source driver. | |
| 23 | VP1 | Positive power supply source driver. | |
| 24 | NC | NO Connection | |
| 25 | VDD | Logic power. | |
| 26 | VDD | Logic power. | |
| 27 | NC | NO Connection | |
| 28 | VSS | Ground | |
| 29 | VSS | Ground | |
| 30 | NC | NO Connection | |
| 31 | VN1 | Negative power supply source driver. | |
| 32 | VN1 | Negative power supply source driver. | |
| 33 | VN1 | Negative power supply source driver. | |
| 34 | NC | NO Connection | |
| 35 | VN2 | Negative power supply source driver. | |
| 36 | VN2 | Negative power supply source driver. | |
| 37 | VN2 | Negative power supply source driver. | |
| 38 | NC | NO Connection | |
| 39 | VN3 | Negative power supply source driver. | |
| 40 | VN3 | Negative power supply source driver. | |
| 41 | VN3 | Negative power supply source driver. | |
| 42 | NC | NO Connection | |
| 43 | VGL | Negative power supply gate driver. | |
| 44 | VGL | Negative power supply gate driver. | |
| 45 | NC | NO Connection | |
| 46 | NC | NO Connection | |

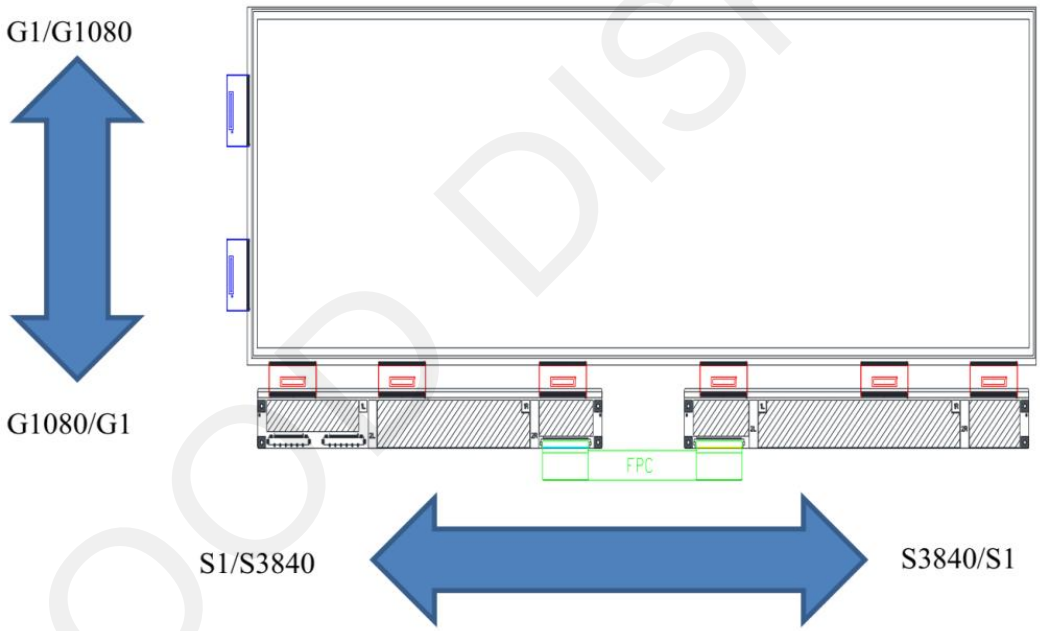
| | | | |
|---|---|---|---|
| 47 | NC | NO Connection | |
| 48 | NC | NO Connection | |
| 49 | STBYB | mini-LVDS enable. | |
| 50 | XON | XON signal gate driver | |
| 51 | MODE | Output enable gate driver | |

## Connector CN2

<table>
<tr><th>Pin #</th><th>Signal</th><th>Description</th><th>Remark</th></tr>
<tr><td>1</td><td>DSEL</td><td>Data Input select</td><td></td></tr>
<tr><td>2</td><td>LEH</td><td>Latch enable source driver</td><td></td></tr>
<tr><td>3</td><td>OEH</td><td>Outputs enabled when OE is logic “H”,<br>Outputs forced to GND when OE is logic “L”.</td><td></td></tr>
<tr><td>4</td><td>UD</td><td>Shift direction control pin gate driver<br>UD = H: Data shift direction from G1 to G800.<br>UD = L: Data shift direction from G800 to G1.</td><td></td></tr>
<tr><td>5</td><td>SHR</td><td>Shift direction control pin source driver<br>SHR =H: Data inputs read sequentially from S800 to S1.<br>SHR =L: Data inputs read sequentially from S1 to S800.</td><td></td></tr>
<tr><td>6</td><td>SPV2</td><td>Start pulse gate driver<table><tr><td>UD</td><td>Start pulse input</td><td>Start pulse output</td></tr><tr><td>H</td><td>SPV1</td><td>SPV2</td></tr><tr><td>L</td><td>SPV2</td><td>SPV1</td></tr></table></td><td></td></tr>
<tr><td>7</td><td>SPV1</td><td>Start pulse gate driver<table><tr><td>UD</td><td>Start pulse input</td><td>Start pulse output</td></tr><tr><td>H</td><td>SPV1</td><td>SPV2</td></tr><tr><td>L</td><td>SPV2</td><td>SPV1</td></tr></table></td><td></td></tr>
<tr><td>8</td><td>SPH2</td><td>Start pulse source driver<table><tr><td>SHR</td><td>Start pulse input</td><td>Start pulse output</td></tr><tr><td>H</td><td>SPH2</td><td>SPH1</td></tr><tr><td>L</td><td>SPH1</td><td>SPH2</td></tr></table></td><td></td></tr>
<tr><td>9</td><td>SPH1</td><td>Start pulse source driver<table><tr><td>SHR</td><td>Start pulse input</td><td>Start pulse output</td></tr><tr><td>H</td><td>SPH2</td><td>SPH1</td></tr><tr><td>L</td><td>SPH1</td><td>SPH2</td></tr></table></td><td></td></tr>
<tr><td>10</td><td>VSS</td><td>Ground</td><td></td></tr>
<tr><td>11</td><td>CKV</td><td>Clock gate driver</td><td></td></tr>
<tr><td>12</td><td>VSS</td><td>Ground</td><td></td></tr>
<tr><td>13</td><td>LV11N</td><td>Data signal source driver</td><td></td></tr>
<tr><td>14</td><td>LV11P</td><td>Data signal source driver</td><td></td></tr>
<tr><td>15</td><td>VSS</td><td>Ground</td><td></td></tr>
<tr><td>16</td><td>LV10N</td><td>Data signal source driver</td><td></td></tr>
<tr><td>17</td><td>LV10P</td><td>Data signal source driver</td><td></td></tr>
<tr><td>18</td><td>VSS</td><td>Ground</td><td></td></tr>
<tr><td>19</td><td>LV9N</td><td>Data signal source driver</td><td></td></tr>
<tr><td>20</td><td>LV9P</td><td>Data signal source driver</td><td></td></tr>
<tr><td>21</td><td>VSS</td><td>Ground</td><td></td></tr>
<tr><td>22</td><td>LV8N</td><td>Data signal source driver</td><td></td></tr>
<tr><td>23</td><td>LV8P</td><td>Data signal source driver</td><td></td></tr>
<tr><td>24</td><td>VSS</td><td>Ground</td><td></td></tr>
<tr><td>25</td><td>LV7N_D15</td><td>Data signal source driver</td><td></td></tr>
<tr><td>26</td><td>LV7P_D14</td><td>Data signal source driver</td><td></td></tr>
<tr><td>27</td><td>VSS</td><td>Ground</td><td></td></tr>
<tr><td>28</td><td>LV6N_D13</td><td>Data signal source driver</td><td></td></tr>
<tr><td>29</td><td>LV6P_D12</td><td>Data signal source driver</td><td></td></tr>
<tr><td>30</td><td>VSS</td><td>Ground</td><td></td></tr>
</table>

| | | | |
|---|---|---|---|
| 31 | CLKN_GLOSTL | Data signal source driver | |
| 32 | CLKP_CKH | Data signal source driver | |
| 33 | VSS | Ground | |
| 34 | LV5N_D11 | Data signal source driver | |
| 35 | LV5P_D10 | Data signal source driver | |
| 36 | VSS | Ground | |
| 37 | LV4N_D9 | Data signal source driver | |
| 38 | LV4P_D8 | Data signal source driver | |
| 39 | VSS | Ground | |
| 40 | LV3N_D7 | Data signal source driver | |
| 41 | LV3P_D6 | Data signal source driver | |
| 42 | VSS | Ground | |
| 43 | LV2N_D5 | Data signal source driver | |
| 44 | LV2P_D4 | Data signal source driver | |
| 45 | VSS | Ground | |
| 46 | LV1N_D3 | Data signal source driver | |
| 47 | LV1P_D2 | Data signal source driver | |
| 48 | VSS | Ground | |
| 49 | LV0N_D1 | Data signal source driver | |
| 50 | LV0P_D0 | Data signal source driver | |
| 51 | VSS | Ground | |

## 5.3 Panel Scan direction



# 6. Electrical Characteristics

## 6.1 Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit | Remark |
|---|---|---|---|---|
| Logic Supply Voltage | VDD | -0.3 to +5.0 | V | |
| Positive Supply Voltage | VP3 | -0.3 to VN3+50 | V | |
| | VP2 | -0.3 to VP3 | V | |
| | VP1 | -0.3 to VP3 | V | |
| Negative Supply Voltage | VN1 | VN3 to + 0.3 | V | |
| | VN2 | VN3 to + 0.3 | V | |
| | VN3 | -25 to + 0.3 | V | |
| Supply Voltage | VGH | -0.3 to +55 | V | |
| Supply Voltage | VGL | -32 to +0.3 | V | |
| Supply Range | VGH-VGL | -0.3 to +55 | V | |
| Operating Temp. Range | TOTR | -15 to +65 | ℃ | |
| Storage Temperature | TSTG | -25 to +70 | ℃ | |

## 6.2 Panel DC Characteristics

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Signal ground | VSS | | | 0 | | V |
| Logic voltage supply | VDD | | 2.7 | 3.3 | 3.6 | V |
| | IDD | VDD=3.3V | | | TBD | mA |
| Gate Negative supply | VGL | | -19 | -20 | -21 | V |
| | IGL | VGL=-20V | | | TBD | mA |
| Gate Positive supply | VGH | | 26 | 27 | 28 | V |
| | IGH | VGH=27V | | | TBD | mA |
| Source Negative supply | VN1 | | -16 | -15 | -14 | V |
| | IN1 | | | | TBD | mA |
| Source Negative supply | VN2 | | -13 | -12 | -11 | V |
| | IN2 | | | | TBD | mA |
| Source Negative supply | VN3 | | -21 | -20 | -19 | V |
| | IN3 | | | | TBD | mA |
| Source Positive supply | VP1 | | 14 | 15 | 16 | V |
| | IP1 | | | | TBD | mA |
| Source Positive supply | VP2 | | 11 | 12 | 13 | V |
| | IP2 | | | | TBD | mA |
| Source Positive supply | VP3 | | 19 | 20 | 21 | V |
| | IP3 | | | | TBD | mA |
| Border supply | - | | - | - | - | V |
| Asymmetry source | Vasm | VP1+VN1 | TBD | | TBD | mV |
| Common voltage | Vcom_TFT | | -3.5 | Adjusted | -0.3 | V |
| | Icom_TFT | | | TBD | TBD | mA |

| | | | | | | |
|---|---|---|---|---|---|---|
| | Vcom_FPL | | -3.5 | Adjusted | -0.3 | V |
| | Icom_FPL | | | TBD | TBD | mA |
| Maximum Power panel | Pmax | | | | TBD | mW |
| Typical power panel | Ptyp | | | TBD | | mW |
| Standby power panel | Pstby | | | | TBD | mW |
| Maximum Currents (Note 5) | IP1 | VP1 = 15V | - | | TBD | mA |
| | IN1 | VN1 = -15V | - | | TBD | mA |
| | IGH | VGH = 27V | - | | TBD | mA |
| | IGL | VGL =-20V | - | | TBD | mA |
| | ICOM | | - | | TBD | mA |

Note:

1. The maximum average Currents for power consumption are measured using 75 Hz waveform with following pattern transition: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-1)
2. The Typical average current for power consumption is measured using 75 Hz waveform with following pattern transition: from horizontal 4 gray scale pattern to vertical 4 gray scale pattern.(Note 6-2)
3. The standby power is the consumed power when the panel controller is in standby mode.
4. The Maximum Currents are measured using 75 Hz waveform with following pattern transition:from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-1)

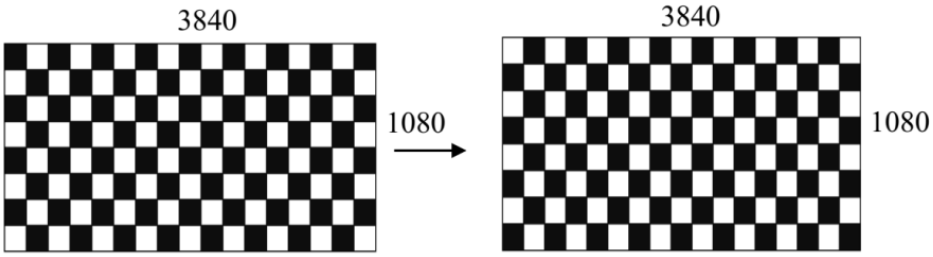
- It is performed with decoupling capacitors on each power rail as below table (Note 6-3).

- The minimum value in table of Maximum current is produced by charging mechanism between decoupling capacitors.

5. The listed electrical/optical characteristics are only guaranteed under the controller and waveform provided by NEWFACE.
6. Vcom is recommended to be set in the range of assigned value ±0.1 V.
7. Use of measuring instruments: Oscilloscope (Model: Tektronix MDO3024).
8. The maximum current is for reference only.

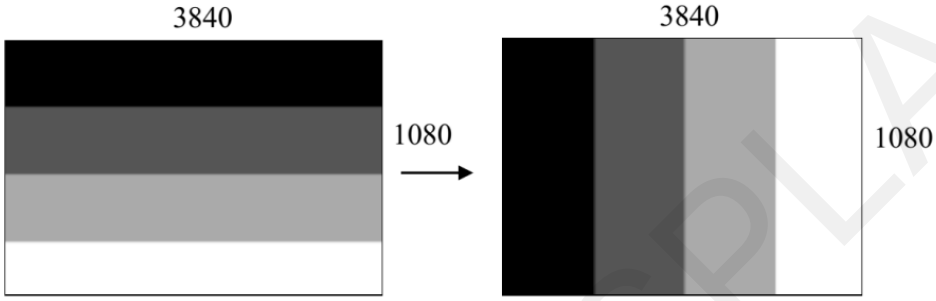
Note6-1

The maximum average current and Maximum Currents




Note6-2

The typical power consumption




Note6-3

The decoupling capacitors on each power rail for Max. Currents

| Power rail | Capacitors suggested ( uF / Tolerance) |
|---|---|
| IDD | 2.2uF x 14pcs / ±10% |
| IP1 | 2.2uF x 12pcs / ±10% |
| IP2 | 2.2uF x 12pcs / ±10% |
| IP3 | 2.2uF x 12pcs / ±10% |
| IN1 | 2.2uF x 12pcs / ±10% |
| IN2 | 2.2uF x 12pcs / ±10% |
| IN3 | 2.2uF x 12pcs / ±10% |
| IGH | 2.2uF x 2pcs / ±10% |
| IGL | 2.2uF x 3pcs / ±10% |
| ICOM | No Capacitor |

## 6.3 Refresh Rate

The module is applied at a maximum screen refresh rate of 75Hz.

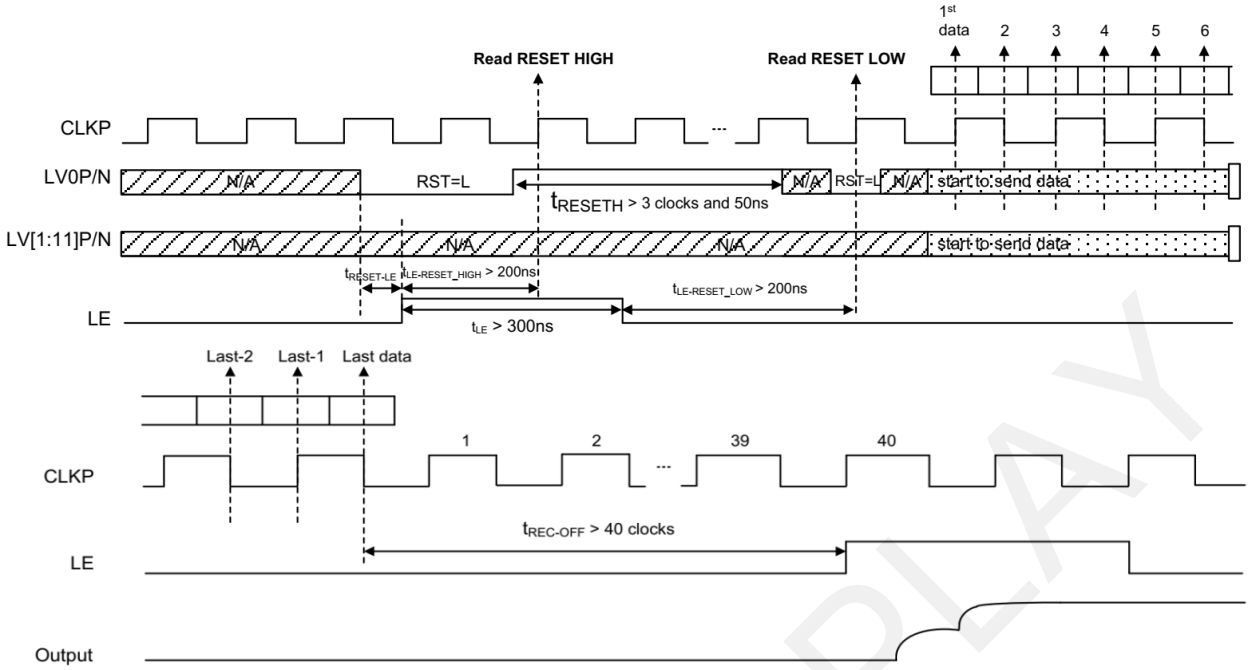
| | Min | Max |
|---|---|---|
| Refresh Rate | - | 75 Hz |

## 6.4. Panel AC characteristics

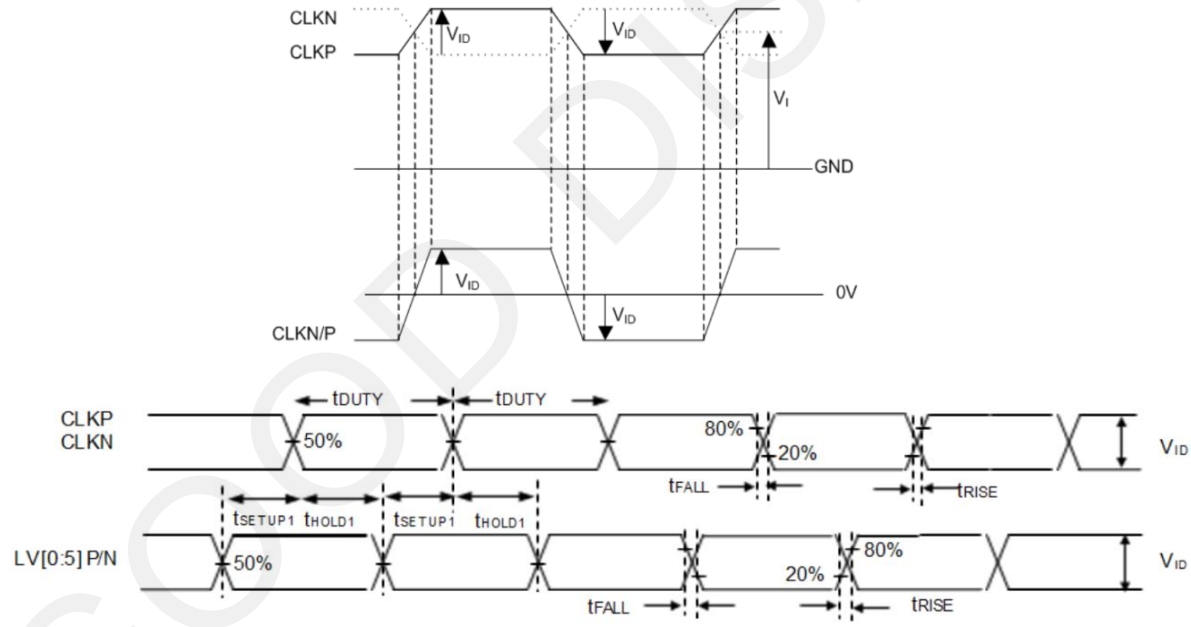
VDD=2.7V to 3.6V, unless otherwise specified.

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| mini-LVDS differential voltage | $V_{ID}$ | 300 | - | - | mV |
| mini-LVDS common mode input voltage range | $V_I$ | 0.4 | 1.0 | VDD-1.4 | V |
| Source Clock frequency | $F_{CLK}$ | - | - | 150 | MHz |
| Source Clock duty | $t_{DUTY}$ | 45 | - | 55 | % |
| Source Clock setup time | $t_{SETUP1}$ | 1.1 | - | - | ns |
| Source Clock hold time | $t_{HOLD1}$ | 1.1 | - | - | ns |
| Rise time | $t_{RISE}$ | - | - | 0.15 | Unit interval |
| Fall time | $t_{FALL}$ | - | - | 0.15 | Unit interval |
| LE rising to reset input time | $t_{LE\text{-}RESET\_HIGH}$ | 200 | - | - | ns |
| LE falling to reset input time | $t_{LE\text{-}RESET\_LOW}$ | 200 | - | - | ns |
| Start pulse delay time | $t_{PLH1}$ | - | - | 4 | CLK |
| | $t_{PHL1}$ | - | - | 4 | CLK |
| Reset high period | $t_{RESETH}$ | 3 | - | - | CLK |
| Receiver off to LE timing | $t_{REC\text{-}OFF}$ | 40 | - | - | CLK |
| LE width | $t_{LE}$ | 300 | - | - | ns |
| Reset low to LE rising time | $t_{RESET\text{-}LE}$ | 0 | - | - | ns |
| Gate clock frequency | $f_{CLK}$ | - | - | 200 | kHz |
| Gate clock pulse high period | $t_{CLKH}$ | 500 | - | - | ns |
| Gate clock pulse low period | $t_{CLKL}$ | 500 | - | - | ns |
| Gate clock rise time | $t_{IR\_CLK}$ | - | - | 100 | ns |
| Gate clock fall time | $t_{IF\_CLK}$ | - | - | 100 | ns |
| Gate Start pulse setup time | $t_{SU}$ | 100 | - | $t_{CLKH}$-100 | ns |
| Gate Start pulse hold time | $t_{HD}$ | 100 | - | $t_{CLKL}$-100 | ns |
| Gate Start pulse rise time | $t_{IR\_STV}$ | - | - | 100 | ns |
| Gate Start pulse fall time | $t_{IF\_STV}$ | - | - | 100 | ns |
| Gate STV output delay from CLK | $t_{OD\_STV}$ | - | - | 500 | ns |
| Output delay time from CLK | $t_{D\_OUT}$ | - | - | 2 | us |
| Output rise time, output pins | $t_{R\_OUT}$ | - | - | 1 | us |
| Output fall time, output pins | $t_{F\_OUT}$ | - | - | 1 | us |
| XONL/R pulse width | $t_{WXON}$ | 10 | - | - | us |
| Output delay time from XON | $t_{DXON\_OUT}$ | - | - | 20 | us |

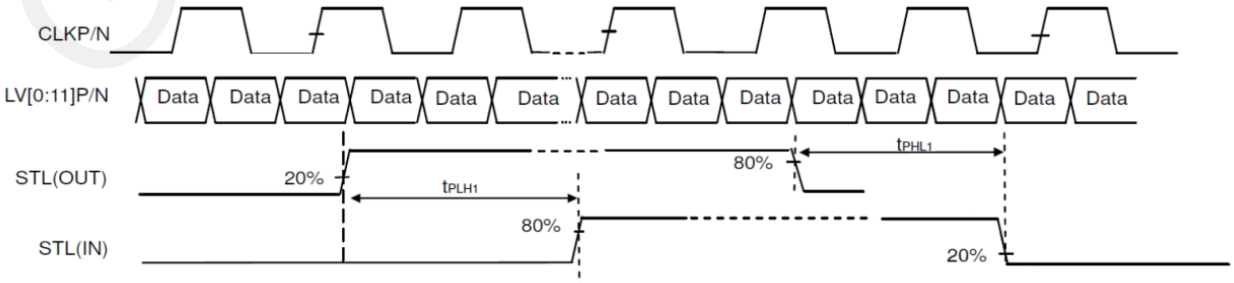
## OUTPUT LATCH CONTROL SIGNALS

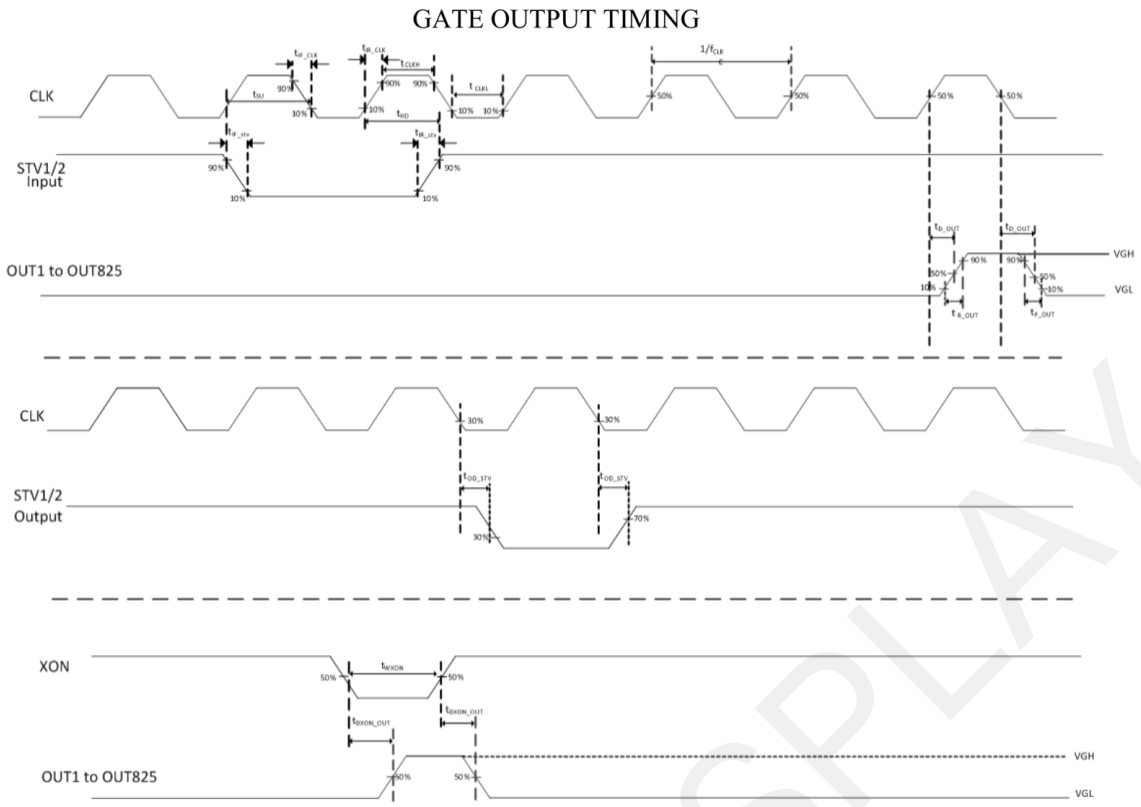



## CLOCK & DATA TIMING




## CKV & SPV TIMING






Note : First gate line on timing

After 5CLK, Gate OUT1 is on.

## 6.5 Controllers Timing

The timing mode is depicted on Figure 6.1 and Figure 6.2 and it refers to timing of Source Driver Output Enable (SDOE) and Gate Driver Clock (GDCK). Note, the controller timing in the mode LGON follows GDCK timing.

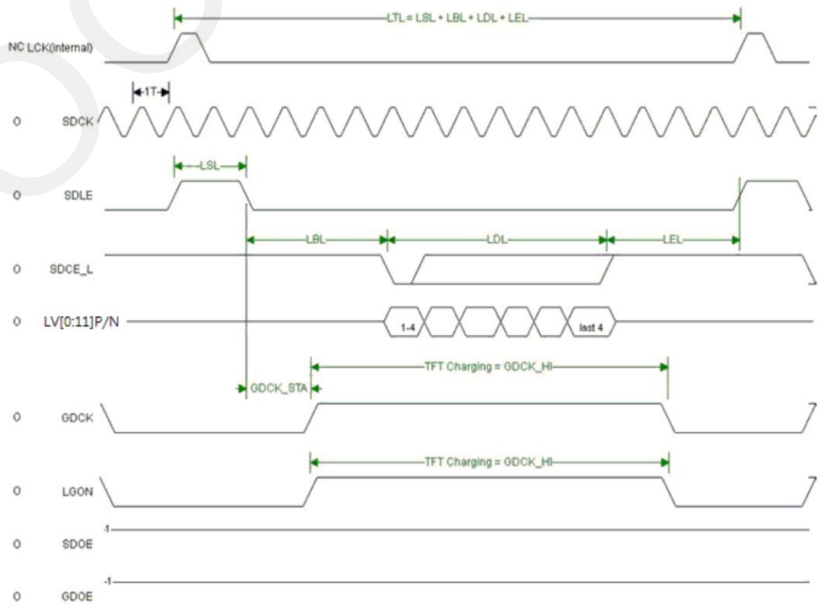



**Figure 6.1 Line Timing in Mode 3**

Note:LCK is an internal signal and it is shown for reference only.

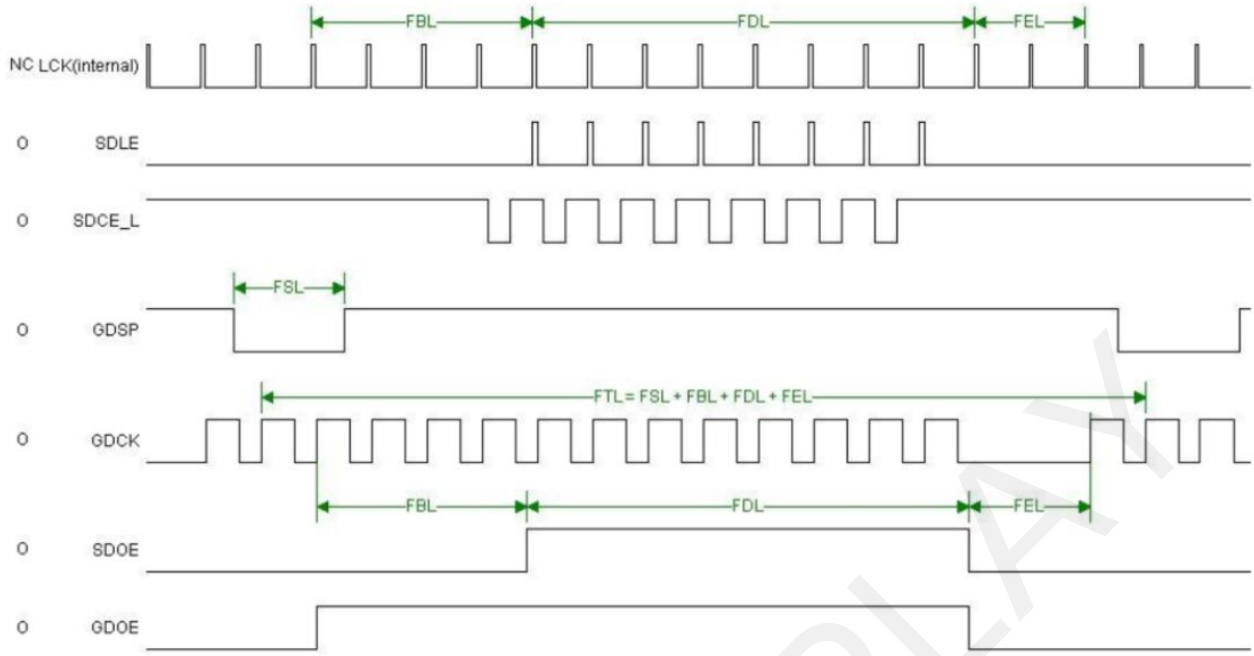



**Figure 6.2 Frame Timing in Mode 3**

Note 1: For Free scale SoC GDOE Low pulse represent FSL and GDSP pulses with the first period of FBL

Note 2:

SDCLK = XCL

LV[0:11]P/N = LV0P~LV11N SDCE_L = XSTL

GDCK = CKV

GDSP = SPV

GDOE = Mode1

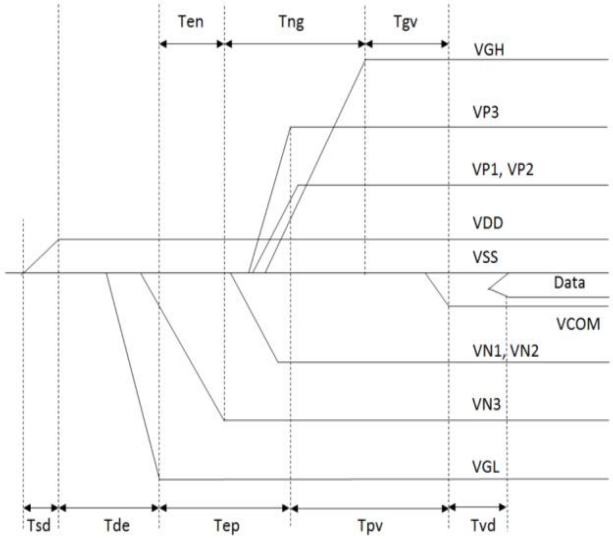
SDOE = XOE

## 7. Power on Sequence

Power Rails must be sequenced in the following order：

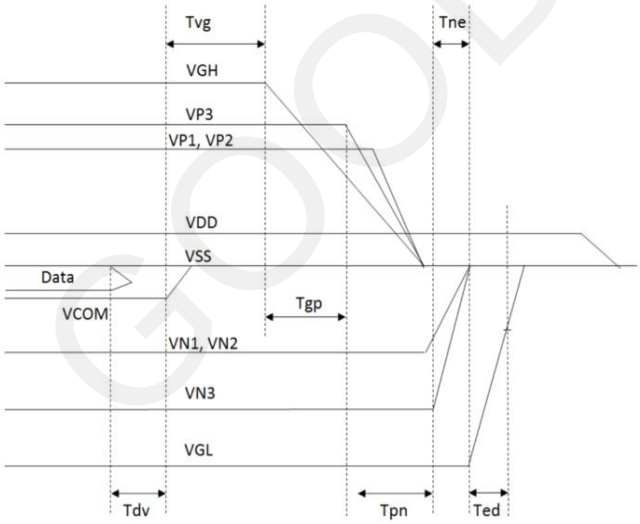
1. VSS →VDD →VN3 →VN1(VN2) →VP1(VP2) →VP3 →VCOM
2. VSS →VDD →VGL →VGH (Gate driver)

POWER ON




| | Min | Max | Remark |
|---|---|---|---|
| Tsd | 30us | - | |
| Tde | 100us | - | |
| Tep | 1000us | - | |
| Tpv | 100us | - | |
| Tvd | 100us | - | |
| Ten | 0us | - | |
| Tng | 1000us | - | |
| Tgv | 100us | - | |

POWER OFF




| | Min | Max | Remark |
|---|---|---|---|
| Tdv | 100μs | - | - |
| Tvg | 0μs | - | - |
| Tgp | 0μs | - | - |
| Tpn | 0μs | - | - |
| Tne | 0μs | - | - |
| Ted | 0.5s | - | Discharged point @ -7.4 Volt |

# 8. Optical Characteristics

## 8.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

T = 25°C

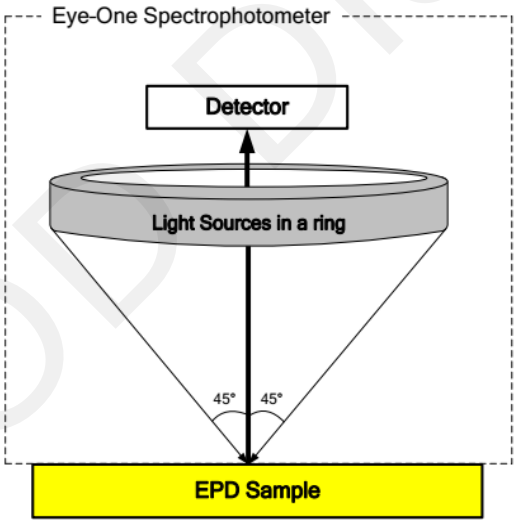
| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| R | Reflectance | White | 30 | 40 | - | % | Note 8-1 |
| Gn | $N_{th}$ Grey Level | - | - | DS+(WS-DS)×n/(m-1) | - | L* | - |
| CR | Contrast Ratio | - | 10 | 12 | - | | |

WS: White state , DS: Dark state, Gray state from Dark to White :DS、G1、G2…、Gn…、Gm-2、WS m:4、8、16 when 2、3、4 bits mode

8-1. Luminance meter: Eye –One Pro Spectrophotometer

## 8.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectancein a dark area (Rd): CR = Rl/Rd.




## 8.3 Reflection Ratio

The reflection ratio is expressed as:
R = Reflectance Factorwhite board x ( Lcenter / Lwhite board )
Lcenter is the luminance measured at center in a white area (R=G=B=1). Lwhite board is the luminance of astandard white board. Both are measured with equivalent illumination source. The viewing angle shallbe no more than 2 degrees.

# 9. Handling, Safety and Environmental Requirements

| WARNING |
| --- |
| The display glass may break when it is dropped or bumped on a hard surface. Handle with care.<br>Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap. |

| CAUTION |
| --- |
| The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. |
| Disassembling the display module can cause permanent damage and invalidate the warranty agreements. |

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

| Data sheet status | |
| --- | --- |
| Product specification | The data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134).<br>Stress above one or more of the limiting values may cause permanent damage to the device.<br>These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and dose not form part of the specification. | |

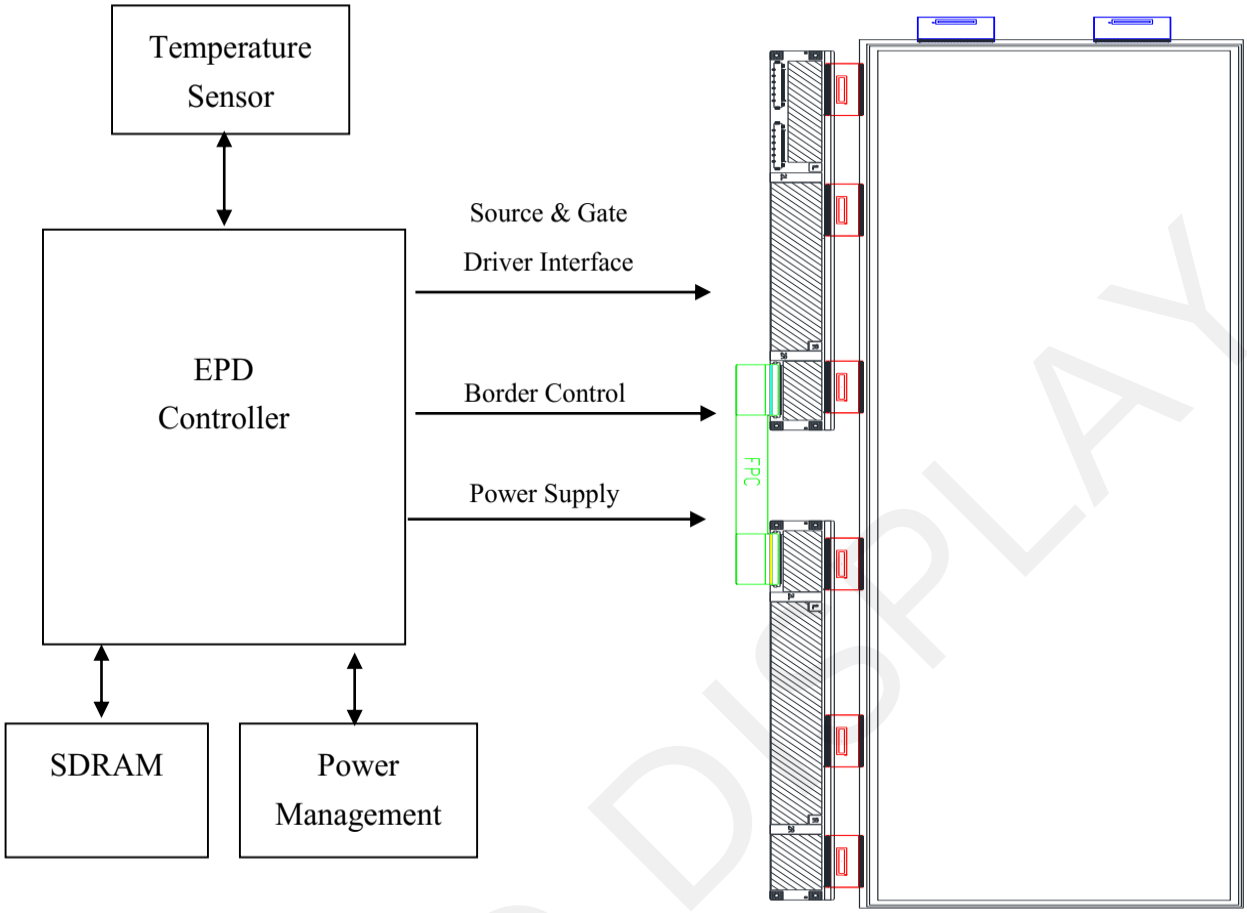
| Product Environmental certification |
| --- |
| RoHS |

## 10. Reliability Test

| | TEST | CONDITION | METHOD | REMARK |
|---|---|---|---|---|
| 1 | High-Temperature Operation | T = +65°C, RH = 30% for 240 hrs | IEC 60 068-2-2Bp | |
| 2 | Low-Temperature Operation | T = -15°C for 240 hrs | IEC 60 068-2-2Ab | |
| 3 | High-Temperature Storage | T = +70°C, RH=23% for 240 hrs<br>Test in white pattern | IEC 60 068-2-2Bp | |
| 4 | Low-Temperature Storage | T = -25°C for 240 hrs<br>Test in white pattern | IEC 60 068-2-1Ab | |
| 5 | High-Temperature,<br>High-Humidity Operation | T = +40°C, RH = 90% for 168 hrs | IEC 60 068-2-3CA | |
| 6 | Temperature Cycle | -25℃→+70℃, 100 Cycles<br>30min 30min<br>Test in white pattern | IEC 60 068-2-14 | |
| 7 | Solar radiation test | 765 W/m2,168hrs,40℃ | IEC60 068-2-5Sa | |
| 8 | Package Vibration | Random Wave (1.5Grms)<br>Frequency: 10~200Hz<br>Direction: X,Y,Z<br>Duration: 30mins each direction | Full packed for shipment | |
| 9 | Package Drop Impact | Drop from height of 15.2 cm<br>on concrete surface.<br>Drop sequence: 6 flats | Full packed for shipment | |
| 10 | Electrostatic Effect<br>(non-operating) | (Machine model)+/- 250V<br>0Ω, 200pF | IEC 62179, IEC 62180 | |
| 11 | Electrostatic Effect<br>(non-operating) | (ESD gun) Air 15k, Contact 8k | IEC 62179, IEC 62180 | |

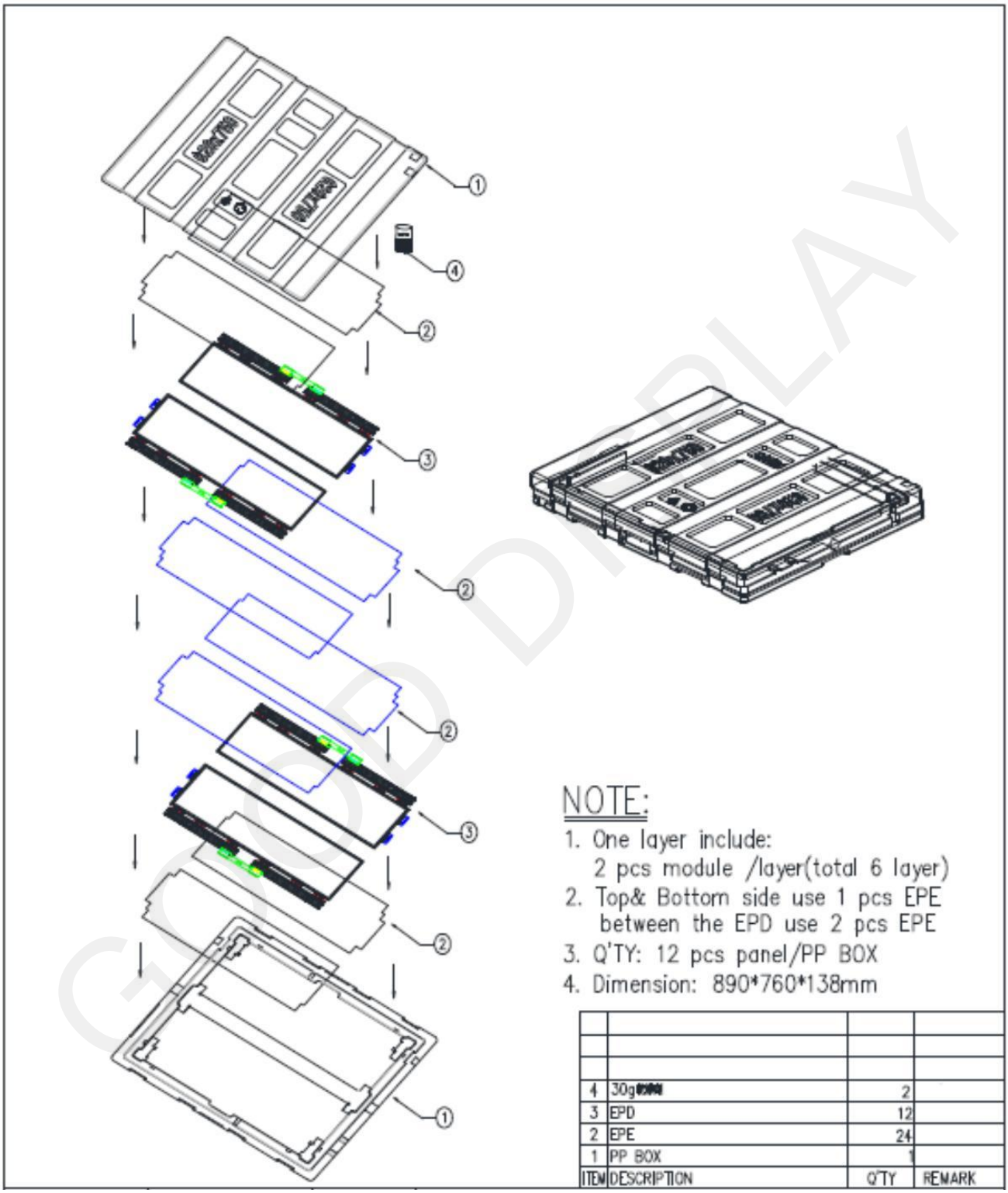
Actual EMC level to be measured on customer application
Note: The protective filmmust be removed before temperature test.
< Criteria >
In the standard conditions, there is not display function NG issue occurred. (Including: line defect, noimage). All the cosmetic specification is judged before the reliability stress.

## 11. Block Diagram

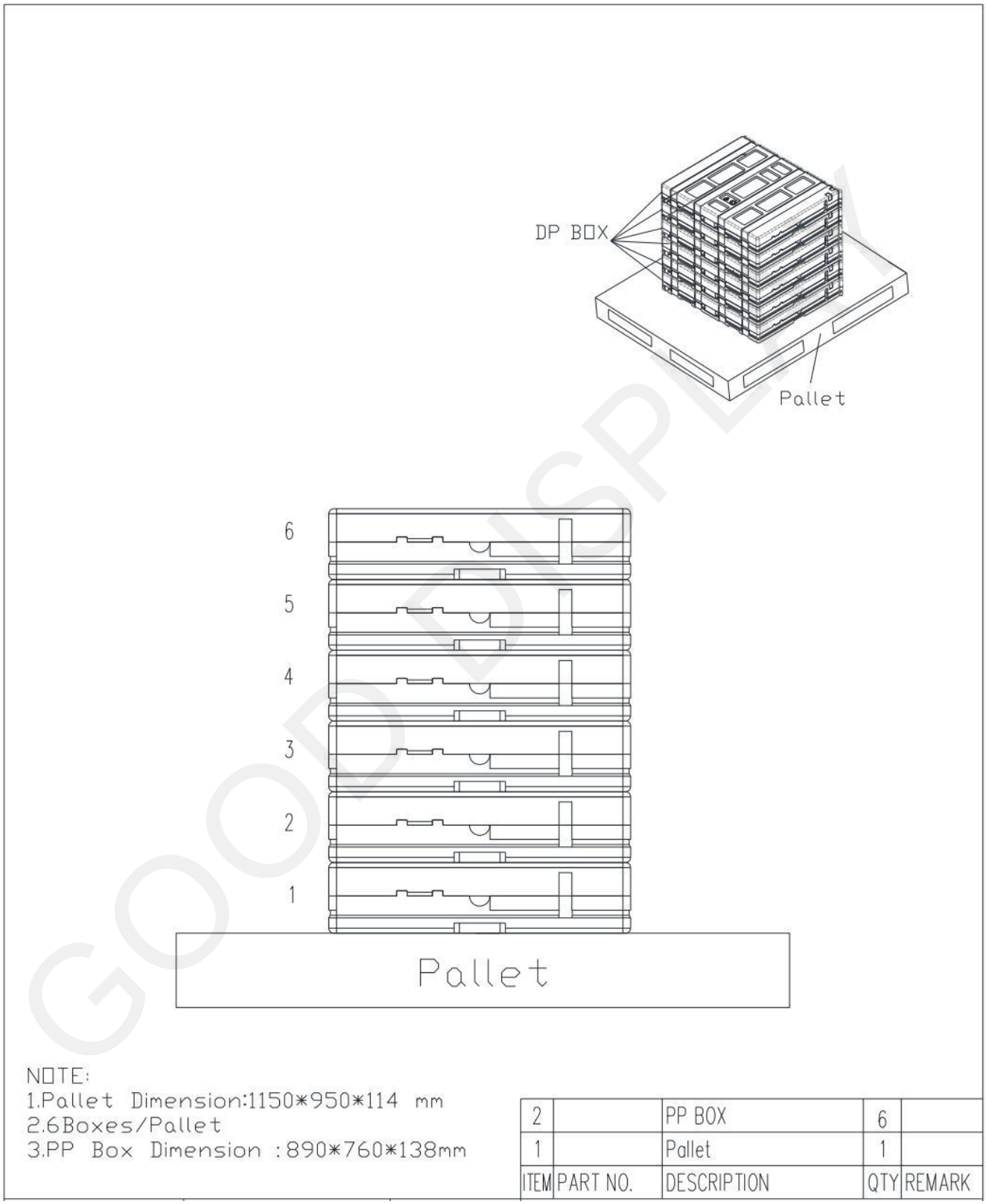


## 12. Packing

### 12.1 packing drawing



Note: Stacking layer limitation: 6 layers.



## 13. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.