



# 7.5 inch E-paper Display Series



**GDEM075Z08**

Dalian Good Display Co., Ltd.

# Product Specifications



<b>Customer</b>	<b>Standard</b>
<b>Description</b>	<b>7.5" E-PAPER DISPLAY</b>
<b>Model Name</b>	<b>GDEM075Z08</b>
<b>Date</b>	<b>2021/02/22</b>
<b>Revision</b>	<b>1.0</b>

	Design Engineering		
	Approval	Check	Design
			

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## Revision History

<b>Version</b>	<b>Content</b>	<b>Date</b>	<b>Producer</b>
1.0	New release	2021/02/22	

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GOOD DISPLAY

## 1. Over View

GDEM075Z08 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white, black and red full display capabilities. The 7.5 inch active area contains 800x480 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

## 2. Features

- ◆ 800x480 pixels display
- ◆ High contrast High reflectance
- ◆ Ultra wide viewing angle Ultra low power consumption
- ◆ Pure reflective mode
- ◆ Bi-stable display
- ◆ Commercial temperature range
- ◆ Landscape portrait modes
- ◆ Hard-coat antiglare display surface
- ◆ Ultra Low current deep sleep mode
- ◆ On chip display RAM
- ◆ Waveform can stored in On-chip OTP or written by MCU
- ◆ Serial peripheral interface available
- ◆ On-chip oscillator
- ◆ On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆ I2C signal master interface to read external temperature sensor
- ◆ Built-in temperature sensor

## 3. Mechanical Specification

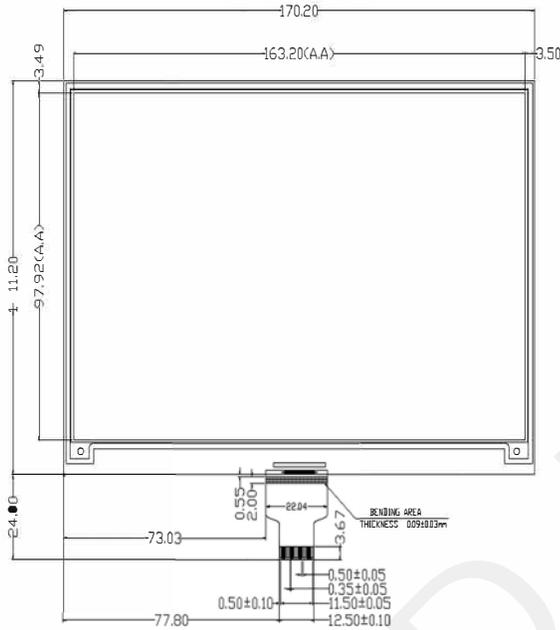
Parameter	Specifications	Unit	Remark
Screen Size	7.5	Inch	
Display Resolution	800(H)×480(V)	Pixel	DPI:124
Active Area	163.2×97.92	mm	
Pixel Pitch	0.204×0.204	mm	
Pixel Configuration	Rectangle		
Outline Dimension	170.2(H)×111.2 (V) ×1.20(D)	mm	
Weight	43.9±0.5	g	

### 4.Mechanical Drawing of EPD Module

**Confirmation:**

DATE	REV.	MODIFICATION
2020-07-09	A	FIRST ISSUE

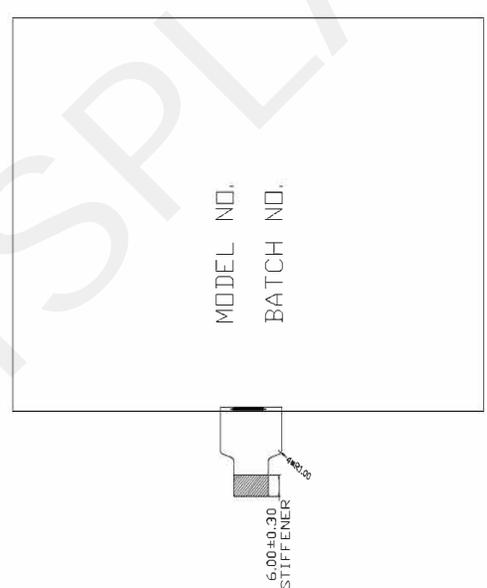
FRONT VIEW



SIDE VIEW



BACK VIEW



PIN	SIGNAL
1	NC
2	GDR
3	RESE
4	NC
5	VSH2
6	TSCL
7	TSDA
8	BS1
9	BUSY
10	RES#
11	D/C#
12	CS#
13	SCL
14	SDA
15	VDDIO
16	VCI
17	VSS
18	VDD
19	VPP
20	VSH1
21	VGH
22	VSL
23	VGL
24	VCDM

**NOTE**

- 1 DISPLAY MODULE 7.5" ARRAY FOR EPD
- 2 DRIVER IC: UC8179C
- 3 RESOLUTION: 800source x 480gate
- 4 PIXEL SIZE: 0.204mmX0.204mm

TOLERANCES UNMARKED	TITLE:	PROJECT:	REV:	DATE:	CUST. P/N
ANGLES±5°	EPD	GDEM075Z08	A	20.07.09	
.X=±0.4mm		DWN.	CHK.	APPR.	
.XX=±0.20mm				UNIT: mm	PAGE: 1/1
.XXX=±0.20mm					

## 5. Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage(Red)	
6	TSCL	O	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I2C Interface to digital temperature sensor Data pin	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	Keep Open
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

**I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/Output),  
P = Power Pin, C = Capacitor Pin**

**Note 5-1:** This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

**Note 5-2:** This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

**Note 5-3:** This pin (RES#) is reset signal input. The Reset is active low.

**Note 5-4:** This pin is Busy state output pin. When Busy is Low, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin Low when -Outputting display waveform -Communicating with digital temperature sensor

**Note 5-5:** Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

## 6. Electrical Characteristics

### 6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.3 to +6.0	V
Logic Input voltage	VIN	-0.3 to VCI +0.5	V
Logic Output voltage	VOUT	-0.3 to VCI +0.5	V
Operating Temp range	TOPR	0 to +40	°C.
Storage Temp range	TSTG	-25 to+40	°C.
Optimal Storage Temp	TSTGo	23±3	°C.
Optimal Storage Humidity	HSTGo	55±10	%RH

**Note:** Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

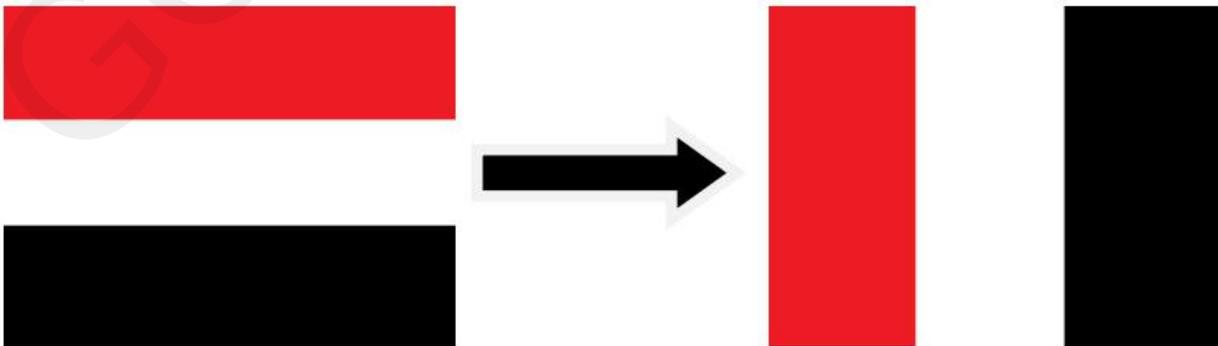
## 6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.3V, TOPR =23°C.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	VSS	-		-	0	-	V
Logic supply voltage	VCI	-	VCI	2.3	3.3	3.6	V
Core logic voltage	VDD		VDD	2.3	3.3	3.6	V
High level input voltage	VIH	-	-	0.7 VCI	-	VCI	V
Low level input voltage	VIL	-	-	0	-	0.3 VCI	V
High level output voltage	VOH	IOH = -100uA	-	VCI-0.4	-	-	V
Low level output voltage	VOL	IOL = 100uA	-	0	-	0.4	
Typical power	PTYP	VCI =3.3V	-	-	26.4	-	mW
Deep sleep mode	PSTPY	VCI =3.3V	-	-	0.003	-	mW
Typical operating current	Iopr_VCI	VCI =3.3V	-	-	10	-	mA
Image update time	-	23 °C	-	-	17	-	sec
Sleep mode current	Islp_VCI	DC/DC off No clock No input load Ram data retain	-	-	20		uA
Deep sleep mode current	Idslp_VCI	DC/DC off No clock No input load Ram data not retain	-	-	1	5	uA

**Notes:**

1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.
2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display.



### 6.3 Panel AC Characteristics

#### 6.3.1 MCU Interface Selection

Provides 3-wire/4-wire serial interface for command and display data transferred from the MCU. The serial interface supports 8-bit mode. Data can be input/output by clocks while the chip is active (CSB =LOW). While input, data are written in order from MSB at the clock rising edge. When too many parameters are input, the chip accepts only defined parameters, and ignores undefined ones.

BS	Interface	CSB	DC	SCL	SDA
High	3-wire SPI	Available	Fix to GND	Available	Available
Low	4-wire SPI	Available	Available	Available	Available

#### 6.3.2 MCU Serial Interface (4-wire SPI)

Data / Command is recognized with DC pin. Data are transferred in the unit of 8 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 8 bits. (The serial counter is reset at the rising edge of the CSB signal.)

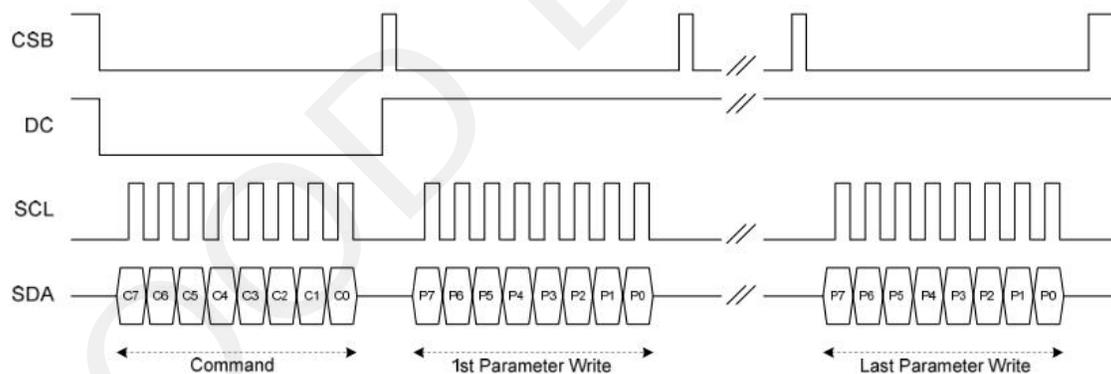


Figure: 4-wire SPI write operation

The MSB bit of data will be output at SDA pin after the CSB falling edge, if DC pin is High.

### 6.3.3 MCU Serial Interface (3-wire SPI)

Data / Command is recognized with the first bit transferred. Data are transferred in the unit of 9 bits. To prevent malfunction due to noise, it is recommended to set the CSB signal to HIGH every 9 bits. (The serial counter is reset at the rising edge of the CSB signal.)

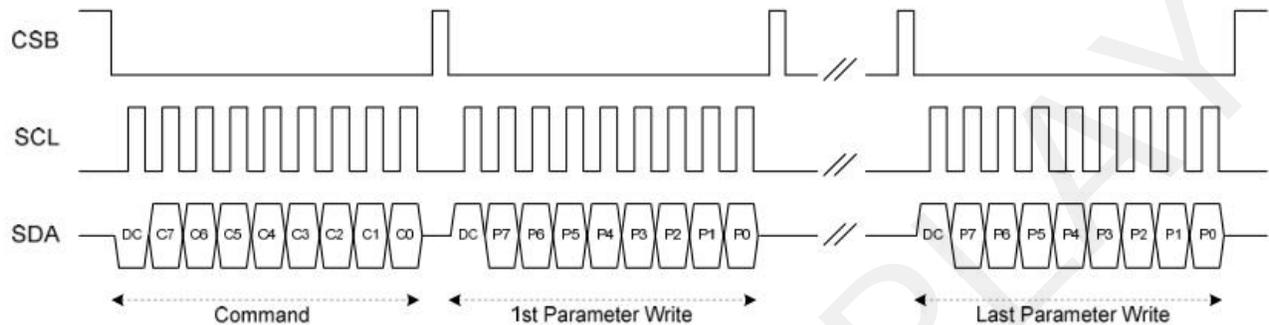


Figure: 3-wire SPI write operation

The MSB bit of data will be output at SDA pin after the 1st SCL falling edge, if the 1st input data at SDA is high.

### 6.3.4 Interface Timing

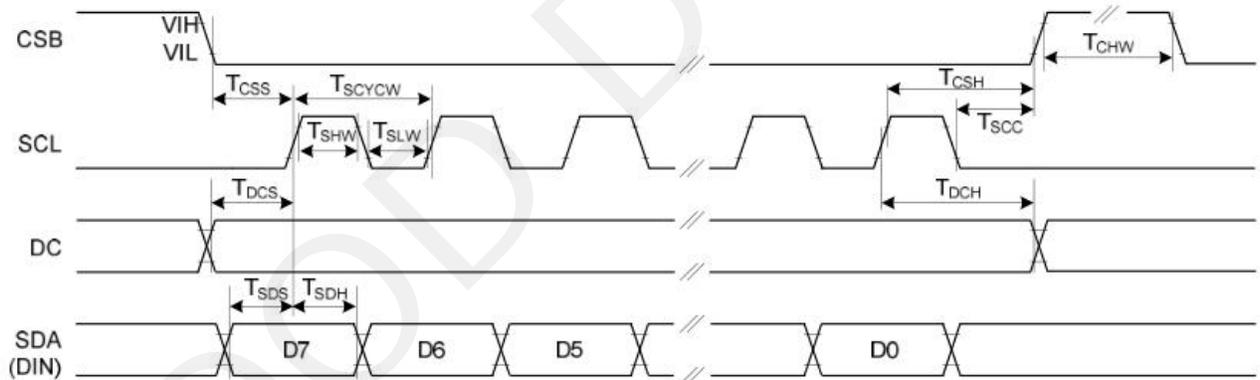
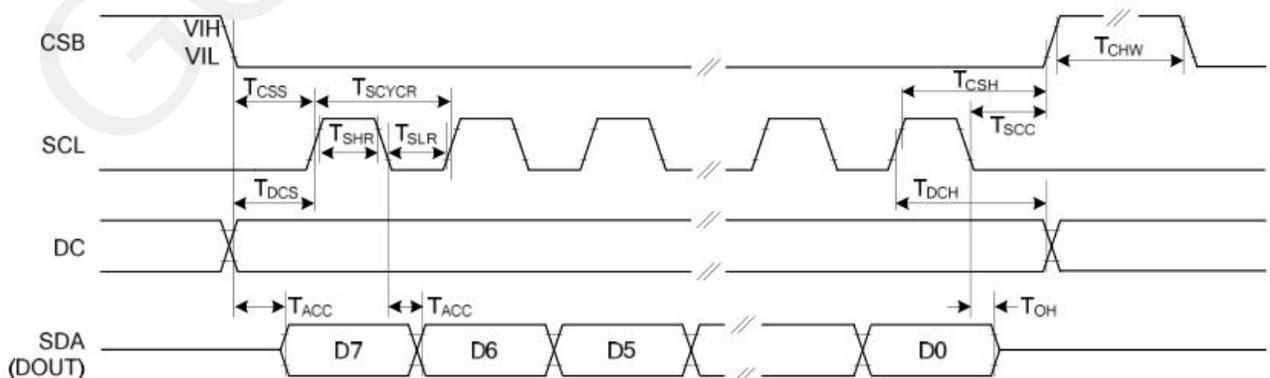


Figure: 4-wire Serial Interface Characteristics (Write mode)



## Serial Interface Timing Characteristics

Symbol	Signal / Parameter	Conditions	Min.	Typ.	Max.	Unit
T <sub>CSS</sub>	CSB	Chip select setup time	60			ns
T <sub>CSH</sub>		Chip select hold time	65			ns
T <sub>SCC</sub>		Chip select setup time	20			ns
T <sub>CHW</sub>		Chip select setup time	40			ns
T <sub>SCYCW</sub>	SCL	Serial clock cycle (Write)	100			ns
T <sub>SHW</sub>		SCL "H" pulse width (Write)	35			ns
T <sub>SLW</sub>		SCL "L" pulse width (Write)	35			ns
T <sub>SCYCR</sub>		Serial clock cycle (Read)	150			ns
T <sub>SHR</sub>		SCL "H" pulse width (Read)	60			ns
T <sub>SLR</sub>		SCL "L" pulse width (Read)	60			ns
T <sub>DCS</sub>	DC	DC setup time	30			ns
T <sub>DCH</sub>		DC hold time	30			ns
T <sub>SDS</sub>	SDA	Data setup time	30			ns
T <sub>SDH</sub>	(DIN)	Data hold time	30			ns
T <sub>ACC</sub>	SDA	Access time			50	ns
T <sub>OH</sub>	(DOUT)	Output disable time	15			ns

## 7.Command Table

W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: : Don't Care

### 1) PANEL SETTING (PSR) (REGISTER: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting the panel	0	0	0	0	0	0	0	0	0	0
	0	1	-	-	REG	KW/R	UD	SHL	SHD_N	RST_N

**REG:** LUT selection

**0: LUT from OTP. (Default)**

1: LUT from register.

**KW/R:** Black / White / Red

**0: Pixel with Black/White/Red, KWR mode. (Default)**

1: Pixel with Black/White, KW mode.

**UD:** Gate Scan Direction

0: Scan down. First line to Last line: Gn-1 Gn-2 Gn-3 ... G0

**1: Scan up. (Default)** First line to Last line: G0 G1 G2 ... .. . Gn-1

**SHL:** Source Shift Direction

0: Shift left. First data to Last data: Sn-1 Sn-2 Sn-3 ... S0

**1: Shift right. (Default)** First data to Last data: S0 S1 S2 ... .. . Sn-1

**SHD\_N:** Booster Switch

0: Booster OFF

**1: Booster ON (Default)**

When SHD\_N becomes LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF. And Source/Gate/Border/VCOM will be released to floating.

**RST\_N:** Soft Reset

0: Reset. Booster OFF, Register data are set to their default values, all drivers will be reset, and all functions will be disabled. Source/Gate/Border/VCOM will be released to floating.

**1: No effect (Default).**

**2) POWER SETTING (PWR) (R01H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1	01H
	0	1	-	-	-	BD_EN	-	VSR_EN	VS_EN	VG_EN	07H
	0	1	-	-	-	VCOM_SLEW	-	VG_LVL[2:0]			17H
	0	1	-	-	VDH_LVL[5:0]						3AH
	0	1	-	-	VDL_LVL[5:0]						3AH
	0	1	-	-	VDHR_LVL[5:0]						03H

**BD\_EN:** Border LDO enable

**0 : Border LDO disable (Default)**

Border level selection: 00b: VCOM 01b: VDHR 10b: VDL 11b: VDHR

**1 : Border LDO enable**

Border level selection: 00b: VCOM 01b: VBH(VCOM-VDL) 10b:VBL(VCOM-VDH) 11b: VDHR

**VSR\_EN:** Source LV power selection

**0 :** External source power from VDHR pins

**1 : Internal DC/DC function for generating VDHR. (Default)**

**VS\_EN:** Source power selection

**0 :** External source power from VDHR/VDL pins

**1 : Internal DC/DC function for generating VDHR/VDL. (Default)**

**VG\_EN:** Gate power selection

**0 :** External gate power from VGH/VGL pins

**1 : Internal DC/DC function for generating VGH/VGL. (Default)**

**VCOM\_SLEW:** VCOM slew rate selection for voltage transition. The value is fixed at 1 .

**VG\_LVL[2:0]:** VGH / VGL Voltage Level selection.

VG_LVL[2:0]	VGH/VGL Voltage Level
000	VGH=9V, VGL= -9V
001	VGH=10V, VGL= -10V
010	VGH=11V, VGL= -11V
011	VGH=12V, VGL= -12V
100	VGH=17V, VGL= -17V
101	VGH=18V, VGL= -18V
110	VGH=19V, VGL= -19V
<b>111 (Default)</b>	<b>VGH=20V, VGL= -20V</b>

**VDH\_LVL[5:0]:** Internal VDH power selection for K/W pixel. (Default value: 111010b)

VDH_LVL	Voltage	VDH_LVL	Voltage	VDH_LVL	Voltage	VDH_LVL	Voltage
000000	2.4 V	010001	5.8 V	100010	9.2 V	110011	12.6 V
000001	2.6 V	010010	6.0 V	100011	9.4 V	110100	12.8 V
000010	2.8 V	010011	6.2 V	100100	9.6 V	110101	13.0 V
000011	3.0 V	010100	6.4 V	100101	9.8 V	110110	13.2 V
000100	3.2 V	010101	6.6 V	100110	10.0 V	110111	13.4 V
000101	3.4 V	010110	6.8 V	100111	10.2 V	111000	13.6 V
000110	3.6 V	010111	7.0 V	101000	10.4 V	111001	13.8 V
000111	3.8 V	011000	7.2 V	101001	10.6 V	<b>111010</b>	<b>14.0 V</b>
001000	4.0 V	011001	7.4 V	101010	10.8 V	111011	14.2 V
001001	4.2 V	011010	7.6 V	101011	11.0 V	111100	14.4 V
001010	4.4 V	011011	7.8 V	101100	11.2 V	111101	14.6 V
001011	4.6 V	011100	8.0 V	101101	11.4 V	111110	14.8 V
001100	4.8 V	011101	8.2 V	101110	11.6 V	111111	15.0 V
001101	5.0 V	011110	8.4 V	101111	11.8 V		
001110	5.2 V	011111	8.6 V	110000	12.0 V		
001111	5.4 V	100000	8.8 V	110001	12.2 V		
010000	5.6 V	100001	9.0 V	110010	12.4 V		

**VDL\_LVL[5:0]:** Internal VDL power selection for K/W pixel. (Default value: 111010b)

VDL_LVL	Voltage	VDL_LVL	Voltage	VDL_LVL	Voltage	VDL_LVL	Voltage
000000	-2.4 V	010001	-5.8 V	100010	-9.2 V	110011	-12.6 V
000001	-2.6 V	010010	-6.0 V	100011	-9.4 V	110100	-12.8 V
000010	-2.8 V	010011	-6.2 V	100100	-9.6 V	110101	-13.0 V
000011	-3.0 V	010100	-6.4 V	100101	-9.8 V	110110	-13.2 V
000100	-3.2 V	010101	-6.6 V	100110	-10.0 V	110111	-13.4 V
000101	-3.4 V	010110	-6.8 V	100111	-10.2 V	111000	-13.6 V
000110	-3.6 V	010111	-7.0 V	101000	-10.4 V	111001	-13.8 V
000111	-3.8 V	011000	-7.2 V	101001	-10.6 V	<b>111010</b>	<b>-14.0 V</b>
001000	-4.0 V	011001	-7.4 V	101010	-10.8 V	111011	-14.2 V
001001	-4.2 V	011010	-7.6 V	101011	-11.0 V	111100	-14.4 V
001010	-4.4 V	011011	-7.8 V	101100	-11.2 V	111101	-14.6 V
001011	-4.6 V	011100	-8.0 V	101101	-11.4 V	111110	-14.8 V
001100	-4.8 V	011101	-8.2 V	101110	-11.6 V	111111	-15.0 V
001101	-5.0 V	011110	-8.4 V	101111	-11.8 V		
001110	-5.2 V	011111	-8.6 V	110000	-12.0 V		
001111	-5.4 V	100000	-8.8 V	110001	-12.2 V		
010000	-5.6 V	100001	-9.0 V	110010	-12.4 V		

**VDHR\_LVL[5:0]:** Internal VDHR power selection for Red pixel. (Default value: 000011b)

VDHR_LVL	Voltage	VDHR_LVL	Voltage	VDHR_LVL	Voltage	VDHR_LVL	Voltage
000000	2.4 V	010001	5.8 V	100010	9.2 V	110011	12.6 V
000001	2.6 V	010010	6.0 V	100011	9.4 V	110100	12.8 V
000010	2.8 V	010011	6.2 V	100100	9.6 V	110101	13.0 V
<b>000011</b>	<b>3.0 V</b>	010100	6.4 V	100101	9.8 V	110110	13.2 V
000100	3.2 V	010101	6.6 V	100110	10.0 V	110111	13.4 V
000101	3.4 V	010110	6.8 V	100111	10.2 V	111000	13.6 V
000110	3.6 V	010111	7.0 V	101000	10.4 V	111001	13.8 V
000111	3.8 V	011000	7.2 V	101001	10.6 V	111010	14.0 V
001000	4.0 V	011001	7.4 V	101010	10.8 V	111011	14.2 V
001001	4.2 V	011010	7.6 V	101011	11.0 V	111100	14.4 V
001010	4.4 V	011011	7.8 V	101100	11.2 V	111101	14.6 V
001011	4.6 V	011100	8.0 V	101101	11.4 V	111110	14.8 V
001100	4.8 V	011101	8.2 V	101110	11.6 V	111111	15.0 V
001101	5.0 V	011110	8.4 V	101111	11.8 V		
001110	5.2 V	011111	8.6 V	110000	12.0 V		
001111	5.4 V	100000	8.8 V	110001	12.2 V		
010000	5.6 V	100001	9.0 V	110010	12.4 V		

### 3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	0	0	0	0	0	0	0	0	1	0

After the Power OFF command, the driver will be powered OFF. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode.

Source/Gate/Border/VCOM will be released to floating.

### 4) POWER OFF SEQUENCE SETTING (PFS) (R03 H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1
	0	1	-	-	T_VDS_OFF[1:0]	-	-	-	-	-

**T\_VDS\_OFF[1:0]:** Source to gate power off interval time.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

### 5) POWER ON (PON) (REGISTER: R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the power	0	0	0	0	0	0	0	1	0	0

After the Power ON command, the driver will be powered ON. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUS\_N signal will return to high.

### 6) BOOSTER SOFT START (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Booster Software Start Set	0	0	0	0	0	0	0	1	1	0
	0	1	BT_PHA[7:6]		BT_PHA[5:3]			BT_PHA[2:0]		
	0	1	BT_PHB[7:6]		BT_PHB[5:3]			BT_PHB[2:0]		
	0	1	-	-	BT_PHC1[5:3]			BT_PHC1[2:0]		
	0	1	PHC2EN	-	BT_PHC2[5:3]			BT_PHC2[2:0]		

**BT PHA 7:6** : Soft start period of phase A.

00b: 10mS    01b: 20mS    10b: 30mS    11b: 40mS

**BT PHA 5:3** : Driving strength of phase A

000b: strength 1    001b: strength 2    010b: strength 3    011b: strength 4

100b: strength 5    101b: strength 6    110b: strength 7    111b: strength 8 (strongest)

**BT PHA 2:0** : Minimum OFF time setting of GDR in phase A

000b: 0.27uS    001b: 0.34uS    010b: 0.40uS    011b: 0.54uS

100b: 0.80uS    101b: 1.54uS    110b: 3.34uS    111b: 6.58uS

**BT PHB 7:6** : Soft start period of phase B.

00b: 10mS    01b: 20mS    10b: 30mS    11b: 40mS

**BT PHB 5:3** : Driving strength of phase B

000b: strength 1    001b: strength 2    010b: strength 3    011b: strength 4

100b: strength 5    101b: strength 6    110b: strength 7    111b: strength 8 (strongest)

**BT PHB 2:0** : Minimum OFF time setting of GDR in phase B

000b: 0.27uS    001b: 0.34uS    010b: 0.40uS    011b: 0.54uS

100b: 0.80uS    101b: 1.54uS    110b: 3.34uS    111b: 6.58uS

**BT PHC1 5:3** : Driving strength of phase C1

000b: strength 1    001b: strength 2    010b: strength 3    011b: strength 4

100b: strength 5    101b: strength 6    110b: strength 7    111b: strength 8 (strongest)

**BT PHC1 2:0** : Minimum OFF time setting of GDR in phase C1

000b: 0.27uS    001b: 0.34uS    010b: 0.40uS    011b: 0.54uS

100b: 0.80uS    101b: 1.54uS    110b: 3.34uS    111b: 6.58uS

**PHC2EN:** Booster phase-C2 enable

0: Booster phase-C2 disable

Phase-C1 setting always is applied for booster phase-C.

1: Booster phase-C2 enable

If temperature < temperature boundary phase-C2(RE7h 7:0 ), phase-C1 setting is applied for booster phase-C.

If temperature = temperature boundary phase-C2(RE7h 7:0 ), phase-C2 setting is applied for booster phase-C.

**BT PHC2 5:3** : Driving strength of phase C2

000b: strength 1    001b: strength 2    010b: strength 3    011b: strength 4

100b: strength 5    101b: strength 6    110b: strength 7    111b: strength 8 (strongest)

**BT PHC2 2:0** : Minimum OFF time setting of GDR in phase C2

000b: 0.27uS    001b: 0.34uS    010b: 0.40uS    011b: 0.54uS

100b: 0.80uS    101b: 1.54uS    110b: 3.34uS    111b:6.58uS

**7) DEEP SLEEP (DSLPL) (R07H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep Sleep	0	0	0	0	0	0	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

**8) DATA START TRANSMISSION 1 (DTM1) (R10H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	0	0
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	:	:	:	:	:	:	:	:
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes OLD data to SRAM.

In KWR mode, this command writes K/W data to SRAM.

In Program mode, this command writes OTP data to SRAM for programming.

**9) DISPLA REFRESH (DRF) (R12H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Refreshing the display	0	0	0	0	0	1	0	0	1	0

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUS N signal will become 0 and the refreshing of panel starts.

**10) DATA START TRANSMISSION 2 (DTM2) (R13 H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	1	1
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	:	:	:	:	:	:	:	:
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

This command starts transmitting data and write them into SRAM.

In KW mode, this command writes NEW data to SRAM.

In KWR mode, this command writes RED data to SRAM.

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-up Table for VCOM (61-byte command, structure of bytes 2~7 repeated 10 times)	0	0	0	0	1	0	0	0	0	0
	0	1	LEVEL SELECT-0		LEVEL SELECT-1		LEVEL SELECT-2		LEVEL SELECT-3	
	0	1	NUMBER OF FRAMES-0							
	0	1	NUMBER OF FRAMES-1							
	0	1	NUMBER OF FRAMES-2							
	0	1	NUMBER OF FRAMES-3							
	0	1	TIMES TO REPEAT							

This command stores VCOM Look-Up Table with 10 groups of data. Each group contains information for one state and is stored with 6 bytes (byte 2 7, 8 13, 14 19, 20 25, ...), while the sixth byte indicates how many times that phase will repeat.

**Bytes 2, 8, 14, 20, 26, 32, 38, 44, 50, 56:**

- D 7:6 , D 5:4 , D 3:2 , D 1:0 : Level Selection
- 00b: VCOM DC
- 01b: VDH+VCOM DC (VCOMH)
- 10b: VDL+VCOM DC (VCOML)
- 11b: Floating

**Bytes 3 6, 9 12, 15 18, 21 24, 27 30, 33 36, 39 42, 45 48, 51 54, 57 60:**

- Number of Frames
- 0000 0000b: 0 frame
- : :
- : :
- 1111 1111b: 255 frames

**Bytes 7, 13, 19, 25, 31, 37, 43, 49, 55, 61:**

- Times to Repeat
- 0000 0000b: 0 time
- : :
- : :
- 1111 1111b: 255 times

If KW/R=0 (KWR mode), all 10 groups are used.  
 If KW/R=1 (KW mode), only 7 groups are used.

**12) W2W LUT (LUTWW) (R21H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	1	0	0	0	0	1
Build White Look-up Table for W2W (43-byte command, structure of bytes 2~7 repeated 7 times)	0	1	LEVEL SELECT-0	LEVEL SELECT-1	LEVEL SELECT-2	LEVEL SELECT-3				
	0	1					NUMBER OF FRAMES-0			
	0	1					NUMBER OF FRAMES-1			
	0	1					NUMBER OF FRAMES-2			
	0	1					NUMBER OF FRAMES-3			
	0	1					TIMES TO REPEAT			
	0	1								

This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes (byte 2 7, 8 13, 14 19, 20 25, ...), while the sixth byte indicates how many times that phase will repeat.

**Bytes 2, 8, 14, 20, 26, 32, 38:**

Level Selection.

00b: GND

01b: VDH

10b: VDL

11b: VDHR

**Bytes 3 6, 9 12, 15 18, 21 24, 27 30, 33 36, 39 42:**

Number of Frames

0000 0000b: 0 frame

: :

: :

1111 1111b: 255 frames

**Bytes 7, 13, 19, 25, 31, 37, 43:**

Times to Repeat

0000 0000b: 0 time

: :

: :

1111 1111b: 255 times

If KW/R=0 (KWR mode), LUTWW is not used.

If KW/R=1 (KW mode), LUTWW is used.

### 13) K2W LUT (LUTKW / LUTR) (R22H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0		
	0	0	0	0	1	0	0	0	1	0	22H	
Build	0	1	LEVEL SELECT-0	LEVEL SELECT-1	LEVEL SELECT-2	LEVEL SELECT-3						--
Look-up Table for K2W or Red	0	1	NUMBER OF FRAMES-0									--
(61-byte command,	0	1	NUMBER OF FRAMES-1									--
structure of bytes 2~7	0	1	NUMBER OF FRAMES-2									--
repeated 10 times)	0	1	NUMBER OF FRAMES-3									--
	0	1	TIMES TO REPEAT									--

This command stores White-to-White Look-Up Table with 10 groups of data. Each group contains information for one state and is stored with 6 bytes (byte 2 7, 8 13, 14 19, 20 25, ...), while the sixth byte indicates how many times that phase will repeat.

#### **Bytes 2, 8, 14, 20, 26, 32, 38, 44, 50, 56:**

Level Selection.

00b: GND

01b: VDH

10b: VDL

11b: VDHR

#### **Bytes 3 6, 9 12, 15 18, 21 24, 27 30, 33 36, 39 42, 45 48, 51 54, 57 60:**

Number of Frames

0000 0000b: 0 frame

: :

: :

1111 1111b: 255 frames

#### **Bytes 7, 13, 19, 25, 31, 37, 43, 49, 55, 61:**

Times to Repeat

0000 0000b: 0 time

: :

: :

1111 1111b: 255 times

If KW/R=0 (KWR mode), all 10 groups are used.

If KW/R=1 (KW mode), only 7 groups are used.

**14) W2K LUT (LUTWK / LUTW) (R23H)**

This command builds Look-up Table for White-to-Black. Please refer to K2W LUT (LUTKW/LUTR) for similar definition details.

Regardless of KW/R=0 or KW/R=1, LUTWK/LUTW is used.

**15) K2K LUT (LUTKK / LUTK) (R24H)**

This command builds Look-up Table for Black-to-Black. Please refer to K2W LUT (LUTKW/LUTR) for similar definition details.

Regardless of KW/R=0 or KW/R=1, LUTKK/LUTK is used.

**16) BORDER LUT (LUTBD) (R25 H )**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Build Look-up Table for Border (43-byte command, Bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	1	0	1
	0	1	LEVEL SELECT-0		LEVEL SELECT-1		LEVEL SELECT-2		LEVEL SELECT-3	
	0	1	NUMBER OF FRAMES-0							
	0	1	NUMBER OF FRAMES-1							
	0	1	NUMBER OF FRAMES-2							
	0	1	NUMBER OF FRAMES-3							
	0	1	TIMES TO REPEAT							

This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes (byte 2 7, 8 13, 14 19, 20 25, ...), while the sixth byte indicates how many times that phase will repeat.

**Bytes 2, 8, 14, 20, 26, 32, 38:**

Level selection.

BD EN=0: 00b: VCOM 01b: VDH 10b: VDL 11b: VDHR

BD EN=1: 00b: VCOM 01b: VBH(VCOM-VDL) 10b: VBL(VCOM-VDH) 11b: VDHR

Bytes 3 6, 9 12, 15 18, 21 24, 27 30, 33 36, 39 42:

Number of Frames

0000 0000b: 0 frame

: :

: :

1111 1111b: 255 frames

**Bytes 7, 13, 19, 25, 31, 37, 43:**

Times to Repeat

0000 0000b: 0 time

: :

: :

1111 1111b: 255 times

Only 7 LUTBD groups are used in KW mode or KWR mode.

### 17) LUT OPTION (LUTOPT) (R2A H )

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0		
LUT Option	0	0	0	0	1	0	1	0	1	0	2AH	
	0	1	STATE_XON[9:8]			-	-	-	-	-	-	00H
	0	1	STATE_XON[7:0]								00H	

This command sets XON control enable.

#### STATE\_XON 9:0 :

All Gate ON (Each bit controls one state, STATE\_XON 0 for state-1, STATE\_XON 1 for state-2 .....

00 0000 0000b: no All-Gate-ON

00 0000 0001b: State-1 All-Gate-ON

00 0000 0011b: State-1 and State2 All-Gate-ON

: :

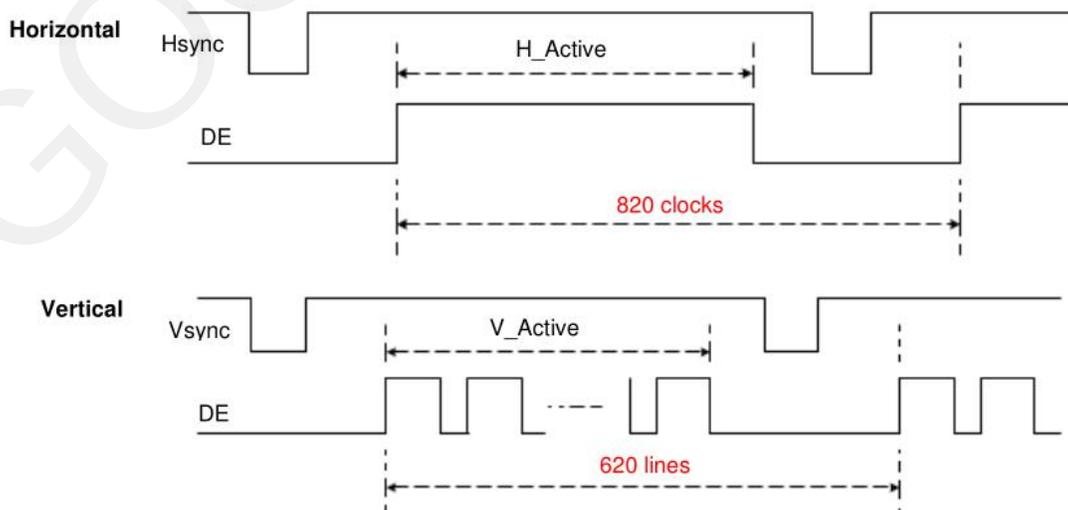
### 18) PLL CONTROL(PLL) (R30 H )

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Controlling PLL	0	0	0	0	1	1	0	0	0	0	30H
	0	1	-	-	-	-	FRS[3:0]				06H

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

FMR[3:0]: Frame rate setting

FRS	Frame rate	FRS	Frame rate
0000	5Hz	1000	70Hz
0001	10Hz	1001	80Hz
0010	15Hz	1010	90Hz
0011	20Hz	1011	100Hz
0100	30Hz	1100	110Hz
0101	40Hz	1101	130Hz
<b>0110</b>	<b>50Hz</b>	1110	150Hz
0111	60Hz	1111	200Hz



### 19) TEMPERATURE SENSOR CALIBRATION (TSC) (R40 H )

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	0	0	0	0	0	0
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0
	1	1	D2	D1	D0	-	-	-	-	-

This command enables internal or external temperature sensor, and reads the result.

**TS[7:0]:** When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

**D[10:0]:** When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temp. (°C)	TS[7:0]/D[10:3]	Temp. (°C)	TS[7:0]/D[10:3]	Temp. (°C)
1110_0111	-25	0000_0000	0	0001_1001	25
1110_1000	-24	0000_0001	1	0001_1010	26
1110_1001	-23	0000_0010	2	0001_1011	27
1110_1010	-22	0000_0011	3	0001_1100	28
1110_1011	-21	0000_0100	4	0001_1101	29
1110_1100	-20	0000_0101	5	0001_1110	30
1110_1101	-19	0000_0110	6	0001_1111	31
1110_1110	-18	0000_0111	7	0010_0000	32
1110_1111	-17	0000_1000	8	0010_0001	33
1111_0000	-16	0000_1001	9	0010_0010	34
1111_0001	-15	0000_1010	10	0010_0011	35
1111_0010	-14	0000_1011	11	0010_0100	36
1111_0011	-13	0000_1100	12	0010_0101	37
1111_0100	-12	0000_1101	13	0010_0110	38
1111_0101	-11	0000_1110	14	0010_0111	39
1111_0110	-10	0000_1111	15	0010_1000	40
1111_0111	-9	0001_0000	16	0010_1001	41
1111_1000	-8	0001_0001	17	0010_1010	42
1111_1001	-7	0001_0010	18	0010_1011	43
1111_1010	-6	0001_0011	19	0010_1100	44
1111_1011	-5	0001_0100	20	0010_1101	45
1111_1100	-4	0001_0101	21	0010_1110	46
1111_1101	-3	0001_0110	22	0010_1111	47
1111_1110	-2	0001_0111	23	0011_0000	48
1111_1111	-1	0001_1000	24	0011_0001	49

### 20) VCOM AND DATA INTERVAL SETTING (CDI) (R50 H )

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval between VCOM and Data	0	0	0	1	0	1	0	0	0	0
	0	1	BDZ	-	BDV[1:0]	N2OCP	-	-	DDX[1:0]	-
	0	1	-	-	-	-	-	-	CDI[3:0]	-

This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

**BDZ:** Border Hi-Z control

**0:** Border output Hi-Z disabled (default)

**1:** Border output Hi-Z enabled

**BDV 1:0 :** Border LUT selection

KWR mode (KW/R=0)

DDX[0]	BDV[1:0]	LUT
0	00	LUTBD
	01	LUTR
	10	LUTW
	11	LUTK
1 (Default)	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTBD

KW mode (KW/R=1)

DDX[0]	BDV[1:0]	LUT
0	00	LUTBD
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (0 → 0)
<b>1 (Default)</b>	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTBD

**N2OCP:** Copy frame data from NEW data to OLD data enable control after display refresh with NEW/OLD in KW mode.

0: Copy NEW data to OLD data disabled (default)

1: Copy NEW data to OLD data enabled

**DDX 1:0 :** Data polarity.

Under KWR mode (KW/R=0):

DDX 1 is for RED data.

DDX 0 is for K/W data,

DDX[1:0]	Data {Red, K/W}	LUT
00	00	LUTW
	01	LUTK
	10	LUTR
	11	LUTR
<b>01 (Default)</b>	00	LUTK
	01	LUTW
	10	LUTR
	11	LUTR

DDX[1:0]	Data {Red, K/W}	LUT
10	00	LUTR
	01	LUTR
	10	LUTW
	11	LUTK
11	00	LUTR
	01	LUTR
	10	LUTK
	11	LUTW

Under KW mode (KW/R=1):

DDX 1 =0 is for KW mode with NEW/OLD,

DDX 1 =1 is for KW mode without NEW/OLD.

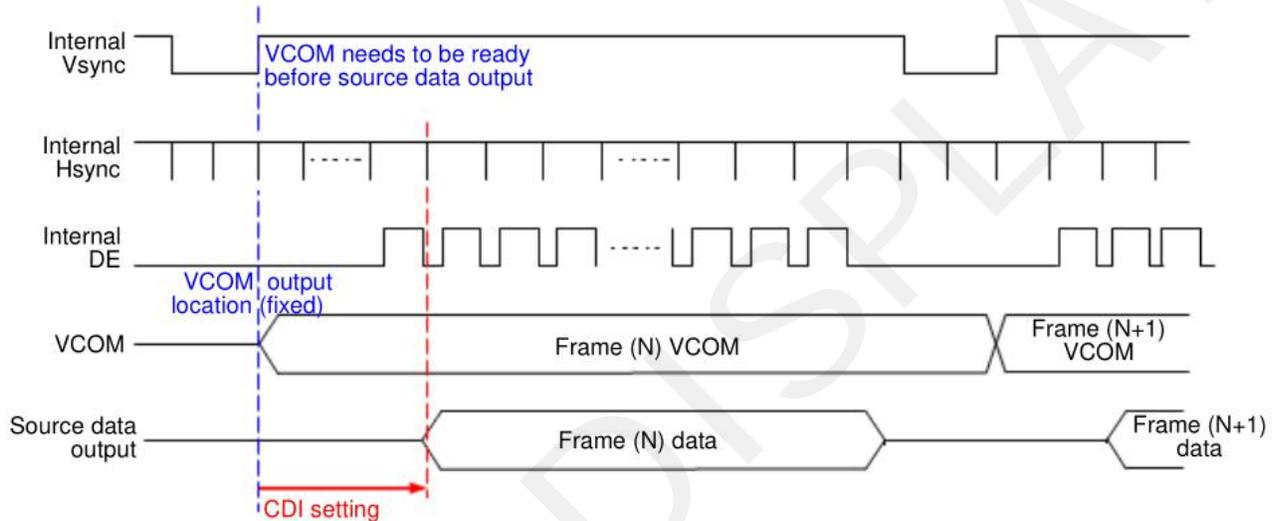
DDX[1:0]	Data {NEW, OLD}	LUT
00	00	LUTWW (0 → 0)
	01	LUTKW (1 → 0)
	10	LUTWK (0 → 1)
	11	LUTKK (1 → 1)
<b>01 (Default)</b>	00	LUTKK (0 → 0)
	01	LUTWK (1 → 0)
	10	LUTKW (0 → 1)
	11	LUTWW (1 → 1)

DDX[1:0]	Data {NEW}	LUT
10	0	LUTKW (1 → 0)
	1	LUTWK (0 → 1)
11	0	LUTWK (1 → 0)
	1	LUTKW (0 → 1)

**CDI 3:0** : VCOM and data interval

CDI[3:0]	VCOM and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
<b>0111</b>	<b>10 (Default)</b>

CDI[3:0]	VCOM and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



**21) TCON SETTING (TCON) (R60 H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Gate/Source Non-overlap Period	0	0	0	1	1	0	0	0	0	0
	0	1	S2G[3:0]				G2S[3:0]			

60h 22h

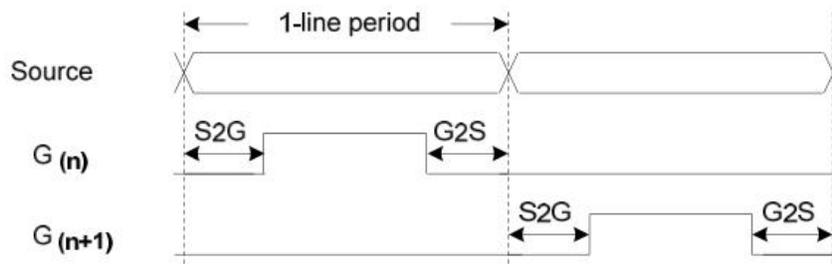
This command defines non-overlap period of Gate and Source.

**S2G[3:0] or G2S[3:0]:** Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000 b	4
0001	8
<b>0010</b>	<b>12 (Default)</b>
0011	16
0100	20
0101	24
0110	28
0111	32

S2G[3:0] or G2S[3:0]	Period
1000 b	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	60
1111	64

Period Unit = 667 nS.



## 22) RESOLUTION SETTING (TRES) (R61 H )

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	0	1	1	0	0	0	0	1	61h
	0	1	-	-	-	-	-	-	HRES[9:8]		03h
	0	1	HRES[7:3]					0	0	0	20h
	0	1	-	-	-	-	-	-	VRES[9:8]		02h
	0	1	VRES[7:0]								58h

This command defines resolution setting.

**HRES 9:3** : Horizontal Display Resolution (Value range: 01h 64h)

**VRES 9:0** : Vertical Display Resolution (Value range: 001h 258h)

Active channel calculation, assuming HST 9:0 =0, VST 9:0 =0:

Gate: First active gate = G0;

Last active gate = VRES 9:0 1

Source: First active source = S0;

Last active source = HRES 9:3 8 1

Example: 128 (source) x 272 (gate), assuming HST 9:0 =0, VST 9:0 =0

Gate: First active gate = G0,

Last active gate = G271; (VRES 9:0 = 272, 272 1= 271)

Source: First active source = S0,

Last active source = S127; (HRES 9:3 =16, 16 8 1 = 127)

## 23) GATE /SOURCE START SETTING (GSST) (R65 H )

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Gate/Source Start	0	0	0	1	1	0	0	1	0	1	65h
	0	1	-	-	-	-	-	-	HST[9:8]		00h
	0	1	HST[7:3]					0	0	0	00h
	0	1	-	-	-	-	-	-	VST[9:8]		00h
	0	1	VST[7:0]								00h

This command defines resolution start gate/source position.

**HST 9:3** : Horizontal Display Start Position (Source). (Value range: 00h 63h)

**VST 9:0** : Vertical Display Start Position (Gate). (Value range: 000h 257h)

Example : For 128(Source) x 240(Gate)

HST 9:3 = 4 (HST 9:0 = 4 8 = 32),

VST 9:0 = 32

Gate: First active gate = G32 (VST 9:0 = 32),

Last active gate = G271 (VRES 9:0 = 240, VST 9:0 = 32, 240-1+32=271)

Source: First active source = S32 (HST 9:0 = 32),

Last active source = S239 (HRES 9:0 = 128, HST 9:0 = 32, 128-1+32=239)

## 24) REVISION (REV) (R70 H )

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0		
LUT/Chip Revision	0	0	0	1	1	1	0	0	0	0	70h	
	1	1	PROD_REV[23:16]									FFh
	1	1	PROD_REV[15:8]									FFh
	1	1	PROD_REV[7:0]									FFh
	1	1	LUT_REV[23:16]									FFh
	1	1	LUT_REV[15:8]									FFh
	1	1	LUT_REV[7:0]									FFh
	1	1	CHIP_REV[7:0]									0Ch

The command reads the product revision, LUT revision and chip revision.

**PROD REV 23:0** : Product Revision. PROD\_REV 23:0 is read from OTP address 0x0BDD 0X0BDF or 0x17DD 0x17DF.

**LUT REV 23:0** : LUT Revision. LUT\_REV 23:0 is read from OTP address 0x0BE0 0X0BE2 or 0x17E0. 0x17E2.

**CHIP REV 7:0** : Chip Revision, fixed at 00001100b.

## 25) VCOM DC SETTING (VDCS) (R82 H )

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set VCOM_DC	0	0	1	0	0	0	0	0	1	0	82h
	0	1	-	VDCS[6:0]							

This command sets VCOM\_DC value

**VDCS[6:0]: VCOM\_DC Setting**

VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)	VDCS [6:0]	VCOM Voltage (V)
000 0000b	-0.10	001 1011b	-1.45	011 0110b	-2.80
000 0001b	-0.15	001 1100b	-1.50	011 0111b	-2.85
000 0010b	-0.20	001 1101b	-1.55	011 1000b	-2.90
000 0011b	-0.25	001 1110b	-1.60	011 1001b	-2.95
000 0100b	-0.30	001 1111b	-1.65	011 1010b	-3.00
000 0101b	-0.35	010 0000b	-1.70	011 1011b	-3.05
000 0110b	-0.40	010 0001b	-1.75	011 1100b	-3.10
000 0111b	-0.45	010 0010b	-1.80	011 1101b	-3.15
000 1000b	-0.50	010 0011b	-1.85	011 1110b	-3.20
000 1001b	-0.55	010 0100b	-1.90	011 1111b	-3.25
000 1010b	-0.60	010 0101b	-1.95	100 0000b	-3.30
000 1011b	-0.65	010 0110b	-2.00	100 0001b	-3.35
000 1100b	-0.70	010 0111b	-2.05	100 0010b	-3.40
000 1101b	-0.75	010 1000b	-2.10	100 0011b	-3.45
000 1110b	-0.80	010 1001b	-2.15	100 0100b	-3.50
000 1111b	-0.85	010 1010b	-2.20	100 0101b	-3.55
001 0000b	-0.90	010 1011b	-2.25	100 0110b	-3.60
001 0001b	-0.95	010 1100b	-2.30	100 0111b	-3.65
001 0010b	-1.00	010 1101b	-2.35	100 1000b	-3.70
001 0011b	-1.05	010 1110b	-2.40	100 1001b	-3.75
001 0100b	-1.10	010 1111b	-2.45	100 1010b	-3.80
001 0101b	-1.15	011 0000b	-2.50	100 1011b	-3.85
001 0110b	-1.20	011 0001b	-2.55	100 1100b	-3.90
001 0111b	-1.25	011 0010b	-2.60	100 1101b	-3.95
001 1000b	-1.30	011 0011b	-2.65	100 1110b	-4.00
001 1001b	-1.35	011 0100b	-2.70	100 1111b	-4.05
001 1010b	-1.40	011 0101b	-2.75		

**26) PROGRAM MODE (PGM) (RA0 H )**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enter Program Mode	0	0	1	0	1	0	0	0	0	0

A0h

After this command is issued, the chip would enter the program mode.

After the programming procedure completed, a hardware reset is necessary for leaving program mode.

**27) ACTIVE PROGRAM (APG) (RA1 H )**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Active Program OTP	0	0	1	0	1	0	0	0	0	1

A1h

After this command is transmitted, the programming state machine would be activated.

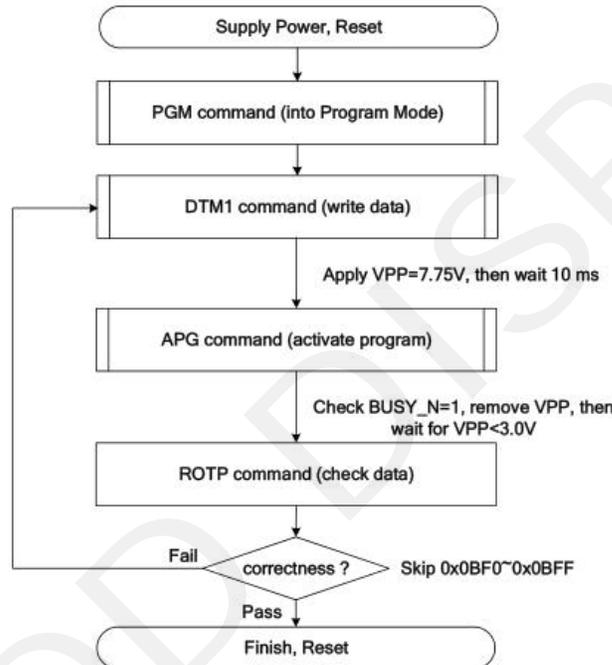
The BUS N flag would fall to 0 until the programming is completed.

**28) READ OTP DATA (ROTP) (RA2 H )**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read OTP data for check	0	0	1	0	1	0	0	0	1	0
	1	1	The data of address 0x000 in the OTP							
	1	1	The data of address 0x001 in the OTP							
	1	1	:							
	1	1	The data of address (n-1) in the OTP							
	1	1	The data of address (n) in the OTP							

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0x17FF.



The sequence of programming OTP.

## 8. Optical Specification

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	34	-	%	8-1
CR	Contrast Ratio	Indoor	15:1	20	-		8-1 8-2
GN	2Grey Level	-	-	-	-		
KS	Black State L* value		-	13	15		8-1
	Black State A* value		-	3	5		8-1
WS	White State L* value		62	65	-		8-1
	White State A* value		-	0	1		8-1
RS	Red State L* value		26	28	-		8-1
	Red State A* value		36	42	-		8-1
T update	Image update time	at 23 °C	-	15	-	sec	
Life		Temp:23 ± 3°C Humidity:55 ± 10%RH		5years			8-3

### Notes:

- 8-1. Luminance meter: Eye-One Pro Spectrophotometer.
- 8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.
- 8-3. When the product is stored. The display screen should be kept white and face up.

## 9. Handling, Safety, and Environment Requirements

### Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

### Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module. Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

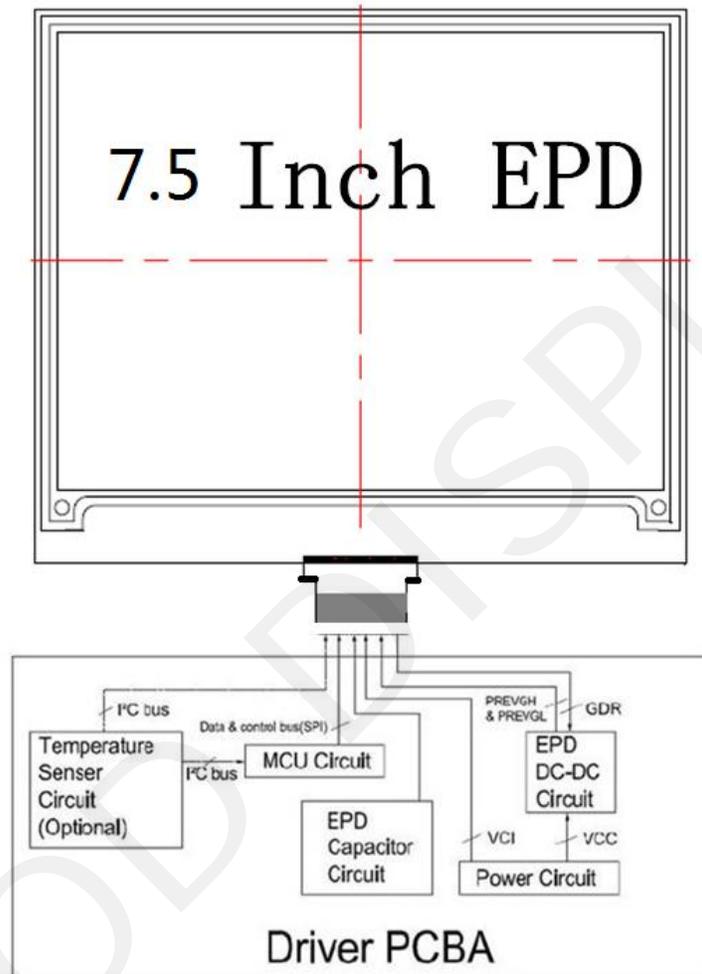
<b>Data sheet status</b>	
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

## 10. Reliability Test

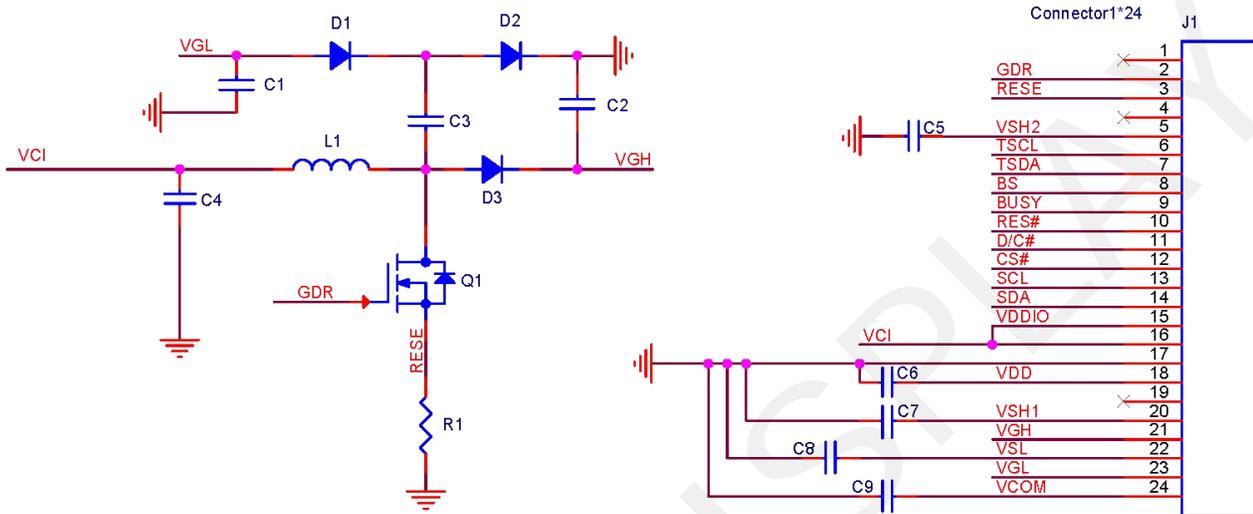
NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=60°C, RH=40%, 240h Test in white pattern
3	High-Temperature Operation	T=40°C, RH=35%, 240h
4	Low-Temperature Operation	0°C, 240h
5	High-Temperature, High-Humidity Operation	T=40°C, RH=80%, 240h
6	High Temperature, High Humidity Storage	T=50°C, RH=80%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min]→[+60 °C 30 min] : 50 cycles Test in white pattern
8	UV exposure Resistance	765W/m <sup>2</sup> for 168hrs,40 °C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell, not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display, no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display, including IC and FPC area)

**Note: Put in normal temperature for 1hour after test finished, display performance is ok.**

### 11. Block Diagram



## 12. Typical Application Circuit with SPI Interface



### 13. Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display and three-color (black, white and red/Yellow) Good Display `s E-paper Display. And it is also added the functions of USB serial port, Raspberry Pi and LED indicator light ect.

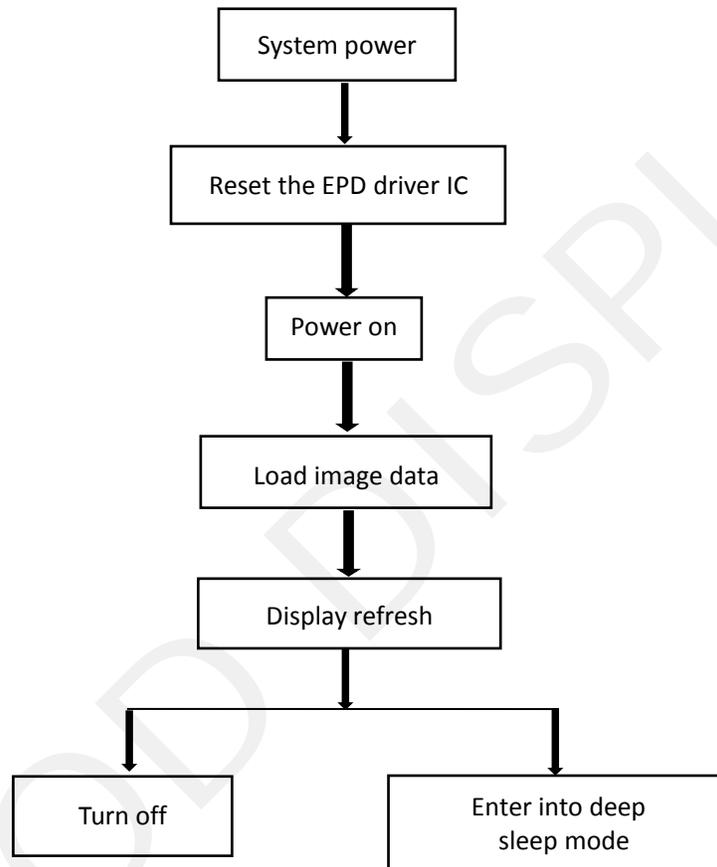
DESPI Development Kit consists of the development board and the pinboard.

More details about the Development Kit, please click to the following link:

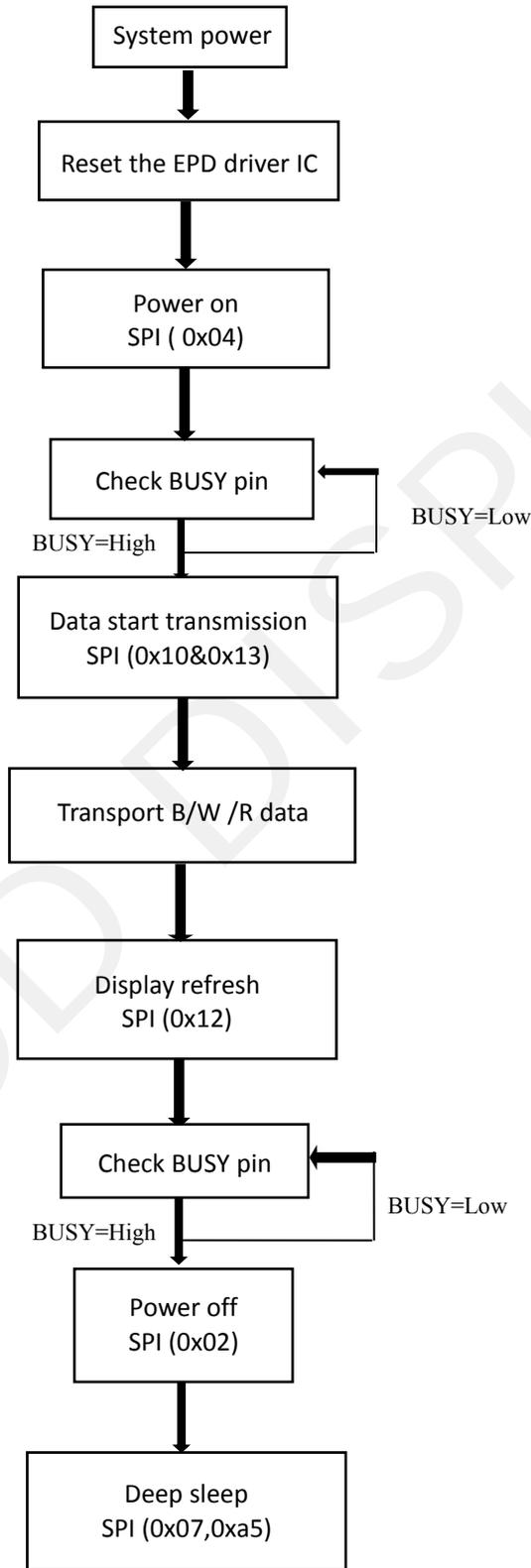
<https://www.good-display.com/product/53/>

## 14 Typical Operating Sequence

### 14.1 LUT from OTP Operation Flow



### 14.2 LUT from OTP Operation Reference Program Code



## 15. Inspection condition

### 15.1 Environment

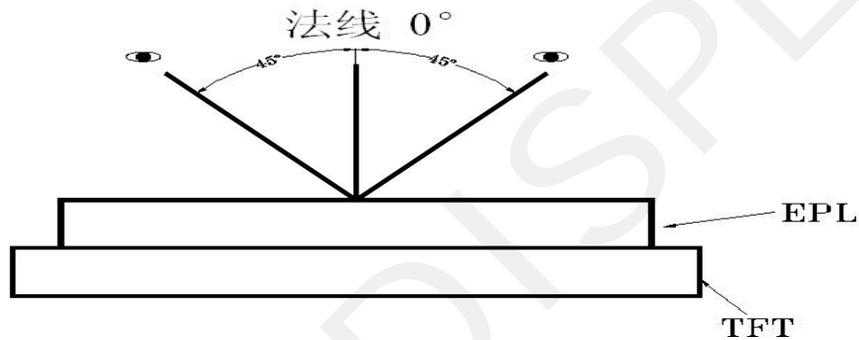
Temperature:  $23 \pm 3^\circ\text{C}$

Humidity:  $55 \pm 10\% \text{RH}$

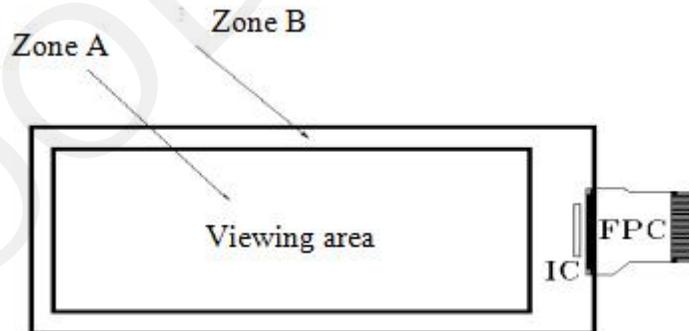
### 15.2 Illuminance

Brightness:  $1200 \sim 1500 \text{LUX}$ ; distance: 30CM; Angle: Relate  $45^\circ$  surround.

### 15.3 Inspect method

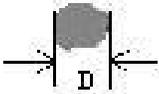
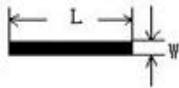


### 15.4 Display area

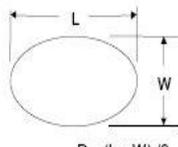
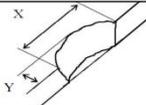
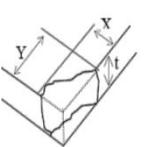
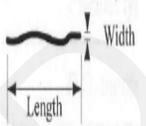


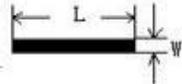
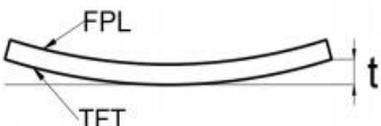
## 15.5 Inspection standard

### 15.5.1 Electric inspection standard

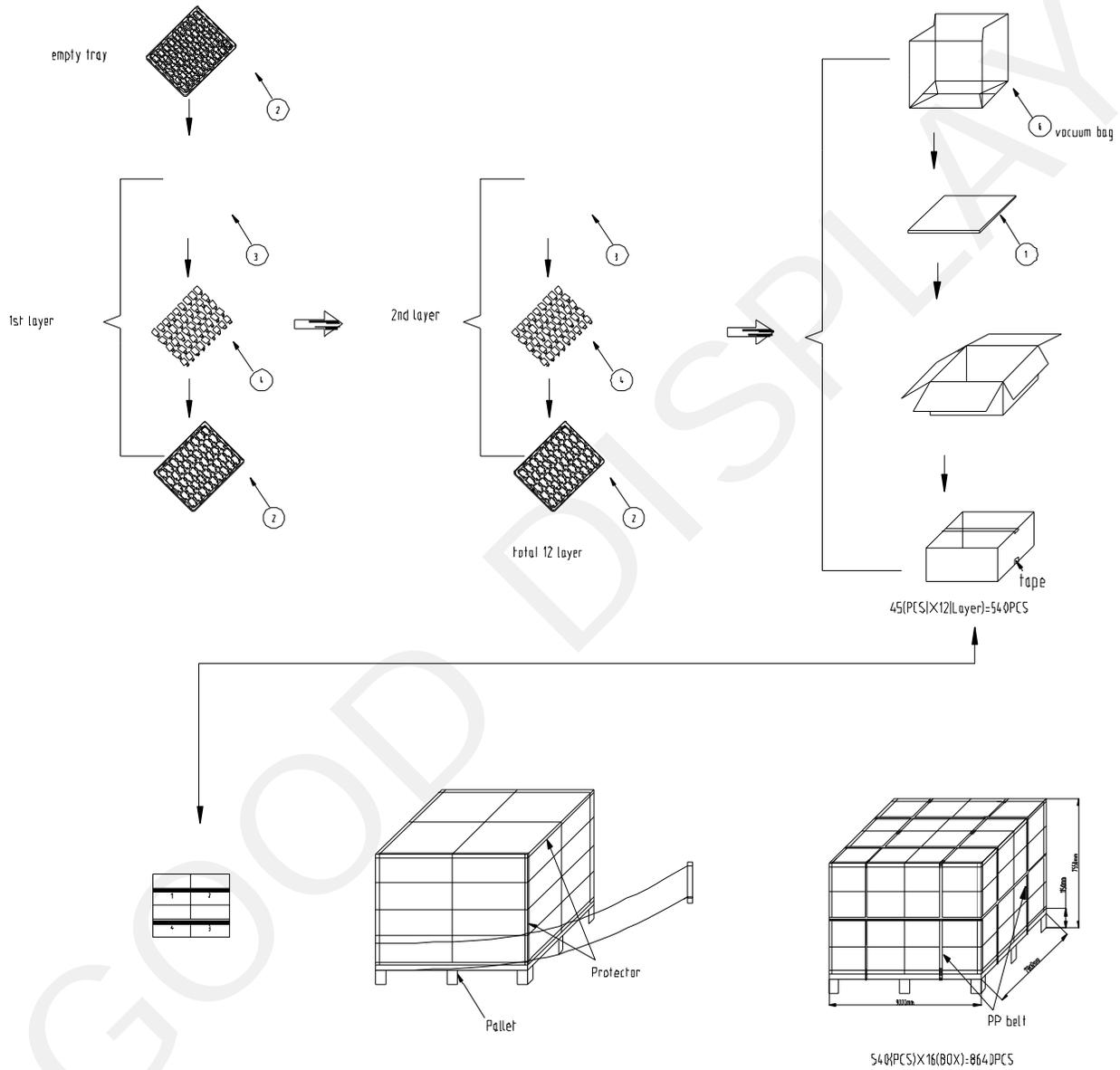
NO.	Item	Standard	Defect level	Method	Scope
1	Display	Clear display Display complete Display uniform	MA		
2	Black/White spots	 <p> <math>D \leq 0.3\text{mm}</math>, negligible  <math>0.3\text{mm} &lt; D \leq 0.5\text{mm}</math>, <math>N \leq 5</math>, Allowed  <math>0.5\text{mm} &lt; D</math> Not Allow                 </p>	MI	Visual inspection	Zone A
3	Black/White spots (No switch)	 <p> <math>L \leq 1.0\text{mm}</math>, <math>W \leq 0.15\text{mm}</math> negligible  <math>1.0\text{mm} &lt; L \leq 4.0\text{mm}</math>  <math>0.15\text{mm} &lt; W \leq 0.5\text{mm}</math>  <math>N \leq 4</math> allowable  <math>L &gt; 4.0\text{mm}</math>, <math>W &gt; 0.5\text{mm}</math> is not allowed                 </p>		Visual/ Inspection card	
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash dot / Multilateral	Flash points are allowed when switching screens Multilateral colors outside the frame are allowed for fixed screen time	MI	Visual/ Inspection card	Zone A Zone B
6	Segmented display	Selection segments are all displayed, and other segments are not displayed after the selection segment.	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Abnormal Display	Not Allow			

**15.5.2 Appearance inspection standard**

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 <p><math>D = (L + W) / 2</math>  <math>D \leq 0.3\text{mm}</math>, Allowed  <math>0.3\text{mm} &lt; D \leq 0.5\text{mm}</math>, <math>N \leq 5</math>  <math>D &gt; 0.5\text{mm}</math>, Not Allow</p>	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	\Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 <p><math>X \leq 3\text{mm}, Y \leq 0.5\text{mm}</math></p>  <p><math>2\text{mm} \leq X</math> or <math>2\text{mm} \leq Y</math> not Allow</p>  <p><math>W \leq 0.1\text{mm}, L \leq 5\text{mm}, n \leq 2</math>  Edge crown: <math>X \leq 0.3\text{mm}, Y \leq 3\text{mm}</math></p>	MI	Visual / Microscope	Zone A Zone B
5	TFT Cracks	 <p>Not Allow</p>	MA	Visual / Microscope	Zone A Zone B
6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	Visual / Microscope	Zone A / Zone B
7	FPC broken/ FPC oxidation / scratch	  <p>Not Allow</p>	MA	Visual / Microscope	Zone B

8	B/W Line	 <p> <math>L \leq 1.0\text{mm}</math>, <math>W \leq 0.15\text{mm}</math>                      negligible  <math>1.0\text{mm} &lt; L \leq 4.0\text{mm}</math>  <math>0.15\text{mm} &lt; W \leq 0.5\text{mm}</math>  <math>N \leq 4</math> allowable  <math>L &gt; 4.0\text{mm}</math>, <math>W &gt; 0.5\text{mm}</math> is not allowed                 </p>	MI	Visual / Ruler	Zone B
9	TFT edge bulge /TFT chromatic aberration	<p>TFT edge bulge:  <math>X \leq 3\text{mm}</math>, <math>Y \leq 0.3\text{mm}</math> Allowed                      TFT chromatic aberration :Allowed</p>	MI	Visual / Microscope	Zone A Zone B
10	Electrostatic point	<p> <math>D \leq 0.25\text{mm}</math>, allow  <math>0.25\text{mm} &lt; D \leq 0.4\text{mm}</math>, <math>n \leq 4</math> allow  <math>D &gt; 0.4\text{mm}</math> is not allowed                      (<math>n \leq 8</math> items are allowed within 5 mm in diameter)                 </p>	MI	Visual / Microscope	Zone A
11	PCB damaged/ Poor welding/ Curl	<p>PCB (Circuit area) damaged Not Allow                      PCB Poor welding Not Allow                      PCB Curl <math>\leq 1\%</math></p>	MI	Visual / Ruler	Zone B
12	Edge glue height/ Edge glue bubble	<p>Edge Adhesives <math>H \leq</math>PS surface (Including protect film) Edge adhesives seep in <math>\leq 1/2</math> Margin width                      Length excluding Edge adhesives bubble: bubble Width <math>\leq 1/2</math> Margin width; Length <math>\leq 5.0\text{mm}</math>. <math>n \leq 5</math></p>	MI		
13	Protect film	Surface scratch but not effect protect function, Allow	MI	Visual Inspection	Zone B
14	Silicon glue	<p>Thickness <math>\leq</math> PS surface(With protect film): Full cover the IC;                      Shape:                      The width on the FPC <math>\leq 0.5\text{mm}</math> (Front)                      The width on the FPC <math>\leq 1.0\text{mm}</math> (Back)                      smooth surface, No obvious raised.</p>	MI	Visual Inspection	
15	Warp degree (TFT substrate)	 <p> <math>t \leq 1.5\text{mm}</math> </p>	MI	Ruler	
16	Color difference in COM area (Silver point area)	Allowed		Visual Inspection	

## 16. Packing



## 17. Precautions

- (1) Do not apply pressure to the EPD panel in order to prevent damaging it.
- (2) Do not connect or disconnect the interface connector while the EPD panel is in operation.
- (3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.
- (4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.
- (5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL /EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue
- (6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.
- (7) For more precautions, please click on the link:  
<https://www.good-display.com/news/80.html>