0.97 inch
E-paper Display Series
GDEM0097T61

GooDisplay®

Dalian Good Display Co., Ltd.

Product Specifications

Customer	**Standard**
Description	**0.97" E-PAPER DISPLAY**
Model Name	**GDEM0097T61**
Date	**2023 / 07 / 19**
Revision	**1.0**

	Design Engineering		
	Approval	**Check**	**Design**
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1. Over View

GDEM0097T61 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white and black full display capabilities.The 0.97inch active area contains 184×88 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2. Features

- ◆184×88 pixels display
- ◆High contrast High reflectance
- ◆Ultra wide viewing angle Ultra low power consumption
- ◆Pure reflective mode
- ◆Bi-stable display
- ◆Commercial temperature range
- ◆Landscape portrait modes
- ◆Hard-coat antiglare display surface
- ◆Ultra Low current deep sleep mode
- ◆On chip display RAM
- ◆Waveform can stored in On-chip OTP or written by MCU
- ◆Serial peripheral interface available
- ◆On-chip oscillator
- ◆On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- ◆I^2C signal master interface to read external temperature sensor
- ◆Built-in temperature sensor

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3. Mechanical Specification

Parameter	Specifications	Unit	Remark
Screen Size	0.97	Inch	
Display Resolution	88(H)×184(V)	Pixel	DPI:210
Active Area	10.65×22.26	mm	
Pixel Pitch	0.121×0.121	mm	
Pixel Configuration	Square		
Outline Dimension	14.15(H)×30.0 (V) ×1.0(D)	mm	
Weight	0.89±0.5	g	

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
KS	Black State L* value		-	18	20		3-1
	Black Ghosting ΔL		-	1	-		3-1
WS	White State L* value		66	67			3-1
	White Ghosting ΔL		-	1	-		3-1
R	White Reflectivity	White	30	34	-	%	3-1
CR	Contrast Ratio	Indoor	15:1	20:1	-		3-1 3-2
GN	2Grey Level	-	-	-	-		
Life		Temp:23±3°C Humidity:55±10%RH		5years			3-3

Notes: 3-1. Luminance meter: Eye-One Pro Spectrophotometer.

3-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

3-3. When the product is stored. The display screen should be kept white and face up.

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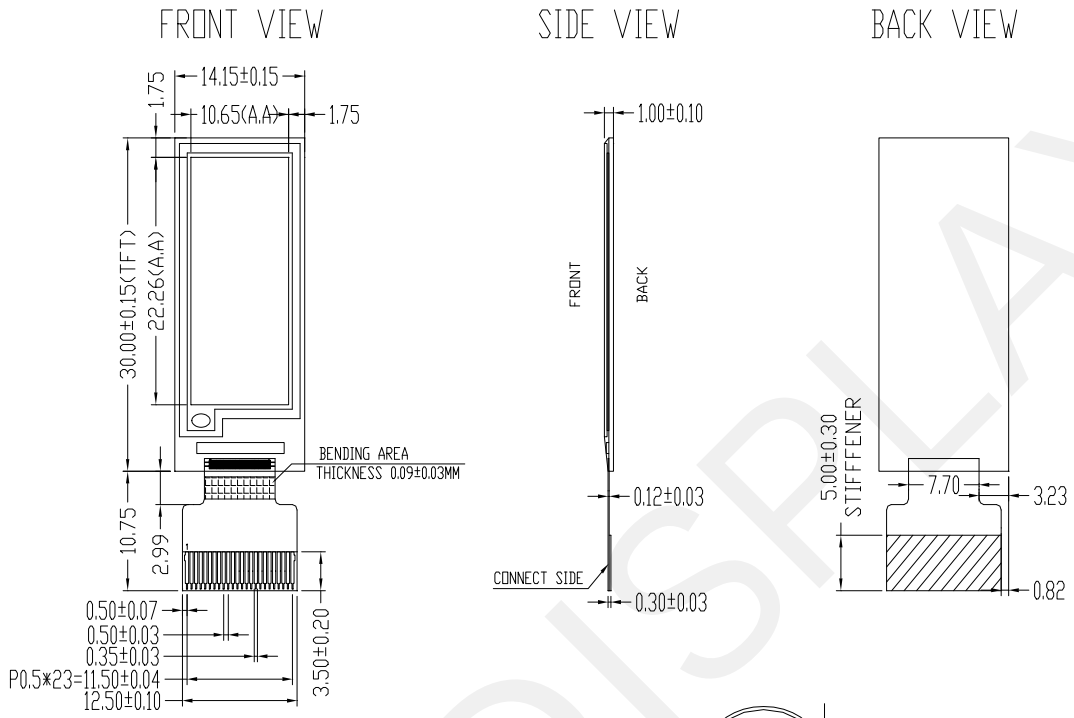
4.Mechanical Drawing of EPD Module

Confirmation:

DATE	REV.	MODIFICATION
2021-06-21	A	FIRST ISSUE



RoHS

NOTE

1 DISPLAY MODE 0.97" ARREY FOR EPD
2 DRIVER IC:SSD1680
3 RESOLUTION:184gateX88source
4 PIXEL SIZE:0.121mmX0.121mm

TOLERANCES UNMARKED	TITLE:	PROJECT:		REV.:	DATE:	CUST. P/N:
ANGLES ±5°	EPD	GDEM0097T61		A	22.06.21	
.X= ±0.4mm	DWN.	CHK.	APPR.	UNIT:	3RD ANGLE:	PAGE:
.XX= ±0.20mm	NN ZHAO	CC ZHENG	XFNE	mm		1/1
.XXX= ±0.20mm						

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5. Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	GDR	O	N-Channel MOSFET Gate Drive Control	
2	RESE	I	Current Sense Input for the Control Loop	
3	VSHR	C	Positive Source driving voltage(Red)	
4	BUSY	O	Busy state output pin	Note 5-4
5	RES#	I	Reset signal input. Active Low.	Note 5-3
6	D/C#	I	Data /Command control pin	Note 5-2
7	CS#	I	Chip select input pin	Note 5-1
8	SCL	I	Serial Clock pin (SPI)	
9	SDA	I/O	Serial Data pin (SPI)	
10	VCI	P	Power Supply for the chip	
11	VSS	P	Ground	
12	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
13	VPP	P	FOR TEST	Keep Open
14	VSH1	C	Positive Source driving voltage	
15	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
16	VSL	C	Negative Source driving voltage	
17	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
18	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

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Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when -Outputting display waveform -Communicating with digital temperature sensor.

Note 5-5: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to VCI +0.5	V
Logic Output voltage	VOUT	-0.5 to VCI +0.5	V
Operating Temp range	TOPR	0 to +50	ºC.
Storage Temp range	TSTG	-25 to+70	ºC.
Optimal Storage Temp	TSTGo	23±2	ºC.
Optimal Storage Humidity	HSTGo	55±10	%RH

Note:

Maximum ratings are those values beyond which damages to the device may occur.

Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

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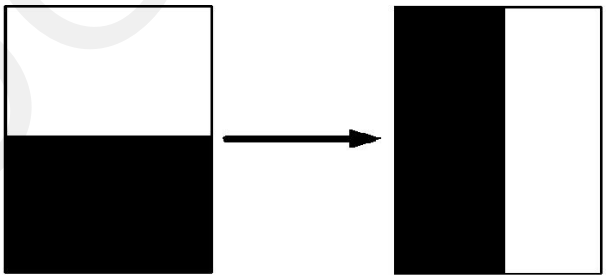
6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{CI}	-	VCI	2.3	3.0	3.6	V
Core logic voltage	V_{DD}		VDD	1.7	1.8	1.9	V
High level input voltage	V_{IH}	-	-	0.8 V_{CI}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 V_{CI}	V
High level output voltage	V_{OH}	IOH = -100uA	-	0.9 V_{CI}	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	0.1 V_{CI}	V
Typical power	P_{TYP}	V_{CI} =3.0V	-	-	6	-	mW
Deep sleep mode	P_{STPY}	V_{CI} =3.0V	-	-	0.003	-	mW
Typical operating current	Iopr_VCI	V_{CI} =3.0V	-	-	2.0	- -	mA
Full update time	-	25 ºC	-	-	3	-	sec
Partial update time	-	25 ºC	-	-	0.26	-	sec
Typical peak current	Iopr_VCI	2.3~3.6v			20	30	mA
Sleep mode current	Islp_V_{CI}	DC/DC off No clock No input load Ram data retain	-	-	20		uA
Deep sleep mode current	Idslp_V_{CI}	DC/DC off No clock No input load Ram data not retain	-	-	1	5	uA

Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical characteristics are only guaranteed under the controller & waveform provided by Good Display.
4. Electrical measurement：Tektronix oscilloscope - MDO3024，

   Tektronix current probe–TCP0030A.

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6.3 Panel AC Characteristics

6.3.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-3-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

6.3.2 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

In the write mode SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte . The data byte in the shift register is written to the Graphic Display Data RAM /Data Byte register or command Byte register according to D/C# pin.

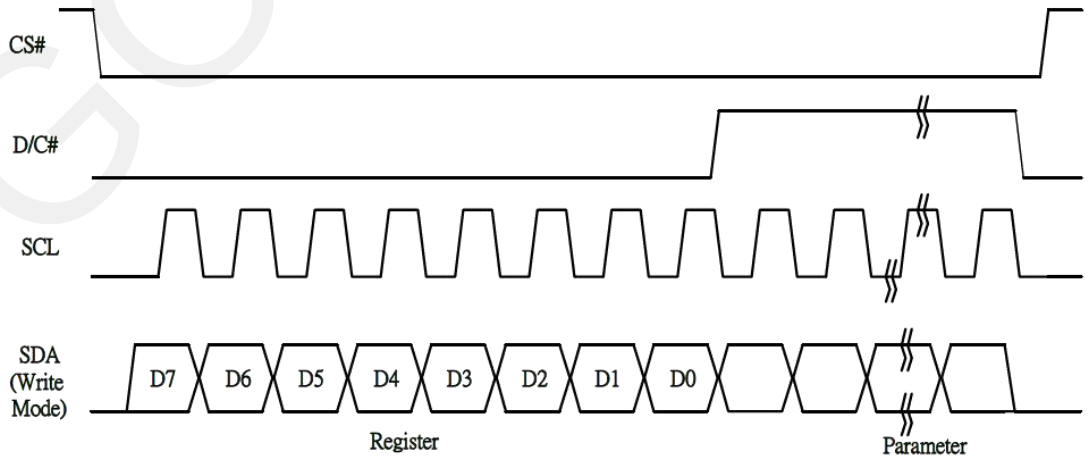


Figure 6-1: Write procedure in 4-wire SPI mode

In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0 with D/C# keep low.
3. After SCL change to low for the last bit of register, D/C# need to drive to high.
4. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, … D0.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

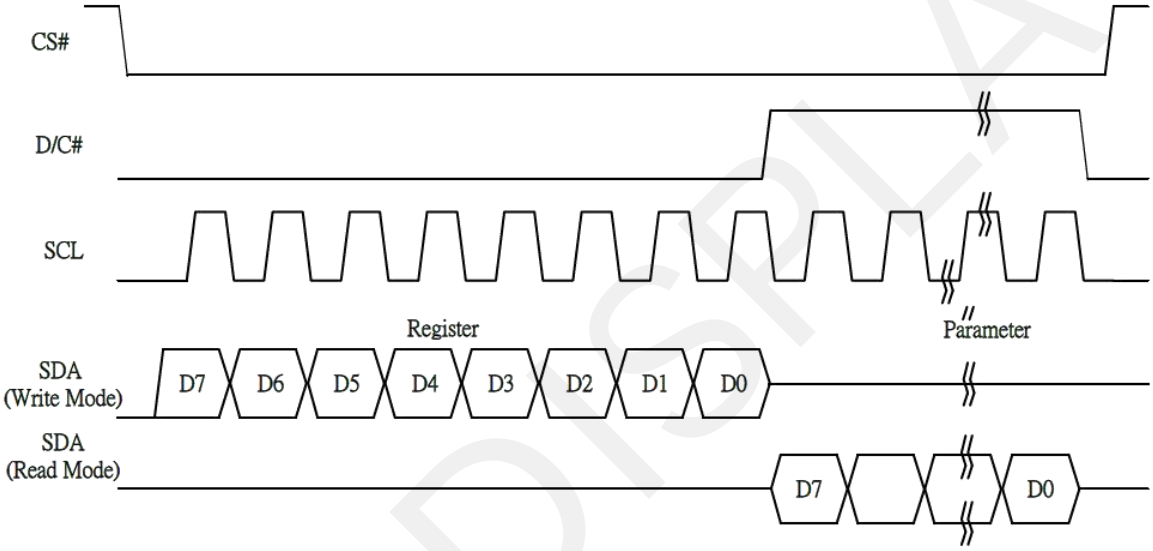


Figure 6-2: Read procedure in 4-wire SPI mode

6.3.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCL, serial data SDA and CS#. This interface also supports Write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

Note：↑ stands for rising edge of signal

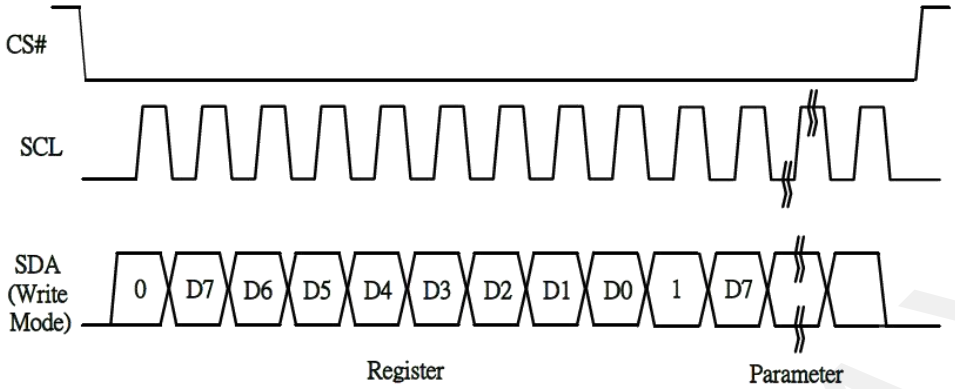


Figure 6-3: Write procedure in 3-wire SPI mode

In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. D/C=0 is shifted thru SDA with one rising edge of SCL
3. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0.
4. D/C=1 is shifted thru SDA with one rising edge of SCL
5. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, … D0.
6. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

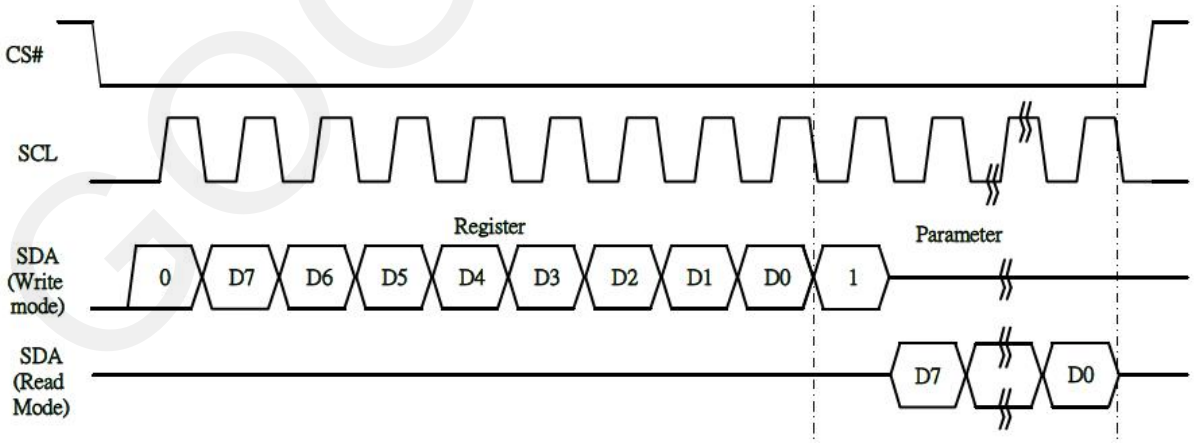
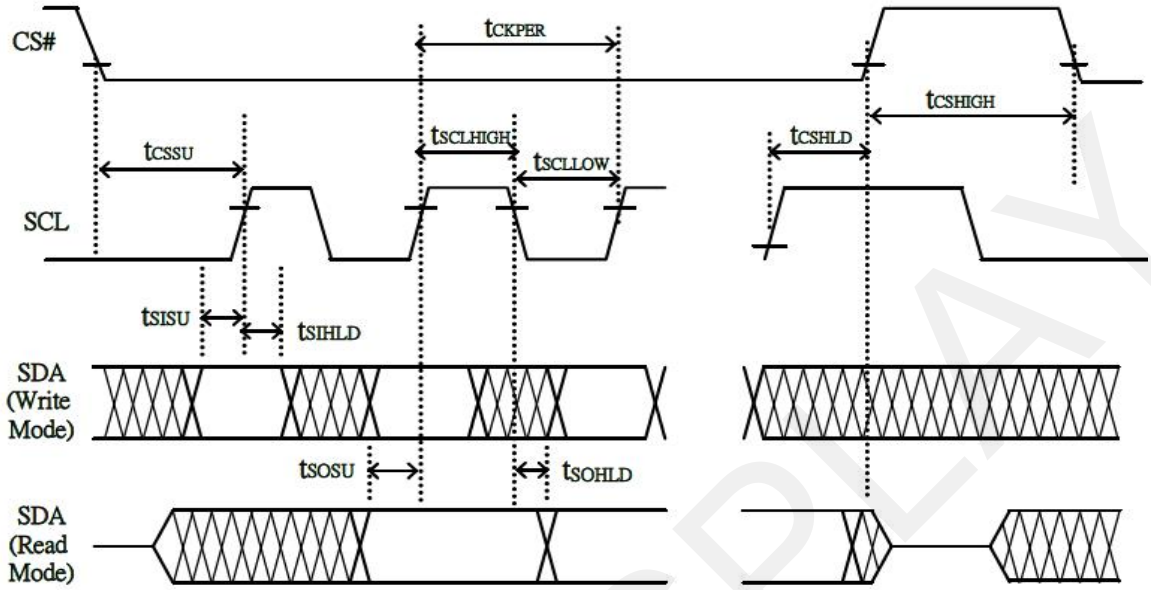


Figure 6-4: Read procedure in 3-wire SPI mode

6.3.4 Interface Timing

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23ºC.



Changed Diagram

Serial Interface Timing Characteristics
(VCI - VSS = 2.2V to 3.7V, TOPR = 23°C, CL=20pF)

Write mode

Symbol	Parameter	Min	Typ.	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	60			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	65			ns
tCSHIGH	Time CS# has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

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Read mode

Symbol	Parameter	Min	Typ.	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CS# has to remain high between two transfers	250			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

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7.Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting Set A[8:0]=0097h Set B[8:0]=00h
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	1		0	0	0	0	0	0	0	A8		
0	1		0	0	0	0	0	B2	B1	B0		
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control: A[1:0] : Description 00 Normal Mode [POR] 01 Enter Deep Sleep Mode 1 11 Enter Deep Sleep Mode 2 After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver
0	1		0	0	0	0	0	0	0	A_0		
0	1		1	A6	A5	A4	A3	A2	A1	A0		
0	1		1	B6	B5	B4	B3	B2	B1	B0		
0	1		1	C6	C5	C4	C3	C2	C1	C0		
0	1		0	0	D5	D4	D3	D2	D1	D0		
0	0	12	0	0	0	1	0	0	1	0	SWRESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command.
0	0	18	0	0	0	1	1	0	0	0	Temperature Sensor Control	Temperature Sensor Selection A[7:0] = 48h [POR], external temperature sensor A[7:0] = 80h Internal temperature sensor
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h User should not interrupt this operation to avoid corruption of panel images.

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0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation A[7:0]= FFh (POR) Operating sequence Parameter (in Hex) Enable clock signal 80 Disable clock signal 01 Enable clock signal Enable Analog C0 Disable Analog Disable clock signal 03 Enable clock signal Load LUT with DISPLAY Mode 1 Disable clock signal C7 Enable clock signal Enable Analog Display with DISPLAY Mode 2 Disable Analog Disable OSC F7 Enable clock signal Enable Analog Load temperature value DISPLAY with DISPLAY Mode 2 Disable Analog Disable OSC FF
0	1		A7	A6	A5	A4	A3	A2	A1	A0		
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x01] A[5]: HV Ready Detection flag [POR=0] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively

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0	0	3C	0	0	1	1	1	1	0	0		Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HIZ. A [7:6] :Select VBD option A[7:6] Select VBD as 00 GS Transition, Defined in A[2] and A[1:0] 01 Fix Level, Defined in A[5:4] 10 VCOM 11[POR] HiZ A [5:4] Fix Level Setting for VBD A[5:4] VBD level 00 VSS 01 VSH1 10 VSL 11 VSH2 A[2] GS Transition control A[2] GS Transition control 0 Follow LUT (Output VCOM @ Yellow) 1 Follow LUT A [1:0] GS Transition setting for VBD A[1:0] VBD Transition 00 LUT0 01 LUT1 10 LUT2 11 LUT3
0	1		A_7	A_6	A_5	A_4	0	0	A_1	A_0		
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit A[4:0]: XSA[4:0], X Start, POR = 00h B[4:0]: XEA[4:0], X End, POR = 0Ch
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	B_4	B_3	B_2	B_1	B_0		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y-address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[8:0]: YSA[8:0], Y Start, POR = 00D3h B[8:0]: YEA[8:0], Y End, POR = 0000h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	0	0	0	0	0	B_8		
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[4:0]: XAD[4:0], POR is 00h
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: YAD[8:0], POR is 00D3h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		

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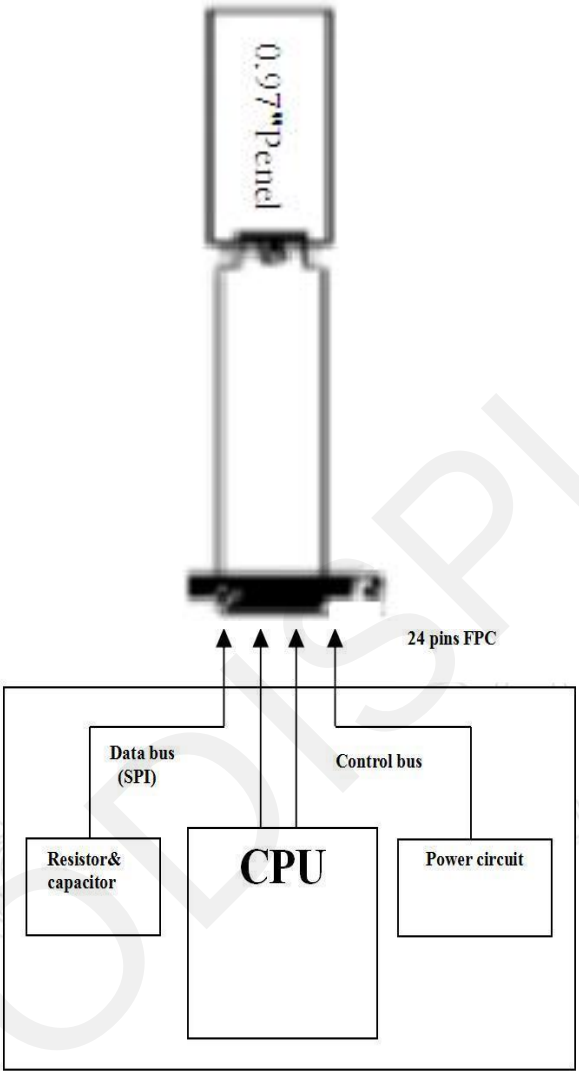
8.Block Diagram



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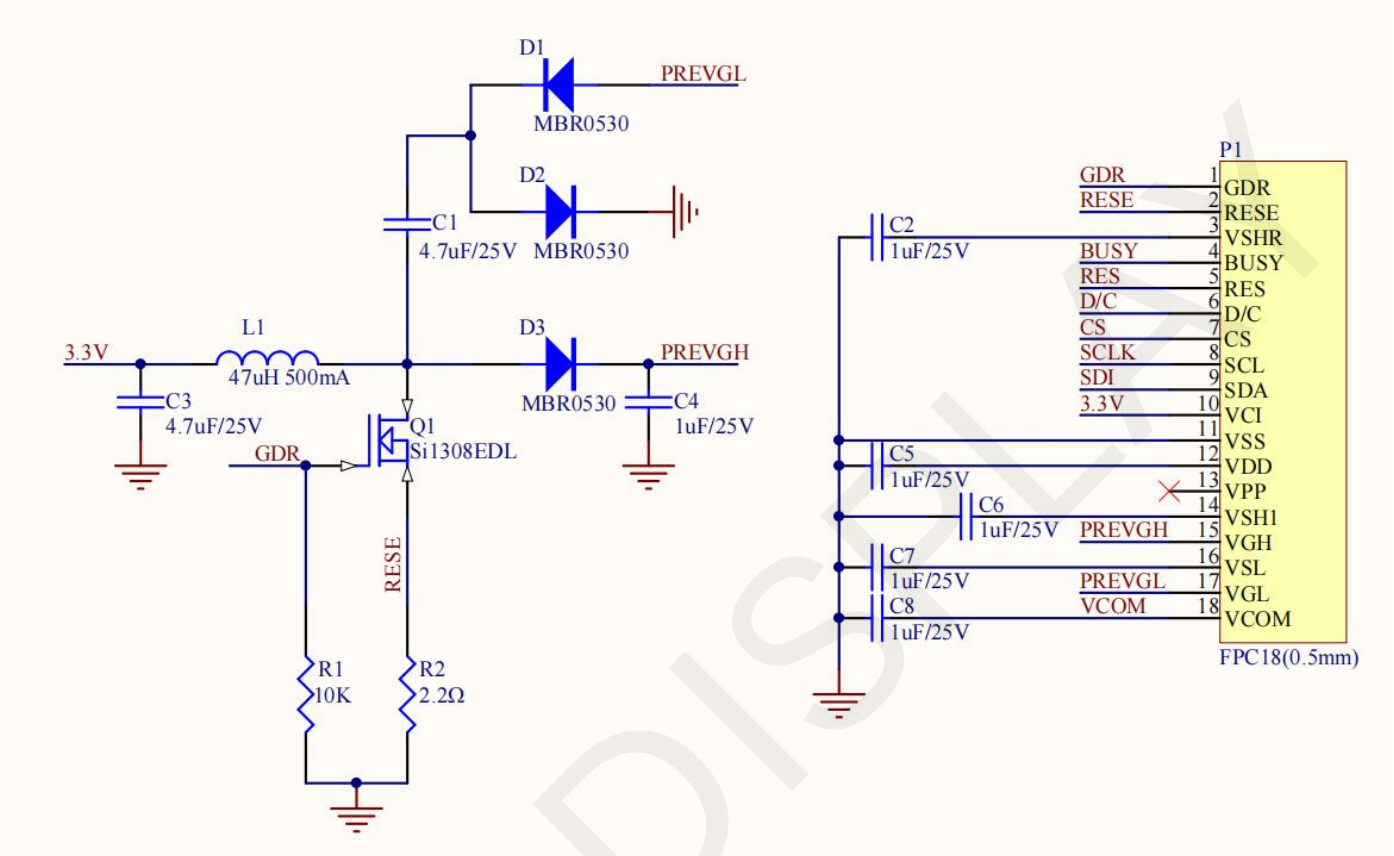
9. Typical Application Circuit with SPI Interface



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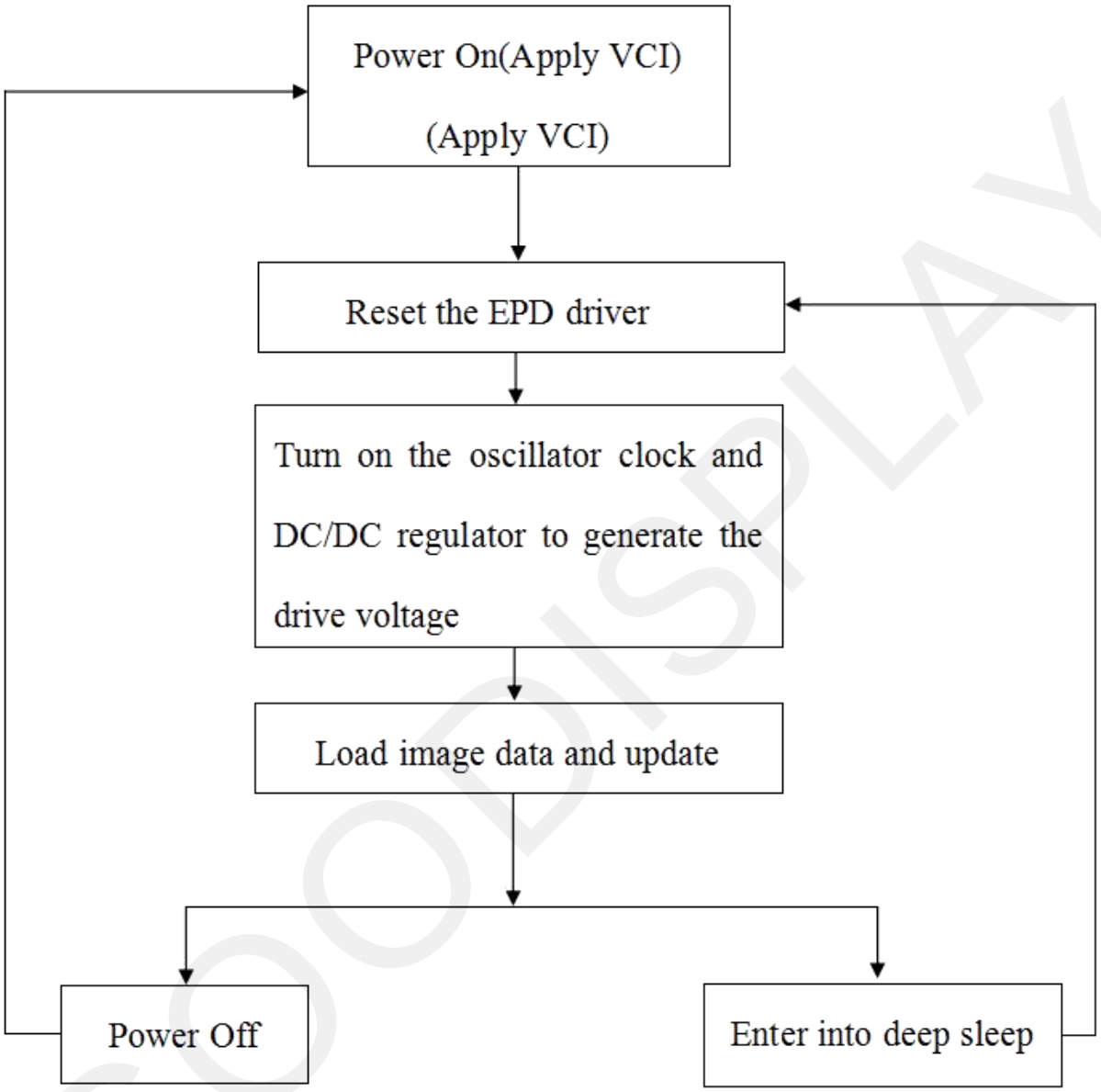
10 Typical Operating Sequence

10.1 LUT from OTP Operation Flow



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10.2 OTP Operation Reference Program Code

ACTION	VALUE/DATA	COMMENT
POWER ON		
delay	10ms	
PIN CONFIG		
RESE#	low	Hardware reset
delay	200us	
RESE#	high	
delay	200us	
Read busy pin		Wait for busy low
Command 0x12		Software reset
Read busy pin		Wait for busy low
SET VOLTAGE AND LOAD LUT		
LOAD IMAGE AND UPDATE		
Command 0x24	4000 bytes	Load BW image (122/8*250)(BW)
Command 0x20		
Read busy pin		Wait for busy low
Command 0x10	Data 0X01	Enter deep sleep mode
POWER OFF		

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12.Inspection condition

12.1 Environment

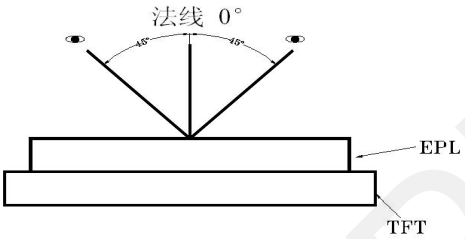
Temperature： 23±3℃

Humidity： 55±10%RH

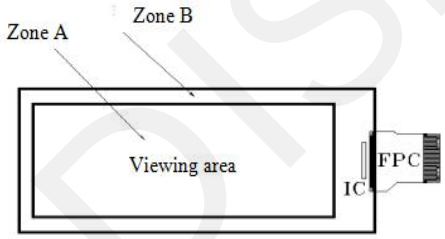
12.2 Illuminance

Brightness:1200～1500LUX;distance:20-30CM;Angle:Relate 45°surround.

12.3 Inspect method

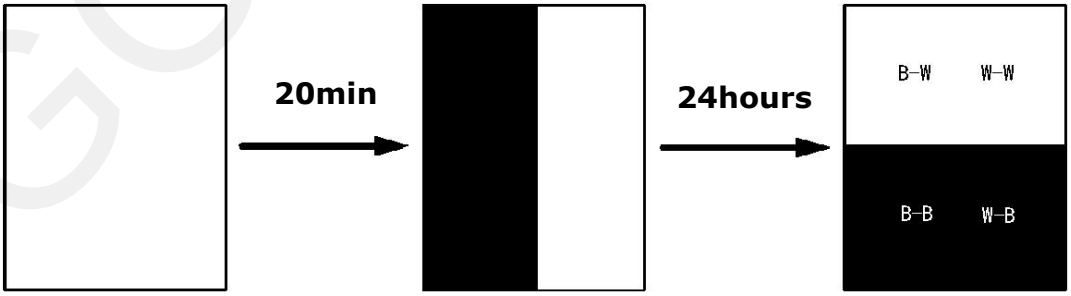


12.4 Display area



12.5 Ghosting test method

Two-color ghosting is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern. The listed optical characteristics are only guaranteed under the controller & waveform provided by Good Display.



1)Measurement Instruments：X-rite i1Pro

2)Ghosting formula:

W ghosting：△L= Max (ΔL(W-W, B-W)) - Min (ΔL(W-W B-W))

3)K ghosting：△L= Max (ΔL(W-B, B-B)) - Min(ΔL(W-B, B-B))

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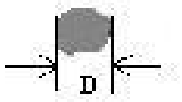
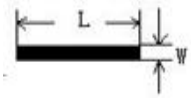
12.6 Inspection standard

12.6.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Display complete Display uniform	MA	Visual inspection	Zone A
2	Black/White spots	 D≤0.25mm，Allowed 0.25mm＜D≤0.4mm。 N≤4 allowable D＞0.4mm is not allowed	MI		
3	Show B/W lines	 L≤0.4mm,W≤0.1mm negligible 0.4mm＜L≤1.0mm 0.1mm＜W≤0.4mm N≤4 allowable L＞1.0mm ,W＞0.4mm is not allowed		Visual/ Inspection card	
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash spots/ Larger FPL size	Flash spots in switching, Allowed FPL size larger than viewing area, Allowed	MI	Visual/ Inspection card	Zone A Zone B
6	Display wrong/Missing	All appointed displays are showed correct	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Display abnormal	Not Allow			

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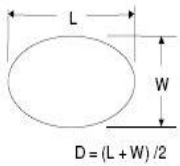
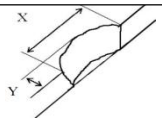
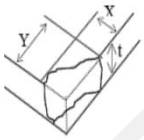
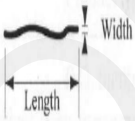
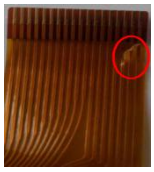
12.6.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 D≤0.25mm negligible 0.25mm＜D≤0.4mm N≤4 allowable D＞0.4mm is not allowed	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 X≤3mm,Y≤0.5mm And without affecting the electrode is permissible  2mm≤X or 2mm≤Y Not Allow  W≤0.1mm,L≤5mm, No harm to the electrodes and N≤2 allow	MI	Visual / Microscope	Zone A Zone B
5	TFT Cracks	 Not Allow	MA	Visual / Microscope	Zone A Zone B
6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	Visual / Microscope	Zone A / Zone B
7	FPC broken/ Goldfingers xidation/ scratch	 Not Allow	MA	Visual / Microscope	Zone B

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8	TFT edge bulge /TFT chromatic aberration	TFT edge bulge： X≤3mm，Y≤0.3mm Allowed TFT chromatic aberration :Allowed	MI	Visual / Microscope	Zone A Zone B
9	PCB damaged/ Poor welding/ Curl	PCB（Circuit area）damaged Not Allow PCB Poor welding Not Allow PCB Curl≤1%	MI	Visual / Ruler	Zone B
10	Edge glue height/ Edge glue bubble	Edge Adhesives H≤PS surface (Including protect film) Edge adhesives seep in≤1/2 Margin width Length excluding Edge adhesives bubble：bubble Width ≤1/2 Margin width；Length ≤0.5mm。n≤5			
11	Protect film	Surface scratch but not effect protect function, Allowed		Visual Inspection	
12	Silicon glue	Thickness≤PS surface(With protect film): Full cover the IC; Shape: The width on the FPC ≤ 0.5mm (Front) The width on the FPC≤1.0mm (Back) smooth surface, No obvious raised.	MI	Visual Inspection	
13	Warp degree (TFT substrate)	 t≤1.0mm	MI	Ruler	
14	Color difference in COM area (Silver point area)	Allowed		Visual Inspection	

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13. Matched Development Kit

Our Development Kit designed for SPI E-paper Display aims to help users to learn how to use E-paper Display more easily. It can refresh black-white E-paper Display, three-color (black, white and red/Yellow) E-paper Display and four-color(black, white, red and yellow) Good Display 's E-pa per Display. And it is also added the functions of USB serial port, FLASH c hip, font chip, current detection ect.
Development Kit consists of the development board and the pinboard.

Supported development platforms include STM32, ESP32, ESP8266, Arduino UNO, etc. More details, please click to the following links:

STM32	https://www.good-display.com/product/219.html
ESP32	https://www.good-display.com/product/338.html
ESP8266	https://www.good-display.com/product/220.html
Arduino UNO	https://www.good-display.com/product/222.html

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14. Handling, Safety and Environmental Requirements

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

Product Environmental certification
RoHS

15. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.

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