25.3 inch
E-paper Display Series

GDEH253C01

Dalian Good Display Co., Ltd.

Product Specifications

Customer	**Standard**
Description	**25.3” E-PAPER DISPLAY**
Model Name	**GDEH253C01**
Date	**2024/04/30**
Revision	**1.0**

	Design Engineering		
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1. General Description

GDEH253C01 is a reflective electrophoretic E Ink® Advanced Color ePaper (ACeP®) technology display module based on active matrix TFT substrate. The diagonal length of active area is 25.3" and contains 3200 x 1800 pixels. The display is capable to display full color images depending on the display controller and the associated lookup table used.

2.Features

- Full color display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Image stable
- Landscape/Portrait mode
- Bi-stable display
- Commercial temperature range (15 ~ 35 ℃)

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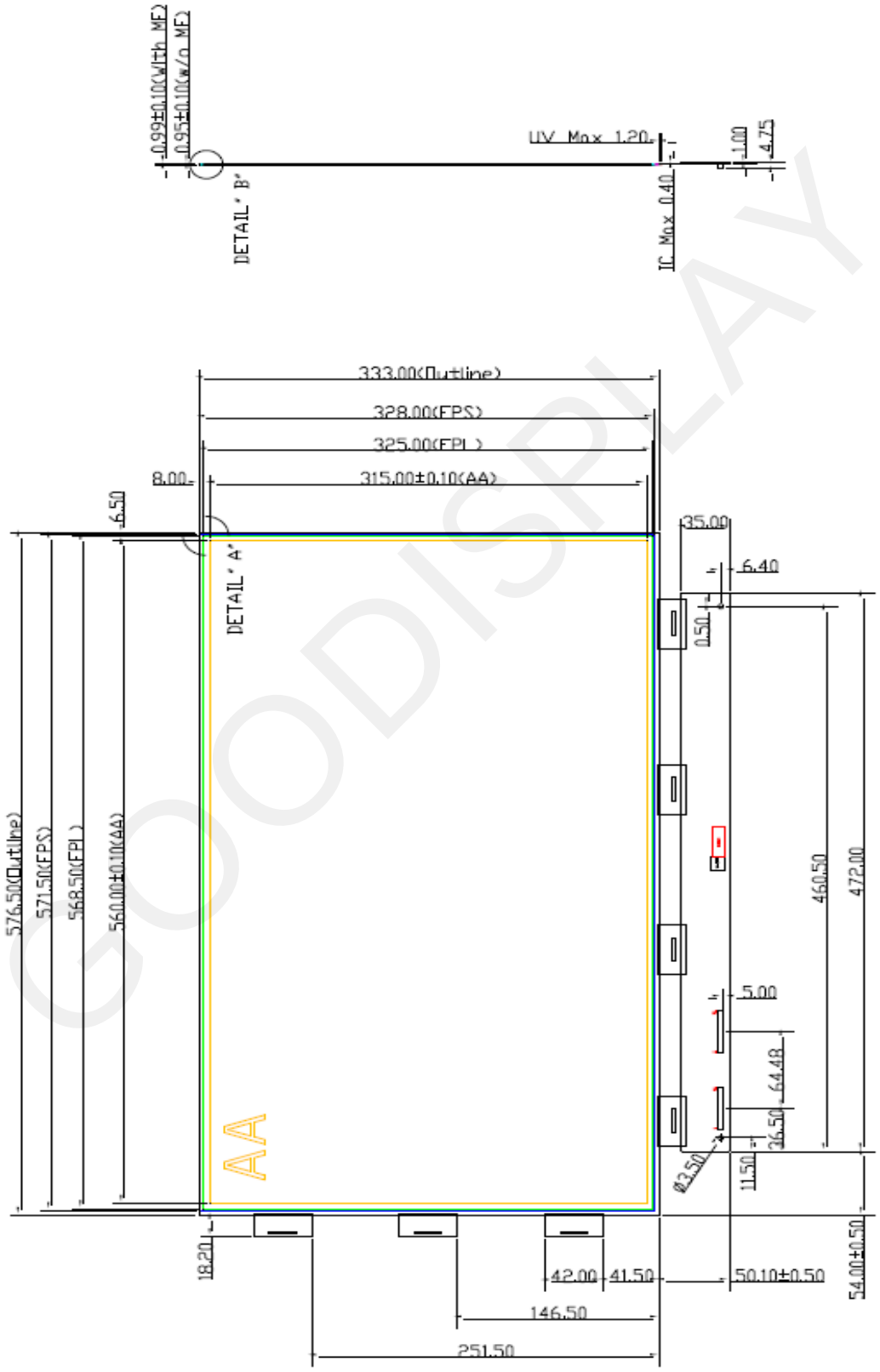
3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	25.3	Inch	
Display Resolution	3200(H) x 1800(V)	Pixel	16:9
Active Area	560.0(H) x 315.0(V)	mm	
Pixel Pitch	0.175(H) x 0.175(V)	mm	
Pixel Configuration	Rectangle		
Outline Dimension	576.5(W) × 333.0(H) × 0.953(D)	mm	w/o masking film
Module Weight	426	g	
Display operating mode	Reflective mode		
Surface treatment	Anti-glare		

4. Mechanical Drawing of EPD module



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5 Input/Output Terminals

5.1 Pin Assignment

CON1 (P-TWO 187059-51221 compatible)

Pin	Signal	Description	Remark
1	FPL_VCOM_3	Common Voltage	
2	FPL_VCOM_2	Common Voltage	
3	FPL_VCOM_1	Common Voltage	
4	NC	No Connection	
5	TFT_VCOM	Common Voltage	
6	TFT_VCOM	Common Voltage	
7	NC	No Connection	
8	BORDER	Border connection	
9	NC	No Connection	
10	VGH	Positive power supply gate driver	
11	VGH	Positive power supply gate driver	
12	NC	No Connection	
13	VP3	Positive power supply source driver.	
14	VP3	Positive power supply source driver.	
15	VP3	Positive power supply source driver.	
16	NC	No Connection	
17	VP2	Positive power supply source driver.	
18	VP2	Positive power supply source driver.	
19	VP2	Positive power supply source driver.	
20	NC	No Connection	
21	VP1	Positive power supply source driver.	
22	VP1	Positive power supply source driver.	
23	VP1	Positive power supply source driver.	
24	NC	No Connection	
25	VDD	Digital power supply drivers	
26	VDD	Digital power supply drivers	
27	NC	No Connection	
28	VDM(GND)	Ground	
29	VDM(GND)	Ground	
30	NC	No Connection	
31	VN1	Negative power supply source driver.	
32	VN1	Negative power supply source driver.	
33	VN1	Negative power supply source driver.	
34	NC	No Connection	
35	VN2	Negative power supply source driver.	
36	VN2	Negative power supply source driver.	
37	VN2	Negative power supply source driver.	
38	NC	No Connection	
39	VN3	Negative power supply source driver.	
40	VN3	Negative power supply source driver.	
41	VN3	Negative power supply source driver.	
42	NC	No Connection	
43	VGL	Negative power supply gate driver	
44	VGL	Negative power supply gate driver	
45	NC	No Connection	
46	NC	No Connection	
47	NC	No Connection	

48	NC	No Connection	
49	STBYB	mini-LVDS enable.	
50	XON	All the gate pins output mode	
51	MODE	Output mode selection gate driver	

CON2 (P-TWO 187059-51221 compatible)

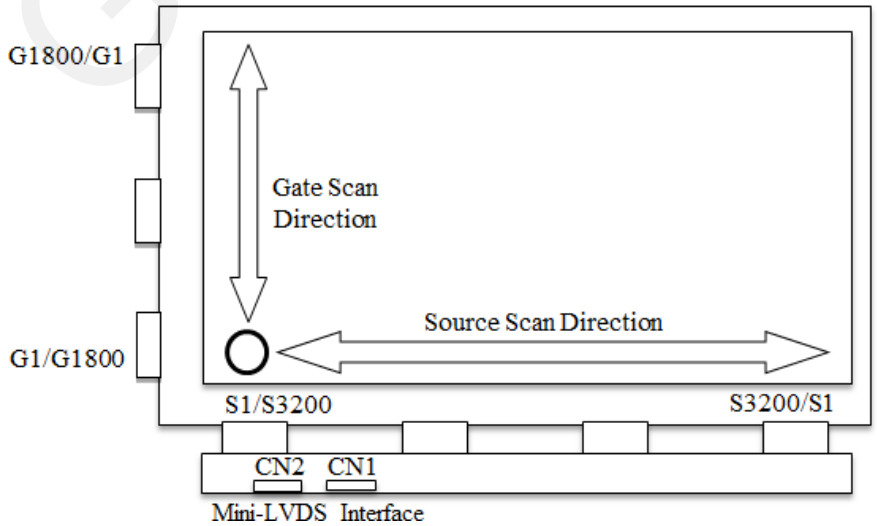
Pin	Signal	Description			Remark
1	DSEL	Data Input select			
2	LEH	Latch enable source driver			
3	OEH	Outputs enabled when OE is logic “H”, Outputs forced to GND when OE is logic “L”.			
4	UD	Shift direction control pin gate driver UD = H: Data shift direction from G1 to G800. UD = L: Data shift direction from G800 to G1.			
5	SHR	Shift direction control pin source driver SHR =H: Data inputs read sequentially from S800 to S1. SHR =L: Data inputs read sequentially from S1 to S800.			
6	SPV2	Start pulse gate driver			
		UD	Start pulse input	Start pulse output	
		H	SPV1	SPV2	
		L	SPV2	SPV1	
7	SPV1	Start pulse gate driver			
		UD	Start pulse input	Start pulse output	
		H	SPV1	SPV2	
		L	SPV2	SPV1	
8	SPH2	Start pulse source driver			
		SHR	Start pulse input	Start pulse output	
		H	SPH2	SPH1	
		L	SPH1	SPH2	
9	SPH1	Start pulse source driver			
		SHR	Start pulse input	Start pulse output	
		H	SPH2	SPH1	
		L	SPH1	SPH2	
10	VSS	Ground			
11	CKV	Clock gate driver			
12	VSS	Ground			
13	LV11N	Data signal source driver			
14	LV11P	Data signal source driver			
15	VSS	Ground			
16	LV10N	Data signal source driver			
17	LV10P	Data signal source driver			
18	VSS	Ground			
19	LV9N	Data signal source driver			
20	LV9P	Data signal source driver			
21	VSS	Ground			
22	LV8N	Data signal source driver			
23	LV8P	Data signal source driver			
24	VSS	Ground			
25	LV7N_D15	Data signal source driver			
26	LV7P_D14	Data signal source driver			
27	VSS	Ground			
28	LV6N_D13	Data signal source driver			

29	LV6P_D12	Data signal source driver	
30	VSS	Ground	
31	CLKN_GLOSTL	Data signal source driver	
32	CLKP_CKH	Data signal source driver	
33	VSS	Ground	
34	LV5N_D11	Data signal source driver	
35	LV5P_D10	Data signal source driver	
36	VSS	Ground	
37	LV4N_D9	Data signal source driver	
38	LV4P_D8	Data signal source driver	
39	VSS	Ground	
40	LV3N_D7	Data signal source driver	
41	LV3P_D6	Data signal source driver	
42	VSS	Ground	
43	LV2N_D5	Data signal source driver	
44	LV2P_D4	Data signal source driver	
45	VSS	Ground	
46	LV1N_D3	Data signal source driver	
47	LV1P_D2	Data signal source driver	
48	VSS	Ground	
49	LV0N_D1	Data signal source driver	
50	LV0P_D0	Data signal source driver	
51	VSS	Ground	

5.2 Panels Electrical Connection

SERVICE	CONNECTOR	TYPE NUMBER	NUMBER OF PINS	MATING CONNECTOR
mini-LVDS	CON1	P-TWO 187059-51221 compatible	51	P-TWO 187059-51221 compatible
	CON2	P-TWO 187059-51221 compatible	51	P-TWO 187059-51221 compatible

5.3 Panel Scan Directions



6. Display Module Electrical Characteristics

6.1 Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	VDD	-0.3 to +5	V
Positive Supply Voltage	VP3	-0.3 to +15	V
	VP2	-0.3 to +10	V
	VP1	-0.3 to +15	V
Negative Supply Voltage	VN1	-12 to + 0.3	V
	VN2	-10 to + 0.3	V
	VN3	-15 to + 0.3	V
Max .Drive Voltage Range	V_{POS} - V_{NEG}	52	V
Supply Voltage	VGH	-0.3 to +45	V
Supply Voltage	VGL	-30 to +0.3	V
Supply Range	VGH-VGL	-0.3 to +45	V
Operating Temp. Range	TOTR	+15 to +35	℃
Storage Temperature	TSTG	-25 to +50	℃

Note

- Maximum ratings are those values beyond which damages to the device may occur.
- Functional operation should be restricted to the limits in the Electrical Characteristics chapter.
- The recommended operating temperature should be kept from 15℃ to 35℃

6.2 Panel DC characteristics

Para meter	Symbol	Conditions	Min	Typ	Max	Unit
Signal ground	VSS			0		V
Logic voltage supply	VDD		2.7	3.3	3.6	V
	IDD	VDD=3.3V		34	70	mA
Gate negative supply	VGL		-22	-20	-19	V
	IGL	VGL=-20V		15	135	mA
Gate Positive supply	VGH		26	27	29	V
	IGH	VGH=27V		13	78	mA
Source negative supply	VN1		-9.5	-12	-13.5	V
	VN1-2		-6.85	-9.5	-11.25	V
	IN1			14	246	mA
Source negative supply	VN2		-9.75	-10	-10.15	V
	IN2			11	70	mA
Source negative supply	VN3		-12.5	-15	-16.5	V
	IN3			14	33	mA
Source Positive supply	VP1		14	16	18	V
	VP1-2		1.5	6	9.5	V
	IP1			29	355	mA
	VP2		8.5	10	12.5	V

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Source Positive supply	IP2			12	87	mA
Source Positive supply	VP3		20	23	25	V
	IP3			13	83	mA
Border supply	(Vcom_FPL)*		-3.5	Adjusted	-0.3	V
Asymmetry source	Vasm	VPOS+VNEG	TBD		TBD	mV
Common voltage	Vcom_TFT*		-20	Adjusted	20	V
	Icom_TFT			52	807	mA
	Vcom_FPL*		-20	Adjusted	20	V
	Icom_FPL			10	23	mA
Maximum Power panel	Pmax				17700	mW
Typical power panel	Ptyp			2200		mW
Standby power panel	Pstby			250		mW

Note

- Voltage adjusted by WFM setting.
- Border should be available controlled by WFM setting or floating.

Rush current	IDD	VDD=3.3V	-650		650	mA
	IGL	VGL=-20V			-8800	mA
	IGH	VGH=27V	-400		400	mA
	INEG-1	VNEG-1=-15V			-5300	mA
	INEG-2	VNEG-2=-15V			-4300	mA
	INEG-3	VNEG-3=-15V			460	mA
	IPOS-1	VPOS-1=15V			7800	mA
	IPOS-2	VPOS-2=15V			5000	mA
	IPOS-3	VPOS-3=15V			5300	mA
	Icom_TFT		-3860		3860	mA
	Icom_FPL		-175		175	

Note

- The Maximum power consumption is measured with following pattern transition: from LineA to LineB.(Note 6-1)
- The Typical power consumption is measured with following pattern transition: from horizontal 8 generic color pattern to vertical 8 generic color pattern (Note 6-2)
- VNEG & VPOS should be available controlled by WFM setting.
- Vcom-TFT & Vcom-FPL should be available controlled by WFM setting.
- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display.
- Vcom is recommended to be set in the range of assigned value ± 0.1V.
- The rush current is for reference only.

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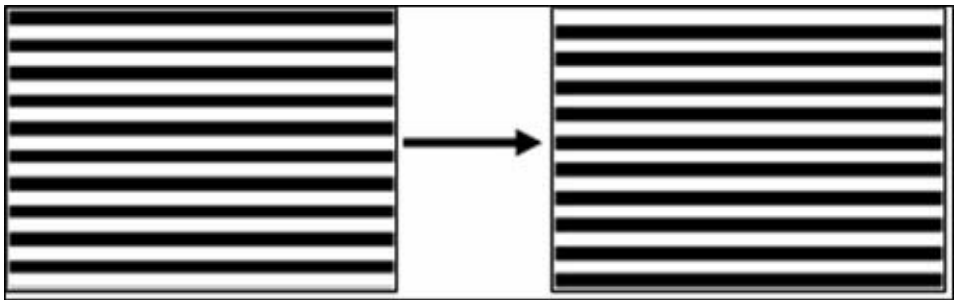
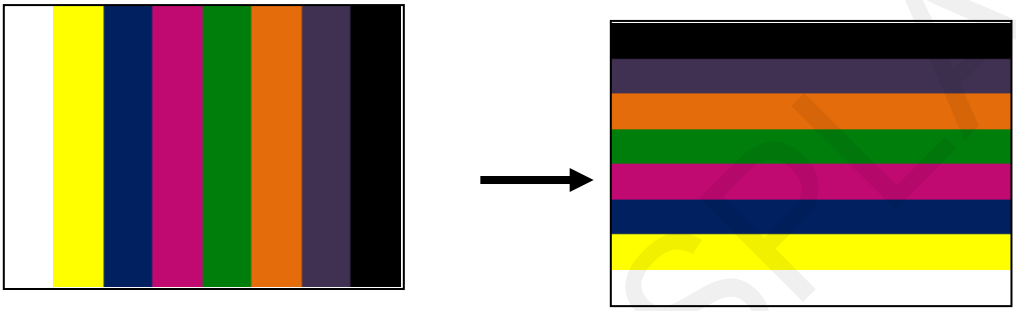
Note 6-1
The Maximum power consumption



Note 6-2
The Typical power consumption



6.3 Refresh Rate

The module GDEH253C01 is applied at a maximum screen refresh rate of 65Hz..

	Min	Max
Refresh Rate	-	65Hz

6.4 Panel AC characteristics

VDD=2.73V to 3.6V, unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Unit
mini-LVDS differential voltage	V_{ID}	300	-	-	mV
mini-LVDS common mode input voltage range	V_I	0.4	1.0	VDD-1.4	V
Source Clock frequency	F_{CLK}	-	-	150	MHz
Source Clock duty	t_{DUTY}	45	-	55	%
Source Clock setup time	t_{SETUP1}	1.1	-	-	ns
Source Clock hold time	t_{HOLD1}	1.1	-	-	ns
Rise time	t_{RISE}	-	-	0.15	Unit interval
Fall time	t_{FALL}	-	-	0.15	Unit interval
LE rising to reset input time	$t_{LE\text{-}RESET_HIGH}$	200	-	-	ns
LE falling to reset input time	$t_{LE\text{-}RESET_LOW}$	200	-	-	ns

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Start pulse delay time	t_{PLH1}	-	-	4	CLK
	t_{PHL1}	-	-	4	CLK
Reset high period	t_{RESETH}	3	-	-	CLK
Receiver off to LE timing	$t_{REC-OFF}$	40	-	-	CLK
LE width	t_{LE}	300	-	-	ns
Reset low to LE rising time	$t_{RESET-LE}$	0	-	-	ns
Gate clock frequency	f_{CLK}	-	-	200	kHz
Gate clock pulse high period	t_{CLKH}	500	-	-	ns
Gate clock pulse low period	t_{CLKL}	500	-	-	ns
Gate clock rise time	t_{IR_CLK}	-	-	100	ns
Gate clock fall time	t_{IF_CLK}	-	-	100	ns
Gate Start pulse setup time	t_{SU}	100	-	t_{CLKH}-100	ns
Gate Start pulse hold time	t_{HD}	100	-	t_{CLKL}-100	ns
Gate Start pulse rise time	t_{IR_STV}	-	-	100	ns
Gate Start pulse fall time	t_{IF_STV}	-	-	100	ns
Gate STV output delay from CLK	t_{OD_STV}	-	-	500	ns
Output delay time from CLK	t_{D_OUT}	-	-	2	us
Output rise time, output pins	t_{R_OUT}	-	-	1	us
Output fall time, output pins	t_{F_OUT}	-	-	1	us
XONL/R pulse width	t_{WXON}	10	-	-	us
Output delay time from XON	t_{DXON_OUT}	-	-	20	us

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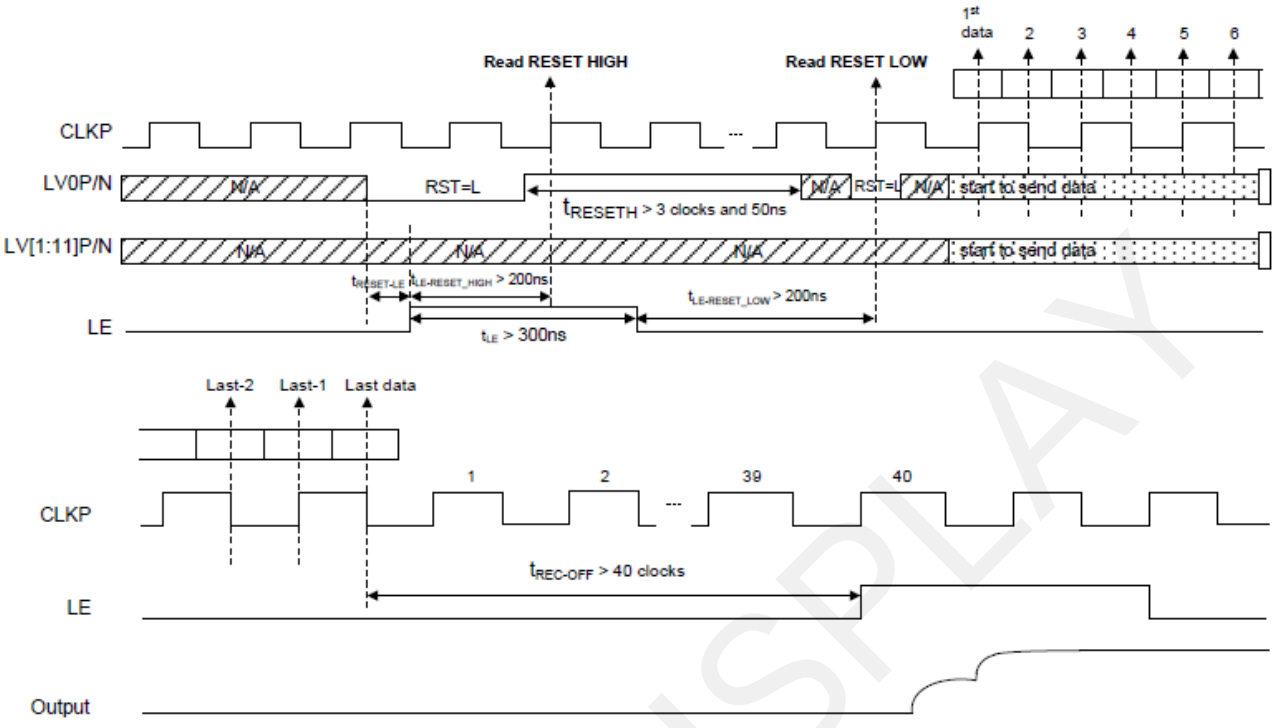
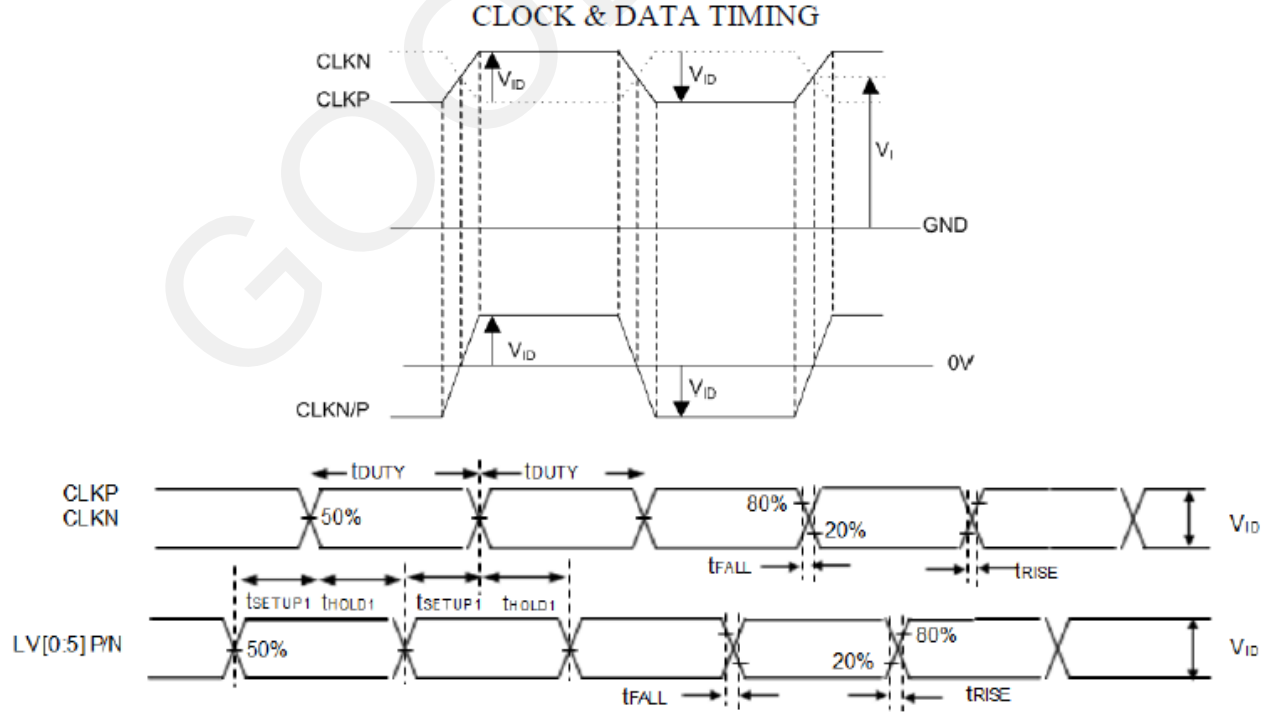
OUTPUT LATCH CONTROL SIGNALS



CLOCK & DATA TIMING



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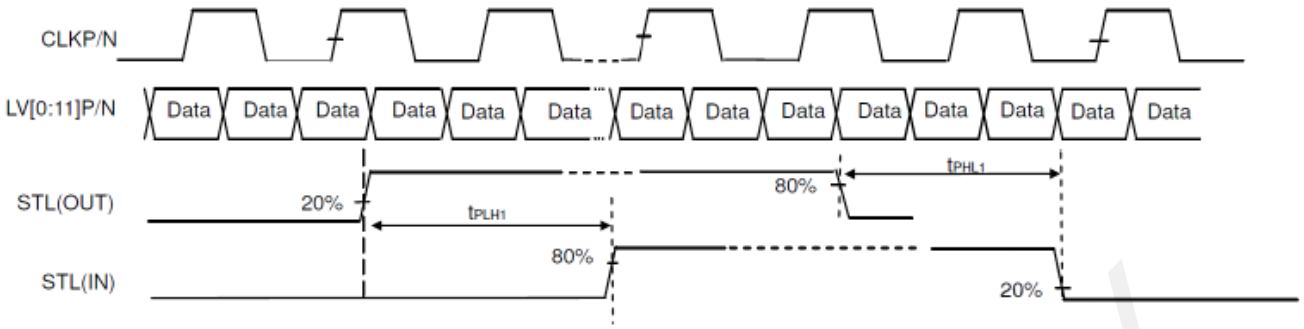
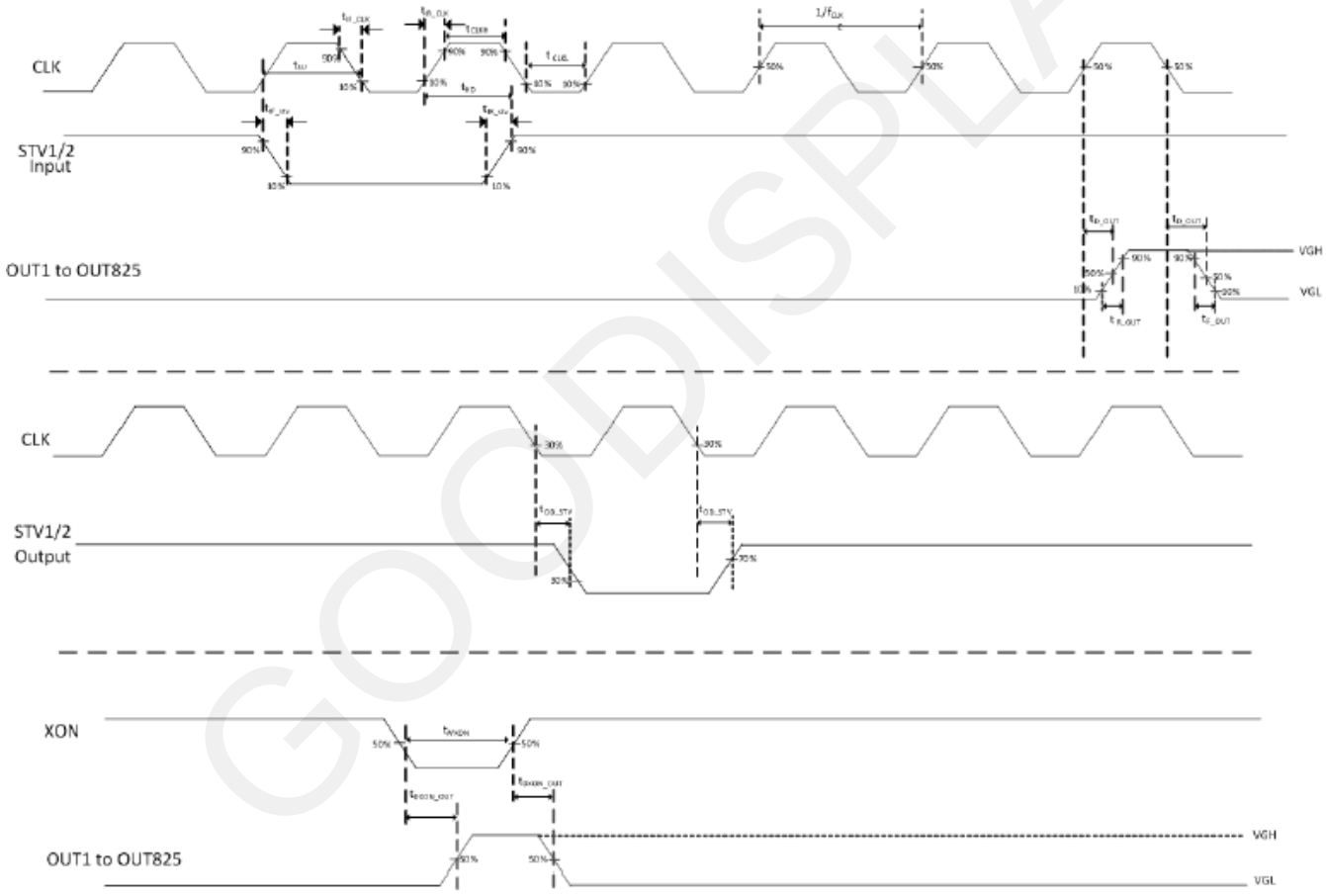
CKV & SPV TIMING



GATE OUTPUT TIMING



Note：First gate line on timing

After 5CLK, Gate OUT1 is on.

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6.5 Controllers Timing

The timing mode is depicted on Figure 6.1 and Figure 6.2 and it refers to timing of Source Driver Output Enable (SDOE) and Gate Driver Clock (GDCK). Note, the controller timing in the mode LGON follows GDCK timing.

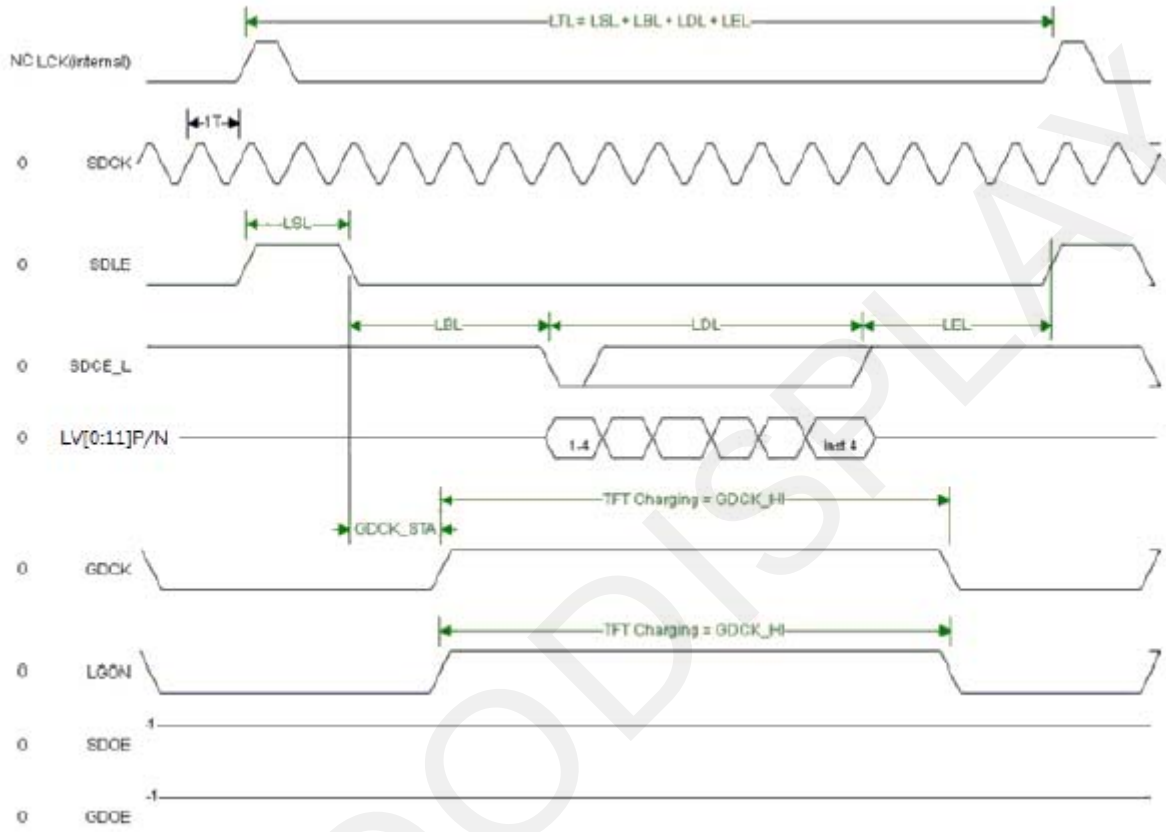


Figure 6.1 Line Timing in Mode 3

Note: LCK is an internal signal and it is shown for reference only.

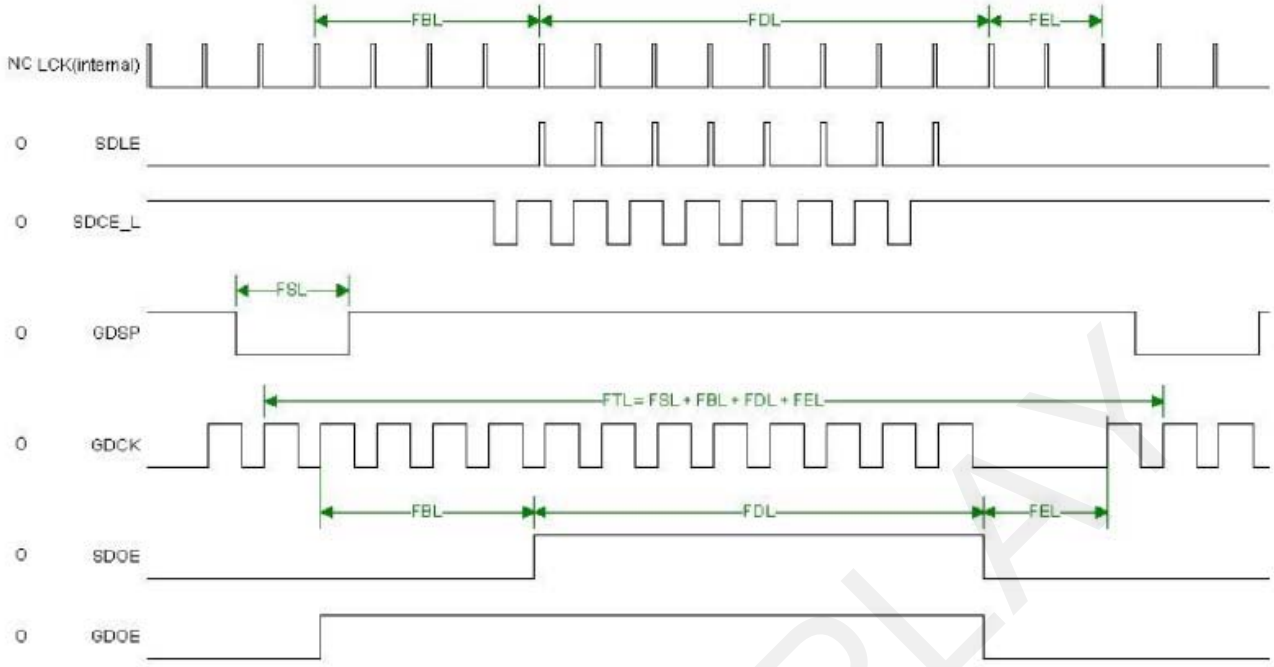


Figure 6.2 Frame Timing in Mode 3

Timing Parameters Table

Mode	3	Resolution 3200x1800				
SDCK(MHz)	60					
Pixels Per SDCK	8					
Line	LSL	LBL	LDL	LEL	GDCK_STA	LGONL
Parameters[SDCK]	17	52	400	40	1	453
Line	-	-	-	-	-	-
Parameters[us]	0.28	0.87	6.67	0.67	0.016	7.55
Frame	FSL	FBL	FDL	FEL	-	FR[Hz]
Parameters[lines]	1	4	1800	6	-	65.09
Frame	-	-	-	-	-	-
Parameters[us]	8.48	33.9	15270	50.9	-	15363

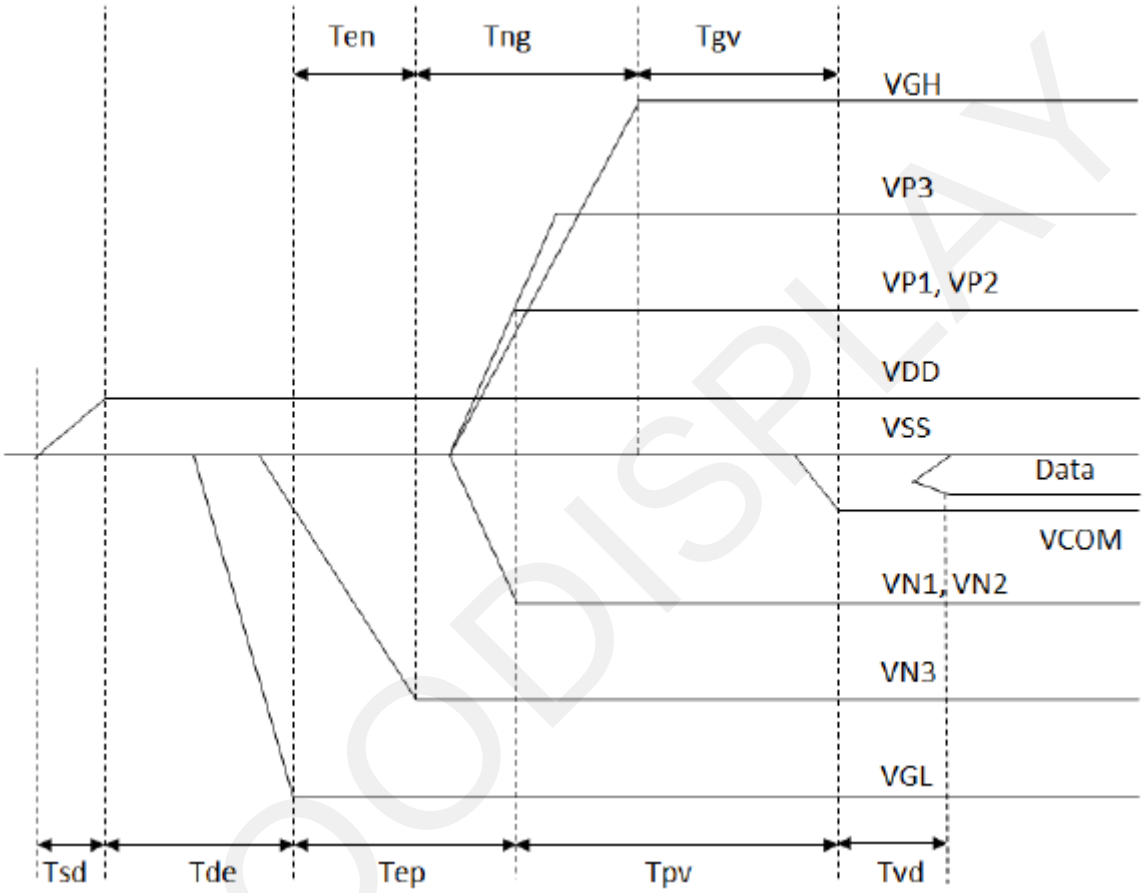
Note 1: For Freescale SoC GDOE Low pulse represent FSL and GDSP pulses with the first period of FBL Note 2:
SDCLK = XCL
LV[0:11]P/N = LV0P~LV11N
SDCE_L = XSTL
GDCK = CKV
GDSP = SPV
GDOE = Mode1
SDOE = XOE

7. Power Sequence

Power Rails must be sequenced in the following order:

1. VSS → VDD →VNx → VPx (Source driver) → VCOM
2. VSS →VDD → VGL →VGH (Gate driver)

POWER ON



	Min	Max
Tsd	30us	-
Tde	100us	-
Tep	1000us	-
Tpv	100us	-
Tvd	100us	-
Ten	0us	-
Tng	1000us	-
Tgv	100us	-

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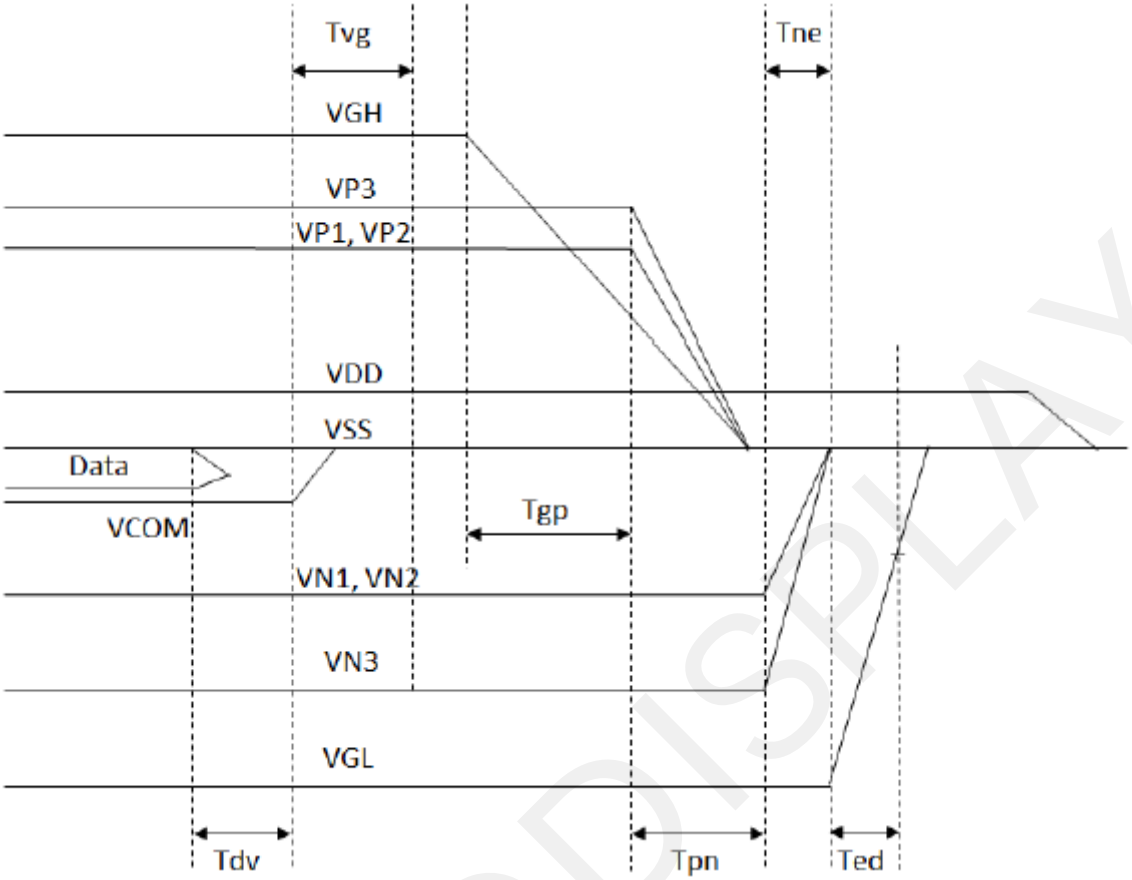
POWER OFF



	Min	Max	Remark
Tdv	100μs	-	-
Tvg	0μs	-	-
Tgp	0μs	-	-
Tpn	0μs	-	-
Tne	0μs	-	-
Ted	0.5s	-	Discharged point @ -7.4 Volt

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8. Optical characteristics

8.1 Specification

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
R	Reflectance	White		35	-	%	Note 8-1
CR	Contrast Ratio	-	8	10	-		-
Gamut	Color Saturation	-	45K	55K		dE^3	
Rendered Color	Color Performance	Cyan (0,131,163)		(TBD)		L*,a*,b*	Note 8-2 8-3
		Magenta (196,0,137)		(45.1, 32.2, -6.4)			
		Yellow (216,203,0)		(65.1, -9.1, 43)			
		Red (190,26,0)		(45.2, 24.5, 21.5)			
		Green (0,137,39)		(TBD)			
		Blue (59,0,137)		(33.9, 15.5, -23)			
		Black (0,0,0)		(22.7, 6.3, 1.3)			
		White (255,255,255)		(70.5, -1.3, 3.5)			
	Color Variation	dE_{2000}			10	dE	
T_{update_RS}	Update time	Clean mode → image		36		sec	Note 8-4

Note 8-1：Luminance meter：Eye – One Pro Spectrophotometer;

Note 8-2：The rendered color inputs are chosen to illustrate the color capability of the reflective ACeP display;

Note 8-3：8 rendered color performance values at 25.5 ℃ ambient; Color meter – PR655 Spectroradiometer Note;

8-4：Pattern switch：Clean mode (White) Picture; not include dwell time

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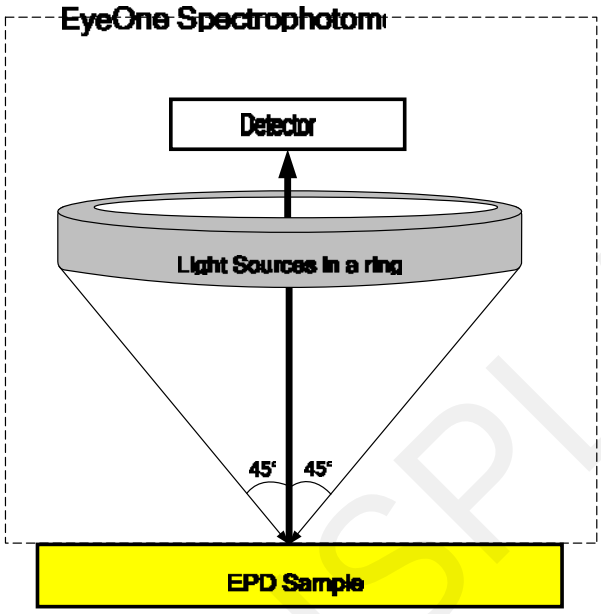
8.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd):

CR = Rl/Rd



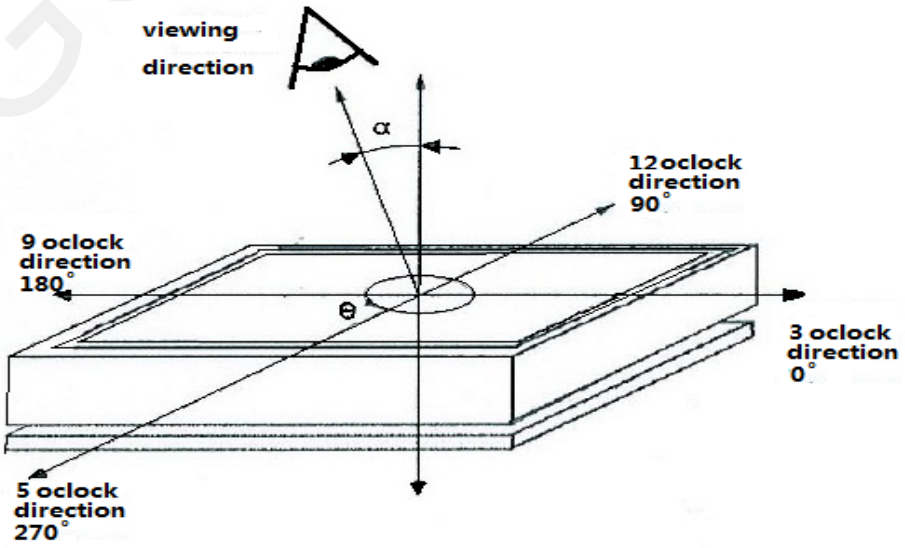
8.3 Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{\text{white board}}$ x (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1).

$L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



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9. Reliability test

9.1 Reliability Test Items

	TEST	CONDITION	REMARK
1	High-Temperature Operation	T=35℃, RH=35%RH, for 240Hr	
2	Low-Temperature Operation	T = 15℃, RH=35%RH for 240 hrs	
3	High-Temperature Storage	T=60℃ RH=35%RH For 240Hr	Test in white pattern
4	Low-Temperature Storage	T = -25℃ for 240 hrs	Test in white pattern
5	High Temperature, High-Humidity Storage	T=60℃,RH=80%RH,For 240Hr	Test in white pattern
6	Temperature Cycle	-25℃(30min)~60℃(30min),50 Cycle	Test in white pattern
7	Package Vibration	1.04G,Frequency : 20~200Hz Direction : X,Y,Z Duration: 30 minutes in each direction	Full packed for shipment
8	Package Drop Impact	Drop from height of 100 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment
9	Electrostatic discharge(non-operating)	Machine model: +/-250V,0Ω,200pF	

Actual EMC level to be measured on customer application.

Note1：Stay white pattern for storage and non-operation test.

Note2：The function, appearance should meet the requirements of the test before and after the test.

Note3：Keep testing after 2 hours placing at 20℃-25℃

Note4: The protective film must be removed before temperature test.

9.2 Product warranty

Warranty conditions have to be negotiated between Good Display and individual customers.

Good Display provides 12+1(one month delivery time) months warranty for all products which are purchased from Good Display.

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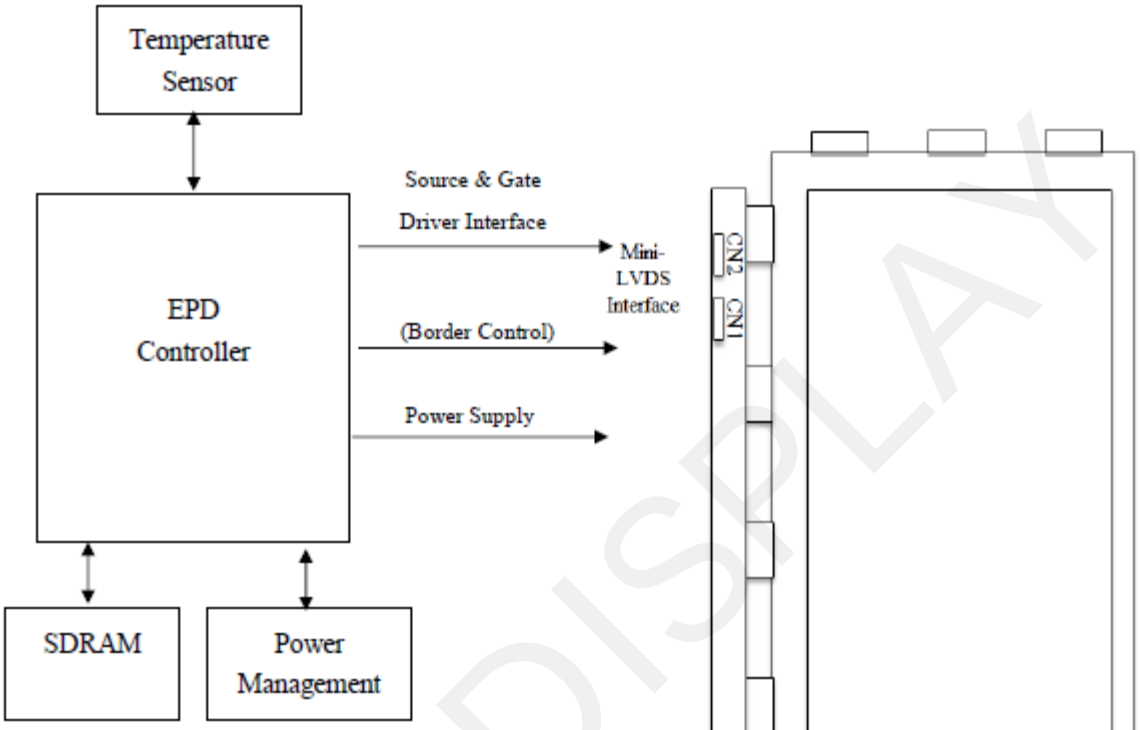
10. Block Diagram



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11. Handling, Safety and Environmental Requirements

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

Product Environmental certification
RoHS

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12. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended to refreshed the ESL /EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.

(7) For more precautions, please click on the link:
https://www.good-display.com/news/80.html

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